Electronics

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Module No. # 05

Lecture No. #28

FETS and MOSFETS

CMOS Inverter

Mosfets are popularly called as mos transistors. Now mosfets have many advantages as we have talked earlier, they take fewer steps for construction they take much lesser space, they have very high input impedance thus they consume very low powers. Besides that there are certain other points which go in favor of mosfets, and these other factors are that mosfets can be connected. We have seen as amplifiers as switches of course, but besides that they can be connected as resistors, and capacitors also. Now, you may say that in a circuit if the purpose is served just by connecting a resistance, then what is the necessity of replacing it by a mos transistor for example, there is a advantage.

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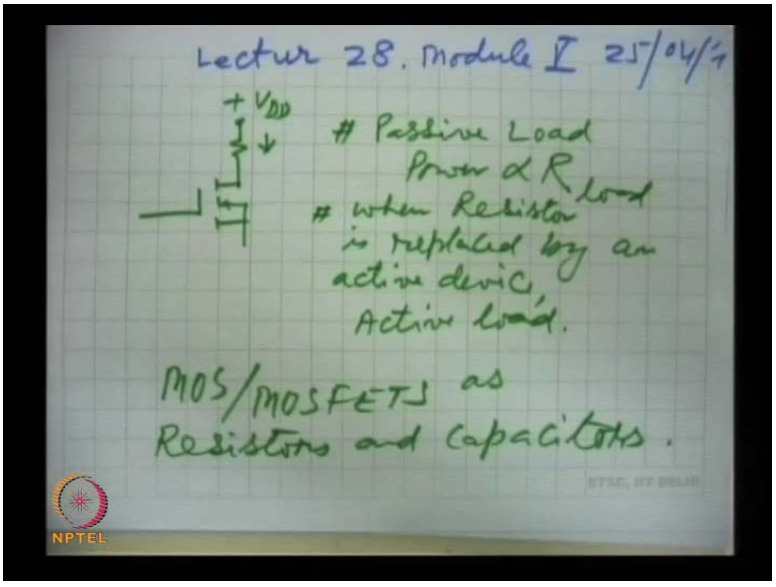

When we connect a resistance for example, in a circuit like this. Here this is the resistance connected, and when the current flows through this resistance, there is a

dissipation of power the normal i square R the heating of a resistance that is a shear dissipation of energy. Now, if this transistor can be replaced by another transistor; for example, we are at the moment talking of mosfets. So, if this is replaced by a mosfet then also as a resistance then also the circuit will work and it will be power wise more efficient than this resistive load. When a circuit makes use of a resistance as a load this is called passive load passive load passive load the resistance which consumes power proportional to R the value of load which we are using, this is a passive load. Active load when resistor is replaced by an active device which acts as a resistor then this is called active load.

So, besides power saving there is additional advantage, because today very large number of circuits are actually in integrated circuit form, in integrated circuits remember one thing that creating one for example, in a unit one mosfet and one resistance is more expensive and it will take more steps for fabrication then two resistors. That means, if we can replace this resistance by a mosfet then the circuit will take make two mosfets, but making of two mosfets are in. In fact, just multiplying in some component is much more economical and convenient in a integrated circuit rather than creating a different element all together resistance and mosfet two are very different elements and two mosfets they are they are they belong to the same category and hence their construction is very simple and more economical. So, now we start that how a mosfet a mos can be connected as a resistor and as a capacitor. So, mos which is same as mosfets as resistors and capacitors. First we take how a mosfet can be connected as a resistor.

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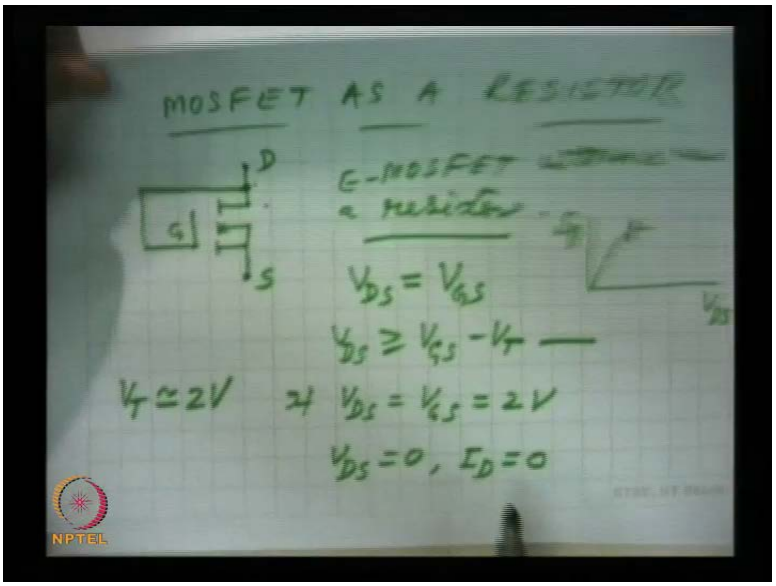

So, mosfet as a resistor let us one of the ways a mosfet can be connected to work as a resistor is this is a mosfet in which we have connected this is gate, this is drain and this is source the gate has been shorted internally to the drain in this the E mosfet that means, enhancement mosfet works as a resistance as a resistor. Because, now we will show we will show this point because here since we have shorted the gate with the drain then this voltage VDS between drain and source is same as VGS. This is shorted and we are this is VGS. So, this is same as this voltage VDS, VDS is equal to VGS and the condition we remember we remember that drain and VDS that condition here.

So, that this mosfet works in the saturation region that condition is that VDS is equal or greater than VGS minus V T. If this condition is satisfied then this mosfet when connected this way with other parts of the circuit of course, then it will work as a resistor. It will work as a in the in the saturation region of the characteristics and we will show that this will work as a resistor. Now if VDS is equal to VGS if VDS is equal to VGS then for all voltages above V T with threshold voltage is around 2 volts normally. So, if VGS is equal to 2 volts then in this condition VDS will be 0 and VDS 0 implies zero drain current drain current is zero.

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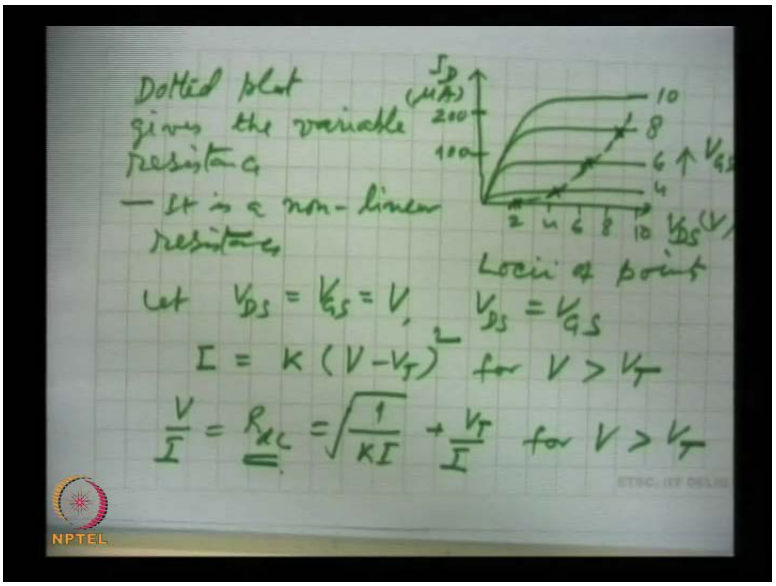

So, if we make a plot of this point that different values of VDS are equal to VGS then we get a plot like this. VDS in volts and drain current in micro amperes and here it is 200 micro ampere. Here it is typical values 100 micro ampere and so, on then the plot as we have talked here when what is the loci of these points where VDS is equal to VGS and we have seen that when VGS is 2 volts then VDS will be 0 and I D will be 0 and that point will start from here and then 4, 6, 8 and so, on. So, here this is the loci of the points here this is loci of points VDS this is VDS is equal to VGS this is output voltage and this is of course, drain current and this slope of this curve this dotted curve that will give the resistance. These will the resistance which is of course, varying because the slope of this curve is varying.

So, dotted plot gives the variable resistance of the device when the device is connected in this fashion and we can see here that this resistance of course, is a it is a non-linear resistance and because normally we work in this region. So, there any value depending on the type of mosfet which we are using we can choose. So, we can see that this acts as a resistance and we can calculate that value and let VDS equal to VGS which is true for all these points equal to V then in this saturated region the drain current which is I it varies as K VGS. Which is now V minus V T square this is for voltages greater than V T by solving this we can get the ratio V by I, V by I ratio which gives the dc resistance and this comes out to be 1 by K I plus V T by I.

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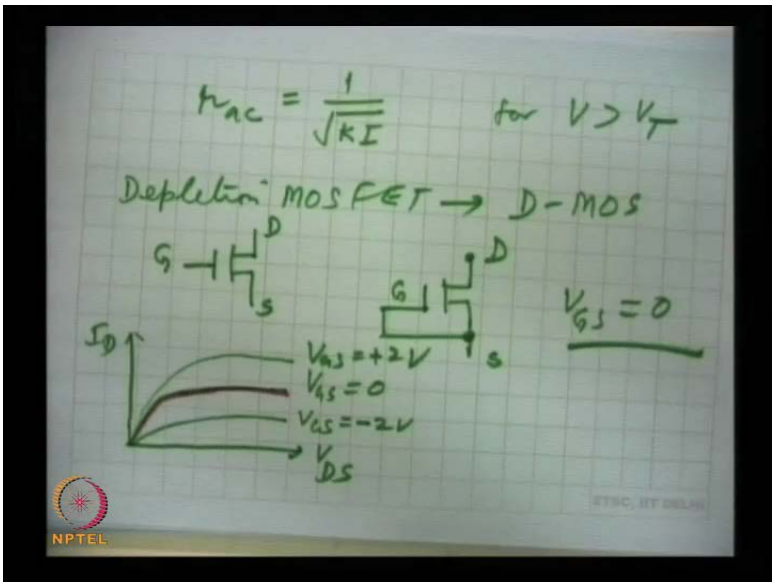

So, this is the value of resistance this is true for voltages greater than V T and when we differentiate this is dc resistance. Which this device will give and by differentiating it we can get the ac resistance and that comes out to be R ac by differentiating this equation and this comes out to be 1 by root K I where K is the device constant this we have discussed when we were discussing the enhancement mosfet. So, this is the value of ac resistance and this is also true for V greater than V T.

So, this way the resistances can be calculated and for the device we know what is the K and what are these drain characteristics from there we can find the value. This was how a enhancement mosfet can be connected as a resistor. Similarly, a depletion mosfet a depletion mosfet normally the most commonly used symbol for depletion mosfet. Which is written as depletion DMOS, the most commonly used symbol for DMOS is this is drain, source and gate this is DMOS symbol very commonly used and this gap is the difference with the j f e t in junction field effecter junction field effect transistor this gap is absent. So, this gap is now this mosfet can be connected like this.

This is source, this is gate and this is drain when we connect like this then obviously, VGS is 0 this is VGS is 0. Because both have been shorted and on the drain characteristics this is VDS and this is I D and this is VGS equal to 0. Here it goes negative value VGS equal to for example, minus 2 volts here this is VGS equal to plus 2 volts because a depletion mosfet can be used as a enhancement mosfet as a depletion

mosfet and so, on. This we have talked. So, in under this condition this represents the slope of this one, VGS equal to 0. Now the slope this is very high resistance this is almost flat this is the voltage, this is the current and so, this slope inverse of this slope voltage by current that represents the resistant is a very high resistance. So, a DMOS can be connected like this by shorting gate with the source as a resistor.

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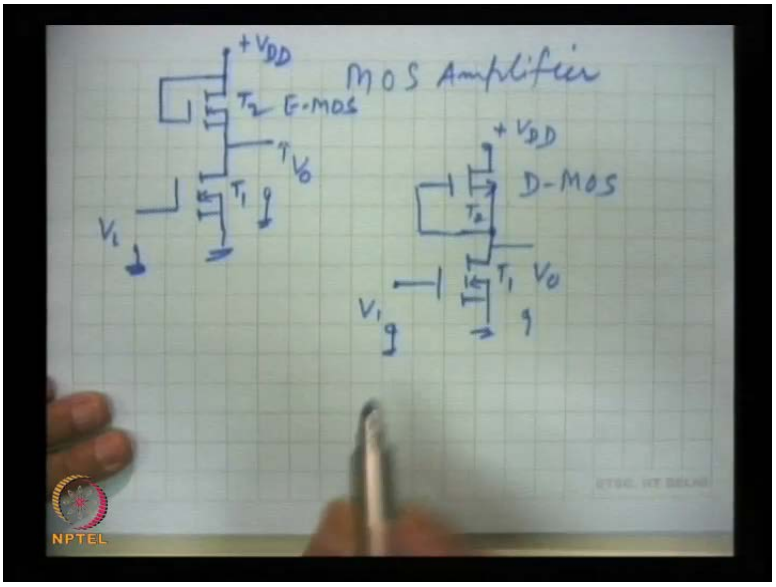

How the circuits will look the circuits with active load will look like this. This is the E mosfet connected as load and this is for example, say a amplifier. So, these two transistor T 1 and T 2 they give the complete active load and amplifier circuit. So, this is a mos amplifier in the same way we can connect a depletion mosfet instead of E mosfet this is E mosfet this is the DMOS this is D mos as load and this is the EMOS for as amplifier, we get output here input is given at this gate of T 1 and this is T 2. So, input is given here and output is taken here this is another a mos amplifier with EMOS acting as amplifier and depletion mosfet D mosfet as load. So, these are the amplifiers they can be analyzed and completely satisfactory performance can be obtained.

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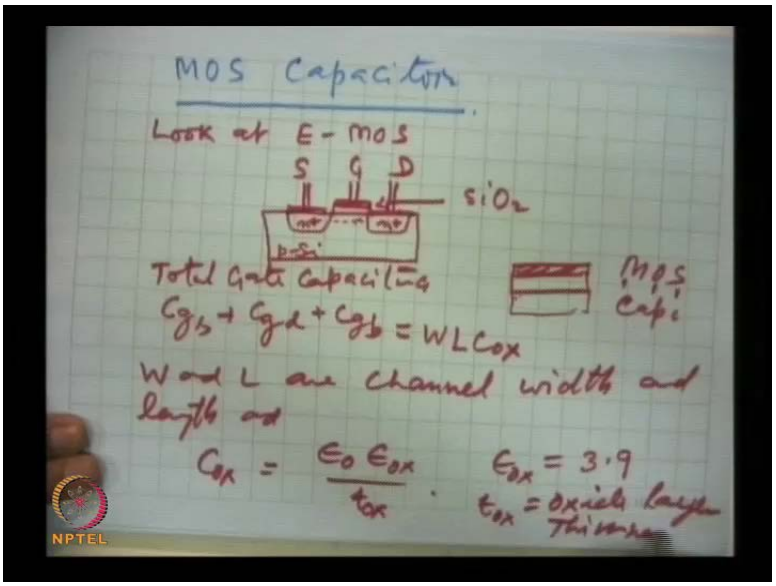

So, this is how that a mos transistor can be connected as a resistor. So, such circuits on a chip will contain only most circuits properly connected. Then we take most capacitor we will recall the structure of EMOS. Let us look at EMOS and the EMOS structure was like this is p silicon this is an heavily doped and one is drain the other is source and this was the s i o 2 layer and over that there is a metal here also there is metal this is also metal and then this is gate source and this is drain, now here this is the channel. So, this structure is known to you. Now this forms the metal at the gate metal and then insulating s i o 2 and then here this is also having conductivity much higher conductivity as compared to the s i o 2 layer. So, this is another this is semi conductor actually at the back. So, this is an mos capacitor metal oxide semi conductor.

So, this capacitor can be used as a capacitance and this gate capacitance can be because there are overlap regions with the source and drain. So, the gate source g s gate source capacitance plus the total gate capacitance can be shown as consisting of three terms the gate source voltage, the gate and drain C g s, C g d plus C g b body this body. This acts as so, the total gate capacitance that contains three terms because of the overlap of the gate region with the source and drain. So, this is equal to W L C o x where W and L are channel width and length and this C o x this is equal to epsilon 0 epsilon oxide layer dielectric constant and thickness of the layer. Where this is the dielectric constant of the s i o 2 and which is 3.0 around 3.9 and this is the permittivity of free space and this is the thickness oxide layer thickness. oxide layer thickness.

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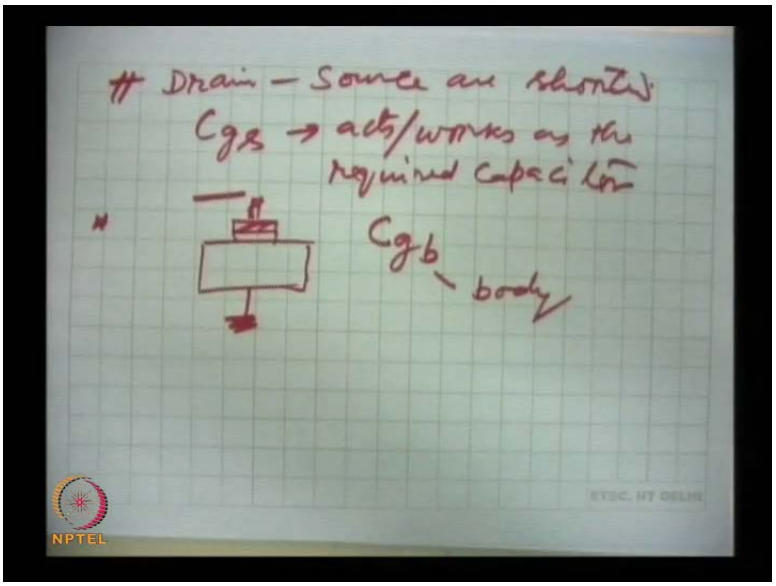

So, this is one way the capacitor can be realized in another form of the capacitor the drain and source they are shorted and C g s acts works as the required capacitor. This is another way one way as capacitor was shown here where the total gate capacitance contained three terms one, two, three and another way is when drain source are shorted together and the capacitance between gate and source is used and third possibility is that for example, if the one side of this capacitor is grounded for example, the body side here. This is the layer oxide layer and here and this is the body which is the semi conductor this is grounded then.

We can directly use C g b, b for body this. So, this is another way very often the mos devices are connected as capacitors here there is no need to create a source and drain they are absent they are not required. So, this way the capacitor C g b is quite popular and very often the devices are connected like that. So, this is how the three ways a capacitance can be obtained a capacitor can be formed by most device. So, the circuits will contain purely mos devices some will be connected as amplifiers others will be connected as active loads and still others may be connected as capacitors. So, that it is all the mos network in which different mos are working as either as amplifier or as capacitor or as active load.

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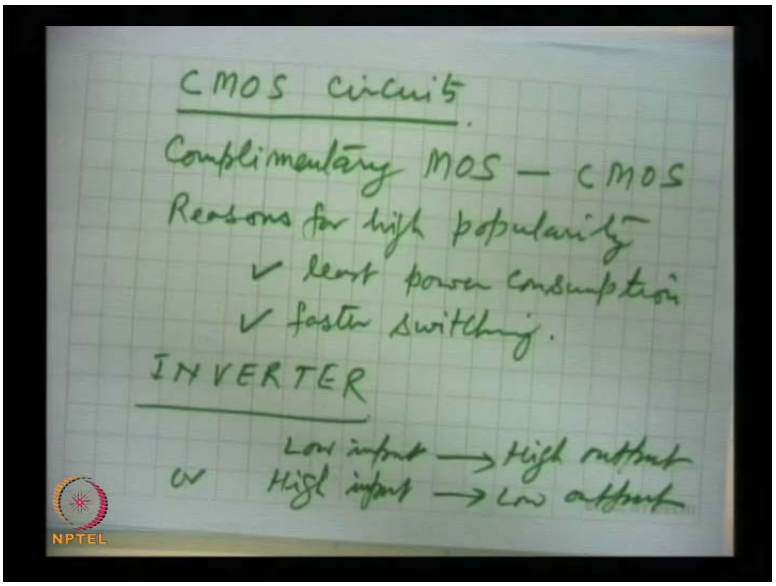

Now, we go for another kind of mos circuits which are very popular and these are CMOS circuits CMOS, C tends for complementary mos complementary mos CMOS. What is CMOS normally we have seen that we use either NMOS or PMOS, but CMOS is on the same chip NMOS and PMOS are simultaneously present they are connected. We will take example in which one circuit will be a PMOS the other one transistor will be p mos the other transistor will be NMOS for example, we took these few examples of the circuits they were connected of course, in a resistance configuration, but otherwise the one has to be one can be a PMOS other can be NMOS for a CMOS circuit. This is a special connection where they were connected as resistors.

So, remember that complementary mos CMOS that contains on the same chip the PMOS and NMOS devices simultaneously. CMOS are very widely used in advanced circuits they are most popular and the reason for their popularity are these reasons for high popularity all the advantages which mos devices offer over b j t that we have talked in addition to that one advantage is least power consumption least power consumption till today the lowest power consumption shown by exhibited by any logic is by CMOS least we will see that why it is least. So, power dissipation that means, power consumption is least in CMOS this is one reason and yet another reason for their popularity is faster switching by speed with which they can switch from one state to another high to low or low to high this is very high.

Now, we will take one device which is called the inverter circuit what is the inverter circuit, what is its function and why am taking it why it is. So, important that it should be taken first inverter means first let us see the function the function is a circuit in which low input results into high output low input results in high outputs or high input similarly, high input will result into low output. This is the inversion function voltages have been inverted a low input results into high output inverted from low to high or high input from high to low output. So, that is the function of the inverter.

Now, inverter is very fundamental for any digital circuit most fundamental for any digital circuits the circuits which work on two states high and low 0 and 1 false or true whatever you may call, but actually electric electronic circuits under the voltages.

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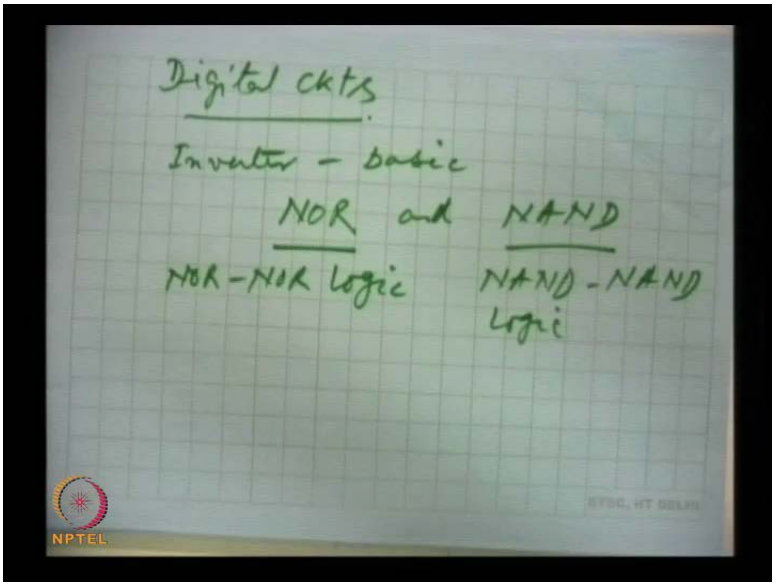

So, the voltages are low or high and the circuits respond to that and all logics can be constructed based on these circuits. Now for any distort circuit inverter function is basic and by combining inverters we can get for example, if time permits then we may also take these circuits the two most fundamental and I mean most important universal gates the NOR gate and NAND gate inverter circuit is also called not function or not gate and by combining these inverters we can get a NOR logic or NAND logic. I repeat that inverter circuit inverter function is basic to any distort circuit and by extending the functioning function of the inverter by connecting inverters. We can get NOR function or a NAND function any logic can be realized can be constructed in NOR logic two level

NOR logic can result in any logic you can form you can realize or instead of NOR we can use NAND and we can get what we call NAND logic.

Two levels logics are most popular NAND logic and similarly here NOR, NOR-NOR logic, NAND, NAND-NAND logic. So, they are most important for any circuit and to these NOR and NAND inverter function is fundamental. So, first we take a inverter function. Let us first before moving to CMOS, let us take a inverter with a resistive load and then later we replace that resistance with another transistor and that will become CMOS.

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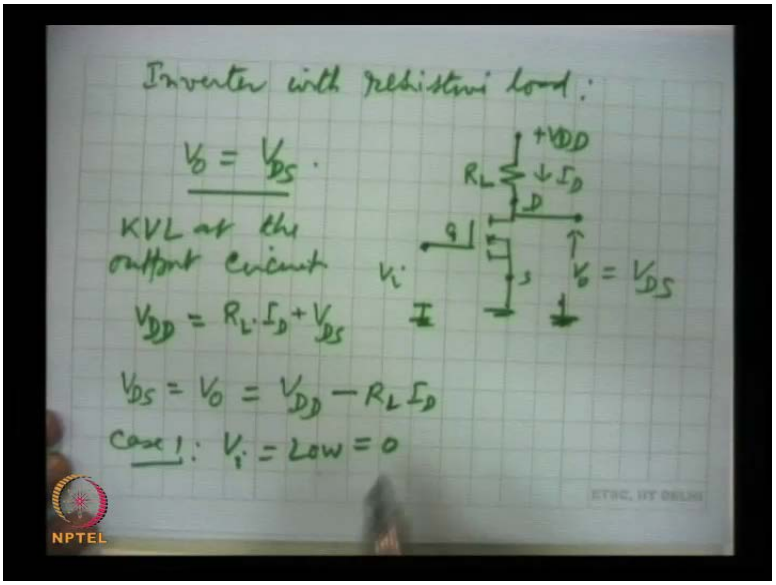

So, inverter with resistive load is the resistance across which we take the output. So, it is called load resistor with resistive load. So, the simple circuit is this is the EMOS and this is VDD and this is the load resistor R L, this is drain this is gate and this is source and output is taken here from here we take the output with respect to ground the input is given between gate and source is of course, grounded this is the input and output is taken here and this is the EMOS and this is the load. Now the output we are taking as V out we are taking as between drain and source VDS, if a current drain current I D flows through it then at the output circuit we can write the kirchoff's voltage law at the output circuit and that is simply summation of voltages.

So, VDD is equal to R l into I D plus VDS this is VDS same VDS and here or VDS is that is the output V 0 from here itself this is VDD minus R L into I D. Now see how will

it work case 1: when input is low this V i is low that means, it is 0 when this is 0 then obviously, because V i is also same as VGS is same as VGS and since it is 0. That means it is obviously, less than V T this will require high voltage for its conduction, but in the present case input is low that means, VGS is less than V T no conduction channel will be formed and I D the drain current will be 0. If drain current is 0 here this term becomes equal to 0 and output becomes equal to VDD. Which is normally will be 5 volts that is high, low input results into high output this is what we expect from the inverter function.

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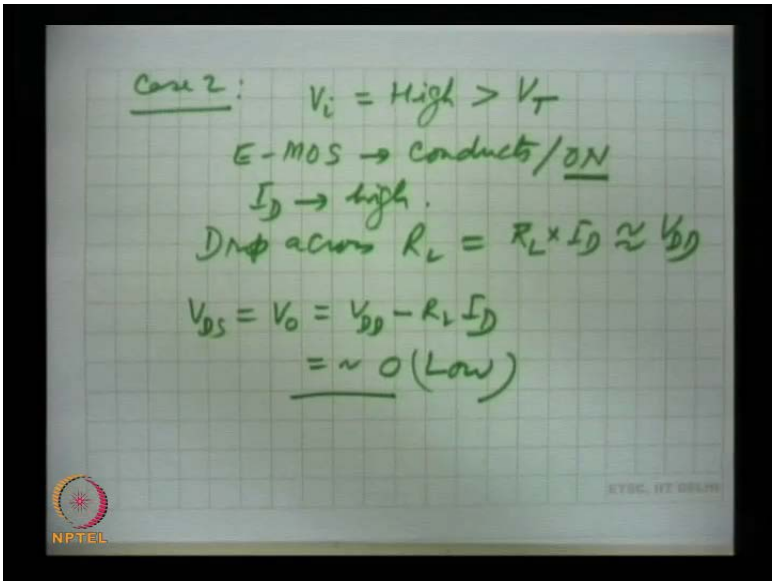

So, this is case 1 when input was low. We take case 2 when input when when input is high V i is high and it is greater than the threshold voltage required for the channel formation in the device. So, under this condition this will conduct EMOS conducts that means, it is on earlier it was off. Here this is on and current will flow and in this equation now there is a current a resistance. So, there will be a quite a bit voltage drop across this and that voltage drop may be close to VDD itself and therefore, I D high and drop across R L will be R L into I D which may be close to VDD therefore, from this equation which we wrote initially this equation VDD, VDS which is output this was shown to be VDD minus R L I D and since this is also equal almost equal to that.

So, this will be close to 0 that means, low. What we are getting in this circuit which is a resistive load inverter when input is low we are getting high output and when case 2 an input is high then we are getting low output close to 0 this is inverter function and this

was the conventional case and now we can take the CMOS the complementary mos in which we will replace this transistor also this resistance also with the mos of another kind if it is NMOS then it has to be PMOS and as we said in the beginning that in the complementary mos the NMOS and PMOS transistors are simultaneously present on the same chip. So, that will be the CMOS inverter.

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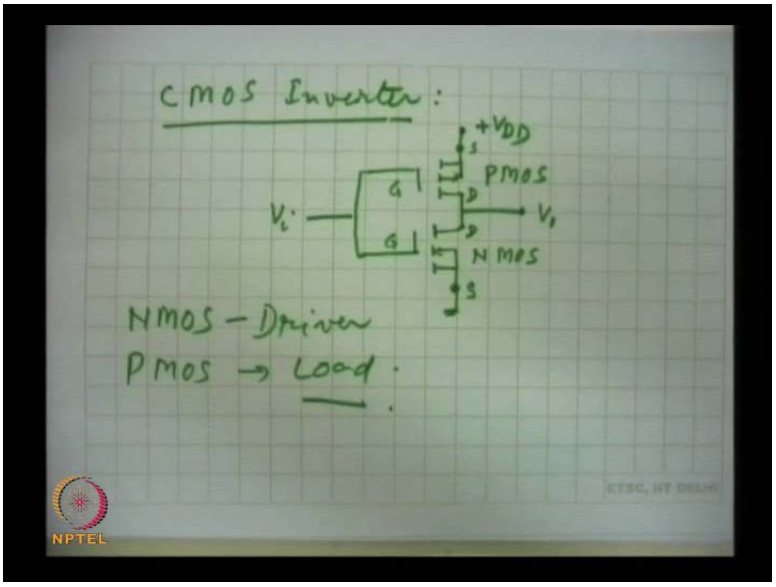

So, we can take the objective why we took this inverter this is with the resistive load to tell you what is the function of the inverter and how it is it can be realized by a resistive load. Now we can move to CMOS inverter in which the PMOS and NMOS transistors will be simultaneously present. So, here is the circuit this is the circuit this is NMOS this is PMOS and this is gate, this is source and note here that the source is here and this is drain and this is also drain for NMOS if this circuit the NMOS x as a driver it will drive the PMOS. So, technically it is known as driver and PMOS is acting as load. We said that we are going to replace the resistive load with another kind of transistor. So, we have replace the transistor with PMOS.

So, PMOS will act as a load and NMOS will act as a as a driver and input is formed by connecting both gates together as it is clear from the figure both gates have been connected together to form the input. So, input is taken from these combined gates with respect to ground and similarly, by connecting drains together the output is taken with respect to ground. Now we will see how this circuit works first let us note that PMOS

requires this important that PMOS requires a negative voltage at the drain instead of using two batteries one for the NMOS another for the PMOS the same function can be obtained by connecting source to a positive voltage.

I repeat what I have said that PMOS requires a negative voltage minus VDD at the drain. Now there are two ways it can be achieved one is that we connect a negative VDD at the drain or we connect a positive voltage source at the source. So, this is what the later scheme is followed in this figure. So, this is the way the single source single dc source VDD is used is used to bias PMOS and NMOS.

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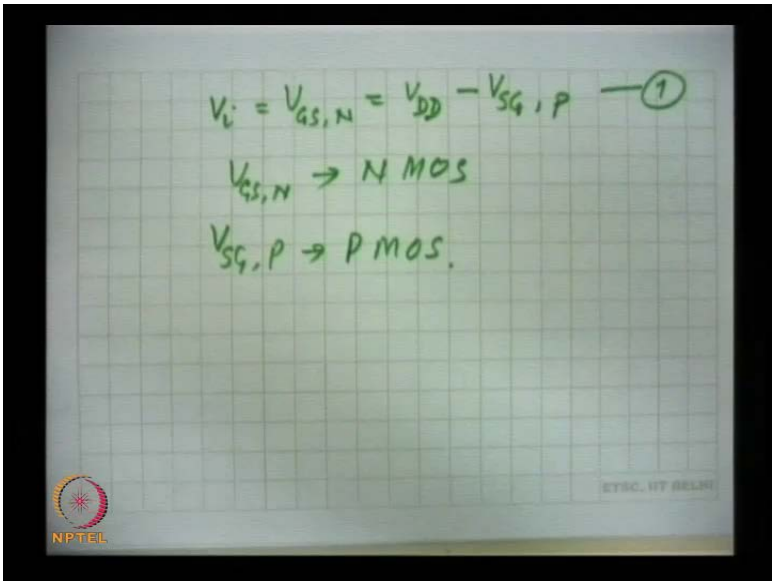

So, we will remember this circuit which is the circuit for a CMOS inverter and here some fundamental relations we have to realize and these relations are first, let me write and then I will explain V i is VGS, N and this is equal to VDD minus VSG, P this is equation number 1. This N subscript N here this is for NMOS in this subscript P here is for PMOS.

So, VGS, N this is the gate source voltage for the NMOS and VSG, P this is the voltage between source and gate for PMOS and then we can see here what we have written that GS, N what is the gate source voltage for the NMOS this is equal to VDD minus the voltage of VSG, P for the PMOS. We will continue this function of the CMOS inverter and then we will show that why the power consumption is least in this logic and that is

the reason that CMOS logic today is most advanced and very widely used logic.