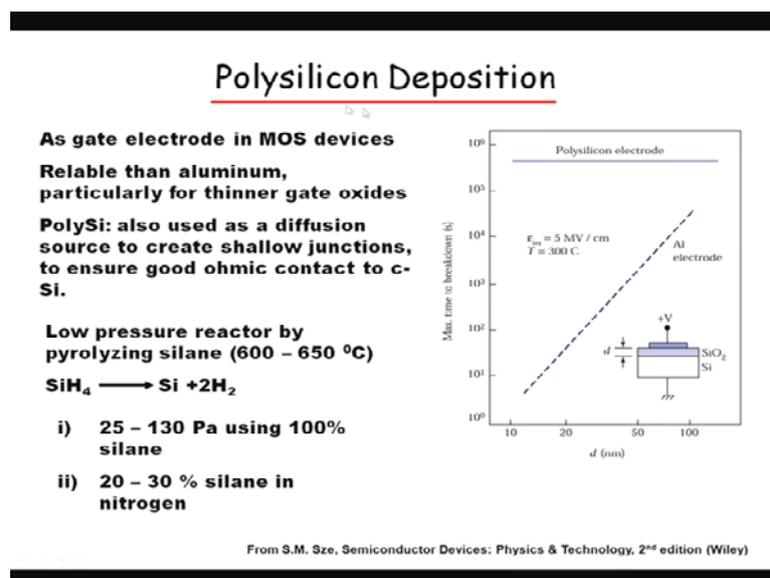


Processing of Semiconducting Materials
Prof. Pallab Banerji
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Indian Institute of Technology, Kharagpur

Lecture - 39
Metallization

Today's topic is Metallization, but one important thin films that is required for the device processing, as I mentioned earlier is the polysilicon deposition. So though it is a semiconductor, silicon is a semiconductor, but we shall find that, polysilicon is widely used for the P metallization layer or as for the gate electrode. And we can see that reliability has better, in case of the polysilicon compared to the normal aluminum films.

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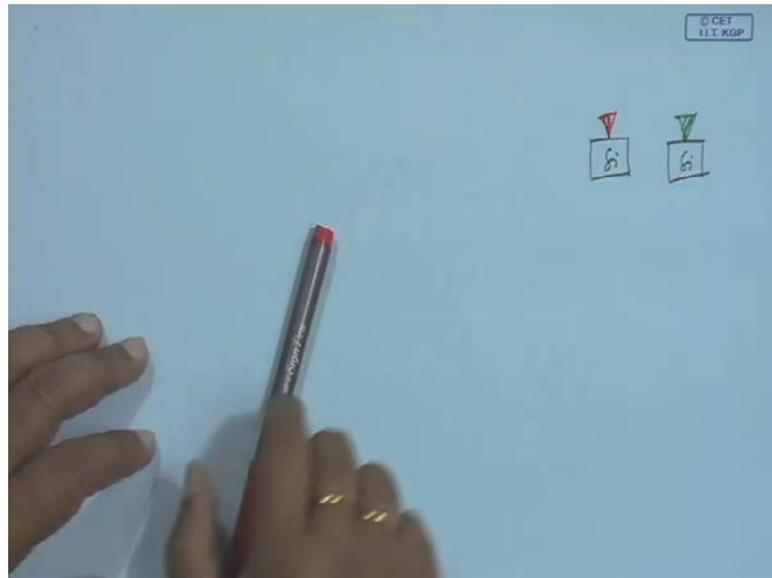


So, in this case you see that the polysilicon it is deposited on the device, but it is deposited as gate electrode in MOS devices, it is electrode. So normally, what we find that, in case of electrodes, the metals are used, but in this case the polysilicon is also used, because it has some distinct advantages over other kind of metals, particularly over aluminum.

If you see that this view graph, where we have seen the maximum time to breakdown versus the scaling of the device the dimension, we can see that polysilicon electrode is

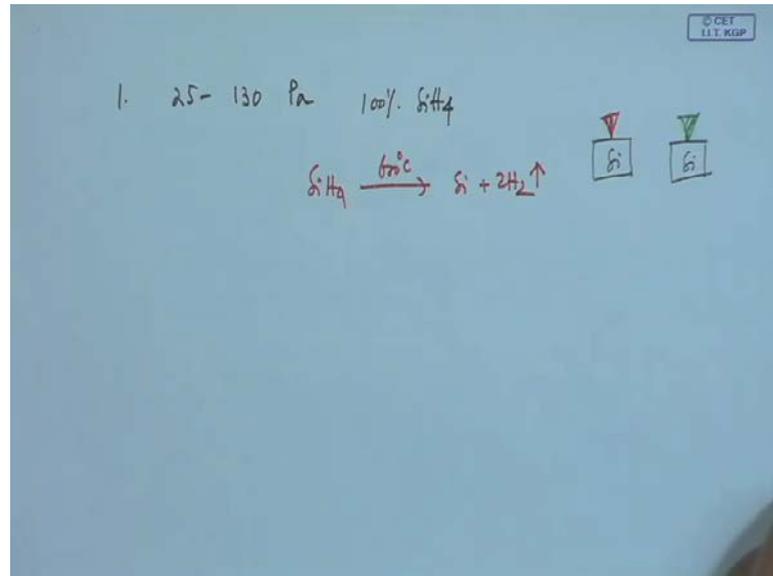
more reliable than the silicon than the aluminum electrode particularly, at the thin or gate oxides, say a 10 nanometer, 20 nanometer. We can find that the breakdown is very quick, for in case of the aluminum electrode, but for polysilicon, it is constant. So, it is more reliable, and this polysilicon is also used as diffusion source to create shallow junction, to create shallow junction to ensure good ohmic contact to crystalline silicon.

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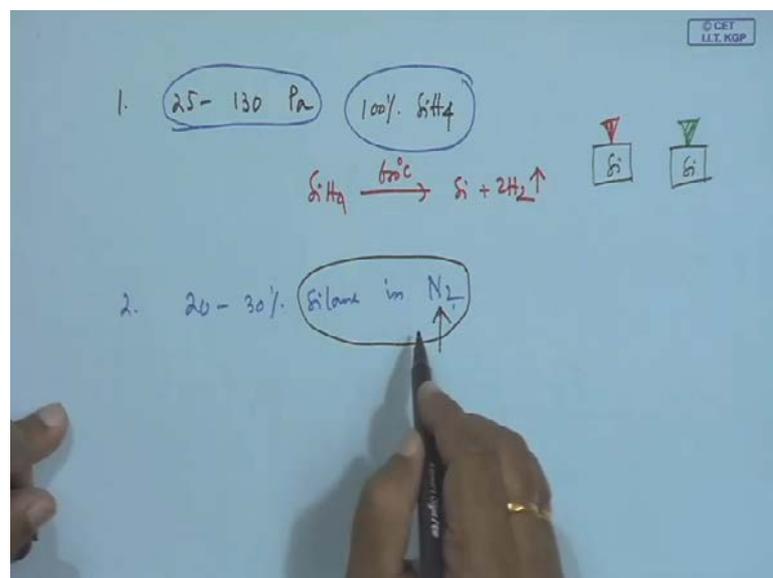
Because we see that normally what we do that? Let us take a silicon over which we deposit aluminum, say for metallization for contact, but if we can use a silicon over which we can use say polysilicon, then what will happen, then the contact will be further better. So, it ensures that good ohmic contact can be made, if we use a crystalline silicon over which we can make an electrode using polysilicon. Now, this polysilicon can be deposited by two processes: one is the low pressure reactor by pyrolyzing silane at 600 to 650 degree centigrade, and this is common for all the processes.

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In the first process, we can see that 25 to 130 pascal, and 100 percent silane is used, and 100 percent silane is used. So, it is basically the pyrolysis of silane let us, take Si H 4 you pyrolyze, it at around 600 degree centigrade, you will get polysilicon with the by-product as hydrogen. So, now this is done in a low pressure reactor, and you can use either 25 to 130 pascal 100 percent silane or you can dilute the silane.

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In case of dilution, what we do that generally, 20 to 30 percent silane in nitrogen, so it is diluted with nitrogen, and the same total pressure, total pressure of nitrogen and silane must be within this range of 25 to 130, so we can adopt two of the processes. One is using 100 percent silane, another is using dilution, where silane is diluted by the nitrogen the pressure used is 25 to 130 pascal. And in the second case where we dilute the silane in nitrogen 20 to 30 percent silane in nitrogen, total pressure of nitrogen silane, partial pressure of silane plus nitrogen must be within this range of 25 to 130 pascal.

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Polysilicon Deposition

As gate electrode in MOS devices
Reliable than aluminum,
particularly for thinner gate oxides

PolySi: also used as a diffusion source to create shallow junctions, to ensure good ohmic contact to c-Si.

Low pressure reactor by pyrolyzing silane (600 – 650 °C)

$\text{SiH}_4 \longrightarrow \text{Si} + 2\text{H}_2$

- i) 25 – 130 Pa using 100% silane**
- ii) 20 – 30 % silane in nitrogen**

Max. time to breakdown (s)

$E_{\text{max}} = 5 \text{ MV/cm}$
 $T = 300 \text{ C}$

Polysilicon electrode

Al electrode

+V

d (nm)

SiO₂

Si

From S.M. Sze, Semiconductor Devices: Physics & Technology, 2nd edition (Wiley)

So, this is the deposition techniques, and the chemistry associated with the polysilicon deposition.

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Polysilicon Deposition

Deposition temperature, dopants & heat cycle

600 – 650 °C: columnar structure: polycrystalline grains size 0.03 – 0.3 μm

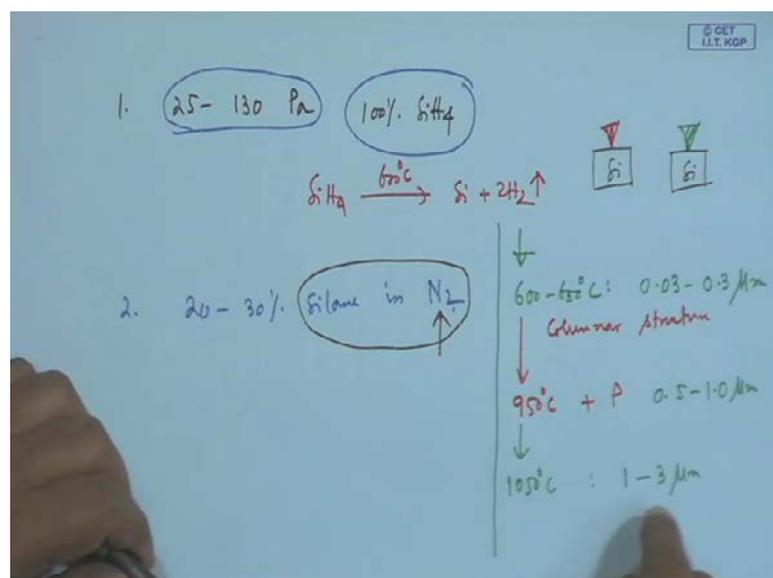
Phosphorus diffusion at 950 °C: structure changes to crystallite with grain size 0.5 – 1.0 μm

If temperature is increased to 1050 °C during oxidation, grain size increases to 1 – 3 μm

i.e. from amorphous to polycrystalline

Now, it depends on the rate, or the quality of the polysilicon deposition, it depends on the deposition temperature, dopants, and heat cycle. Now, if we use this 600 to 650 degree centigrade, we can see that a columnar structure is formed of polycrystalline silicon, the grains will be 0.03 to 0.3 micron.

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So, if we forward the steps at 600 to 650 degree centigrade, the grain size becomes 0.03 to 0.3 micron, this is the grain size, so it is the polycrystalline grains that is formed, and the columnar structure columnar structure. But if we increase the temperature, and at the same time phosphorus diffusion is done, so if phosphorus diffusion at 950 degree centigrade, then structure changes to crystallite with grain size 0.5 to 1 micron. So, what we find that, with the increase of temperature and phosphorus diffusion, the grain sizes increases from 0.03 to 0.5.

So, almost more than ten times increase in the grain size is obtained, if we use after this 600 650 to 950 degree centigrade with the diffusion of phosphorus, so the columnar structure will be converted to the crystallites, having the grain size in this case as 0.5 to 1 micron. Then, if temperature is further increased during oxidation, if temperature is further increased, so what will happen say to 950 degree centigrade to 1050 degree centigrade, the crystallite size or the grain size will increase to 1 to 3 micron.

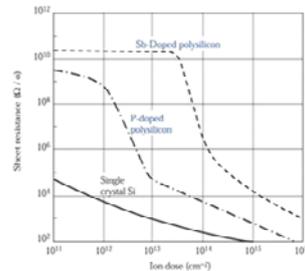
So, there will be a change from the amorphous, in this case 0.03 micron columnar structure to 1.3 micron polycrystalline structure, so that is the growth mechanism, in case of the polycrystalline silicon, it is a function of the temperature dopant and heat cycle. So, that means you and you can increase the temperature, you can use some dopant, and some heat cycle, you can use, so that from amorphous structure to the polycrystalline silicon is formed, in case of the polysilicon deposition.

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Polysilicon: Doping

Can be doped by diffusion, ion implantation or in situ

Carrier traps at the grain boundaries cause very high resistance in the lightly implanted PolySi. Resistance drops rapidly as the carrier traps become saturated with dopants (approaching that of implanted single c-Si)



Sheet resistance of a single c-Si and of 500 nm PolySi doped with Sb and P 30 keV.

From S.M. Sze, Semiconductor Devices: Physics & Technology, 2nd edition (Wiley)

Now, if you dope polysilicon using antimony or phosphorus, so what we see that the resistivity increases, because on the y axis, it is the sheet resistance, and in the x axis, it is ion dose, it must be mentioned that, polysilicon can be doped using diffusion ion implantation, or in situ doping using some kind of say phosphorus, or any kind of dopant say antimony or boron, etcetera.

But, we see that the resistivity increases for with doping, why it is increases? Because, the carrier traps at the grain boundaries, there is wide there is a grains, and this is a amorphous structures, at this temperature, or at this doping concentration, what will happen? that there will be carrier traps at the grain boundary, and they cause very high resistance for the lightly doped ion, that means 10 to the power 11, 10 to the power 12, 10 to the power 13, etcetera. But, if we increase the ion dose say from 10 to the power 14, 15, 16, so what will happen, that there will be saturation of the carrier traps, and the dopants will saturate the carrier traps, and then there will be a drop in the resistance.

There will be a drop in the resistance, in fact it is a rapid drop in the resistance around say 10 to the power 15 10 to the power 16 ion dose, so it will approach the resistance of the single crystalline silicon, at the higher ion doses. So, this is taken for a 500 nanometer polysilicon doped with antimony and phosphorus, at 30 k e V, so ion ion

energy was 30 keV. So, the mechanism we can explain on the basis of the carrier trap, at the grain boundaries at low ion dose, the carrier trap increases, high resistance, but as the ion dose increases, there will be saturation of the carrier traps, and the resistance drops rapidly approaching that of the single crystalline silicon.

(Refer Slide Time: 10:05)

Metallization

Physical Vapour Deposition

- **Thermal evaporation**
- **E-beam evaporation**
- **Plasma spray deposition**
- **Sputtering**

Metals & metal compounds:

Ti, Al, Cu, TiN, TaN

Now, after polysilicon deposition, we can consider the metallization of many metals or alloys generally, the metallization can be done by the physical vapour deposition, or by the chemical vapour deposition. Normally, in IC technology or in semiconductor processing, we will find that aluminum, the compounds of aluminum, titanium, nitride, tungsten, copper, those are used rigorously and widely for making a device. And in IC time delay we have seen that, the resistance of the metal contact must be very, very small. So, we shall find in our discussion, that apart from aluminum, copper is also used in some cases though, copper has certain drawbacks that we shall discuss later.

Now, so far as the physical vapour deposition is concerned, we can use the thermal evaporation, we can use the electron beam evaporation, we can use the sputtering, we can use the plasma spray, and there can be different types of sputtering using which, we can make different kinds of metal layers of metal thin films over the semiconductor structure, for ohmic contact for interconnection etcetera.

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Evaporation

A source material is heated above its melting point in an evacuated chamber.

Evaporated atoms travel at high velocity in straight-line trajectory.

Source is molten by resistance heating/rf heating/focused electron beam.

Thermal evaporation/e-beam evaporation is replaced by Sputtering for ULSI

Now, in the earlier stages physical vapour deposition particularly, the deposition using thermal evaporation and e-beam was widely used, for making the device, but in ultra large scale integration, those evaporation techniques were replaced by the sputtering. Now, what is evaporation? Evaporation is a source material which is heated above its melting point in an evacuated chamber, the source material means the metal which you want to deposit. Suppose, if we want to deposit aluminum, then our source material is aluminum, and let us take a evacuated chamber, that chamber must have the source along with the facility of heating the source material, and this evaporation heating it, it is basically the by the thermal means, or it can be by electron beam, evaporated atoms travel at high velocity in straight-line trajectories.

And source is molten by resistance heating, r f heating, or focused ion beam in normal thermal evaporation resistance heating is used, or in sputtering one can use the r f heating, or sometimes using a magnetic field. That we shall discuss, or if the melting point is very high, which is not, which is not possible to melt, the materials are not possible to melt by the resistance heating it is not possible in that case, the focused electron beam is used to melt the material.

So, the idea is that you have to use a source material, which you would like to deposit

and there will be a substrate, or a wafer placed on the line of the source with some distance, not very close, not very far away, and then you have to melt the source by some heating arrangements, depending on your system the evaporated atoms, then travel at high velocity in straight line trajectories.

However, as mentioned earlier the thermal evaporation or e-beam evaporation is replaced by sputtering for ultra large scale integration. Now, evaporation is very simple system, thermal evaporation, and aluminum at that evaporated chamber, though aluminum melting point is 600 say 60 degree centigrade, and it is evaporated at 300 degree centigrade, if we use an evacuated chamber. So aluminum is very very easily can be evaporated by the thermal evaporation system.

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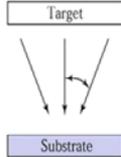
Sputtering

Ion beam sputtering: a source of ions is accelerated towards the target and impinged on its surface.

Sputtered material deposits on a wafer which is facing the target.

Ion current and energy can be independently adjusted.

Evacuated chamber: more target material is transferred to the wafer with less contamination



The diagram illustrates the ion beam sputtering process. It shows a rectangular box at the top labeled 'Target' and a rectangular box at the bottom labeled 'Substrate'. Three vertical arrows point downwards from the target towards the substrate. A curved arrow on the right side of the arrows indicates the direction of sputtered material being deposited onto the substrate.

But for very smooth surface, for uniform thickness, for low thin layer, or for say higher deposition rate, one can use the sputtering, this can be an ion beam sputtering, say a source of ions is accelerated towards the target and impinged on its surface. So, that is the target, target means the metal which you want to deposit, or the metal alloy which you want to deposit on the substrate, so there must be an ion source which will be accelerated towards the target, and impinged on its surface. So, suppose this is, this is the ion source it is coming towards the target now, when it comes towards the target and

impinges on it sputtered material will come out from the target, and deposits on a wafer which is facing the target.

Now, ion current and energy can be independently adjusted, how depending on your growth rate, or depending on the thickness, it must be an evacuated chamber, more target material is transferred to the wafer with less contamination, since we are using an evacuated chamber.

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(i) To increase the ion density and hence sputter deposition rate : use a third electrode that provides more electron for ionization.

(ii) Magnetron Sputtering: Use a magnetic field such as electron cyclotron resonance to capture and spiral electrons, increasing their ionization efficiency in the vicinity of the sputtering target.

Widely used for Al and its alloy: rate: 1 μ m/min

Now, how we can increase the ion density and hence, the sputter deposition rate, that can be done using a third electrode, that provides more electron for ionization, or we can use magnetron sputtering. In this case we use a magnetic field, such an electron cyclotron resonance to capture and spiral electrons, increasing their ionizing efficiency in the vicinity of the sputtering target, and it is widely used this magnetron sputtering for aluminum at its and its alloy deposition, with a rate of 1 micron per minute.

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Long-through Sputtering

Used to control the angular distribution.

In standard sputtering there are two primary reasons for a wide angular distribution of incident flux at the surface: Use of a small target to substrate separation and scattering of the flux by the working gas as the flux travels from the target to the substrate.

Small separation is needed to achieve good throughput, uniformity and film properties when there is substantial gas scattering.

Then, there can be long through sputtering, long through sputtering is used to control the angular distribution, it is used to control the angular distribution, because here you see that the angular distribution is very small, and in standard sputtering, there are two primary reasons for a wide angular distribution of incident flux at the surface. Use of a small target to substrate separation, and scattering of the flux by the working gas as the flux travels from the target to the substrate.

So, we see that here it is the distance is less as mentioned earlier, here the separation use of a small target to substrate separation, that means the distance between the target and the substrate is small, and there will be scattering of flux by the working gas as the flux travels from the target to the substrate.

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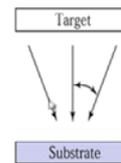
Sputtering

Ion beam sputtering: a source of ions is accelerated towards the target and impinged on its surface.

Sputtered material deposits on a wafer which is facing the target.

Ion current and energy can be independently adjusted.

Evacuated chamber: more target material is transferred to the wafer with less contamination



So, that means in this case say the distance is small between the target and the substrate, why that it is, it is related, because there will be scattering by the working gas, when the target molecules will or materials, will come towards the substrate, there will be scattering by the working gas; working gas say we can use say argon ion, or argon plasma, or nitrogen plasma, or hydrogen plasma, then there will be a scattering. So, the you cannot avoid the scattering in such a case, and because of the scattering the distance we cannot take very high, the distance must be very close between the substrate and the target.

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**Solution: Sputter at very low pressures
(less than 0.1 Pa)**

**Magnetron plasma can sustain under
more rarefied conditions.**

Gas scattering is less important.

**Target-to-substrate distance can be
greatly increased.**

**Angular distribution can be rigorously
narrowed allowing more deposition at
the bottom of high aspect features
such as contact holes.**



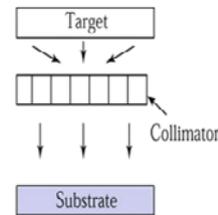
Now, small separation is needed to achieve good throughput, uniformity and film properties, when there is substantial gas scattering is there, so they are interconnected. Now, how to what is the solution? How we can increase the angular distribution? Sputter at very low pressure, that means less than 0.1 pascal, that is done and that is known as the long through sputtering here.

The magnetron plasma can sustain under more rarefied conditions 0.1 pascal is rarefied, and magnetron plasma can sustain in it, because now there are different kinds of systems the those have been designed, and available in the commercial application, or in the market. So, in that case one can, and make very low pressure, and at that case the it the magnetron plasma can also sustain. Then, the gas scattering is less important, because it is 0.1 pascal, so the target to substrate distance can be greatly increased, and if it is greatly increased, then the angular distribution can be greatly narrowed, allowing more deposition at the bottom of the high aspect, features such as contact holes.

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Contact holes with large aspect ratio are difficult to fill with material: scattering events cause the top opening of the hole to seal before appreciable material is deposited on its floor.

Solution: collimating the sputtered atoms by placing an array of collimating tubes just above the wafer to restrict the depositing flux to normal $\pm 5^\circ$. Atoms whose trajectory is more than 5° from normal are deposited on the inner surface of the collimators



Contact holes with large aspect ratio are difficult to fill with material, why because the scattering events, cause the top opening of the hole to seal before, appreciable material is deposited on its floor. Now, then what is the solution solution of such a case is that, we can use a collimator, collimating the sputtered atoms by placing an array of collimating tubes just above the wafer, to restrict the depositing flux to normal plus minus 5 degree within plus minus 5 degree to normal. That means more than 5 degree with the normal it can be made, so that the atoms whose trajectory is more than 5 degree from normal, are deposited on the inner surface of the collimators, and the rest will be deposited on the floor.

So, that is very important concept, so that means we can see that, we can use thermal evaporation for low melting point material, however at the same time we can use the high melting point material, or some compound using sputter targets, or within the sputtering. This sputtering can be through ion beam, it can be magnetron sputtering and at the same time, we can use the collimator for collimating the target materials, before reaching to the contact holes, or different areas of the device.

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CVD: metal film deposition

Coatings are conformal, good step coverage, large number of wafers at a time (high throughput)

Refractory metal deposition

Tungsten's low electrical resistivity (5.3 $\mu\Omega$ -cm) and its refractory nature: desirable in IC fabrication.

Tungsten is used both as a contact plug and as first level metal.

Now, apart from this physical vapour deposition, we can use CVD also chemical vapour deposition of the metal films, and we can see that the coatings in those cases are conformal, good step coverage is obtained, large number of wafers at a time can be handled, that means the high throughput, we can coat large number of wafers at a time. This CVD is particularly, useful for refractory metal deposition, refractory metal deposition, say tungsten is a refractory metal. So, we can use tungsten deposition using CVD, and tungsten's low electrical resistivity, it is very small 5.3 micro ohm centimeter, and its refractory nature makes it a very desirable candidate in IC fabrication. And tungsten is used both both as contact plug, and as first level metal.

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CVD-W

(i) Hydrogen reduction

(ii) Silicon reduction

(iii) Silane reduction

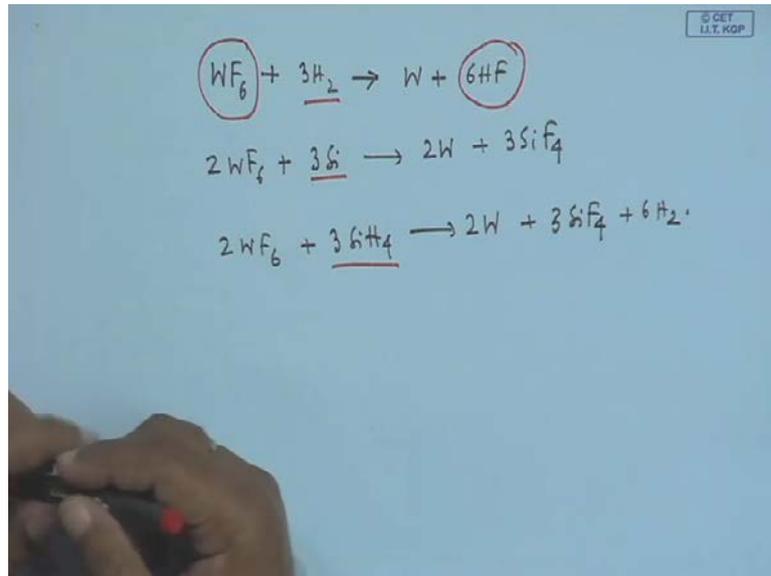
Silicon reduction: provides a nucleation layer of W on Si but not on SiO₂.

Hydrogen reduction can deposit W rapidly on the nucleation layer, forming the plug: excellent conformal coverage.

Less selectivity. HF as by-product: encroachment of the oxide, rough surface of deposited W films.

Now, this tungsten can be done deposited by the CVD method, there are three different techniques using, which one can make the tungsten deposition using CVD: one is known as the hydrogen reduction, second one is known as the silicon reduction, and third one is the silane reduction. Now, these three reductions reaction or the chemistry involved in this, we can write in this manner, say tungsten fluoride is the source material and why tungsten fluoride is used? Because, it is liquid at room temperature and a normal room temperature, it is it boils at normal room temperature, so very easily one can use the, the vapour pressure on the top of the tungsten fluoride cylinders or the bottles.

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Then, WF_6 when reacts with hydrogen that is the hydrogen reduction reaction, one can get tungsten with the hydrogen fluoride, this is very important by-product in this reaction, that means, so far as the hydrogen reduction reaction is concerned. Apart from tungsten, we can have hydrogen fluoride as well then, there can be silicon reduction in this case, the tungsten fluoride reacts with silicon to obtain tungsten, with SiF_4 , so no HF is obtained, and for silane reduction SiH_4 that is the silane, we can add tungsten with that silicon fluoride and hydrogen. So, we see that hydrogen hydrogen reduction, silicon reduction, and silane reduction reaction with tungsten fluoride, deposit tungsten metal layer by CVD.

(Refer Slide Time: 22:03)

CVD-W

(i) Hydrogen reduction

(ii) Silicon reduction

(iii) Silane reduction

Silicon reduction: provides a nucleation layer of W on Si but not on SiO₂.

Hydrogen reduction can deposit W rapidly on the nucleation layer, forming the plug: excellent conformal coverage.

Less selectivity. HF as by-product: encroachment of the oxide, rough surface of deposited W films.

Now, silicon reduction provides say nucleation layer of tungsten on silicon, but not on Si O₂, and hydrogen reduction can deposit tungsten, rapidly on the nucleation layer forming the plug excellent conformal coverage, but the problem is it is less selective, its selectivity is very less at the same time, the by-product is hydrogen fluoride which has the property of encroaching to the oxide. And it makes because of this hydrogen fluoride it makes rough surface of deposited tungsten films, so hydrogen reduction has some drawback, because it etches out oxide encroachment of oxide.

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Silane reduction: high deposition rate, much smaller W grain size. HF penetration or rough surface problem is eliminated (no HF by product).

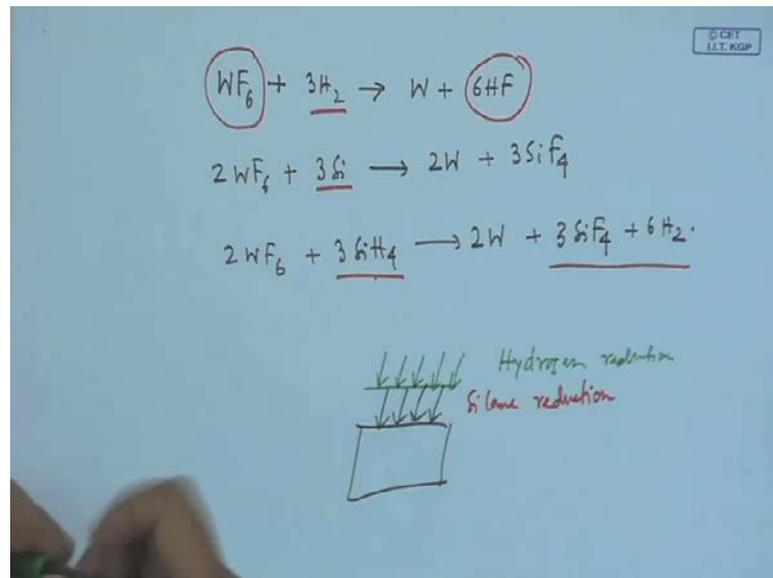
Generally, a silane reduction process is used as the first step in blanket W deposition to serve as a nucleation layer and to reduce junction damage.

After silane reduction, hydrogen reduction is used to grow blanket W layer.

b

Then, what is the solution? Solution is that for silane reduction we can make silane reduction. We can see that using silane reduction, there is no hydrofluoric penetration or rough surface problem is eliminated, because no HF as the by-product. So, it has high deposition rate, much smaller tungsten grain size, and since hydrogen fluoride by-product is not there, so there will be no penetration of hydrogen fluoride towards the oxide layers, or rough surface problem is eliminated. So, generally a silane reduction process is used as the first step in blanket tungsten deposition, to serve as a nucleation layer and to reduce junction damage, then you use silane reduction reaction after silane reduction reaction you use hydrogen reduction to grow blanket W layer.

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So, that means let us take a silicon on which, first silane reduction reaction takes place, this is silane reduction reaction, so blanket tungsten will be formed without any damage etcetera. Because, there is no hydrogen fluoride, then above once the nucleation layer is grown, then at the top of this tungsten layer, you can make some layer of tungsten using the hydrogen reduction reaction or...

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CVD: TiN

Widely used as diffusion barrier-metal layer in metallization. Also deposited by sputtering.

CVD grown TiN can provide better step coverage than PVD grown TiN in deep submicron technology.

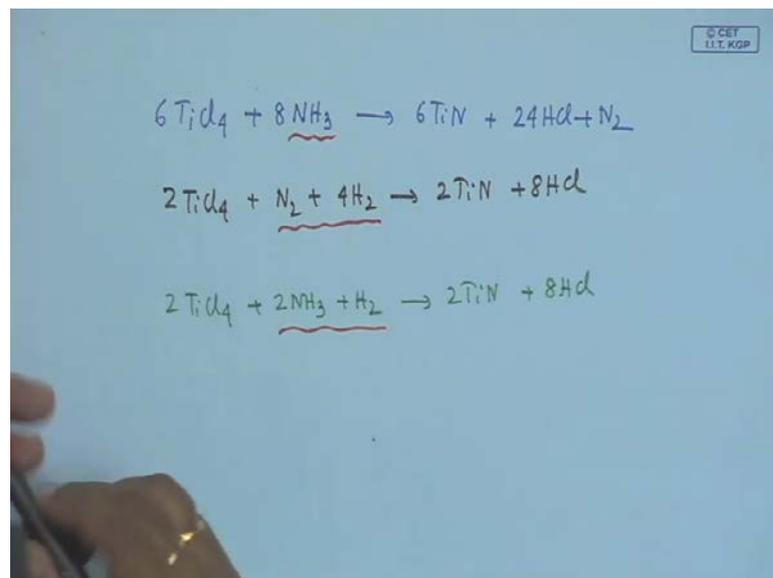
TiCl₄ with NH₃, H₂/N₂ or NH₃/H₂ is used.

Deposition temperature: 400 – 700 °C for NH₃ reduction and is higher than 700 °C for N₂/H₂ reaction.

The higher the deposition temperature, better the TiN film and less Cl incorporation (~5%).

Apart from the tungsten, titanium nitride is also used, because titanium nitride is widely used as diffusion barrier metal layer in metallization, it is also deposited by sputtering, that means by PVD physical vapour deposition, and this CVD grown titanium nitride can provide better step coverage than PVD grown titanium nitride in deep submicron technology, because it is well known fact that, so far as the step coverage or the conformal is deposition is concerned, one has to use the CVD not the PVD. Then this titanium nitride CVD can be made, or the titanium nitride films can be deposited, using CVD using titanium chloride $TiCl_4$ with different kind of reaction, in one case, one case use the ammonia, in one case, one can use the hydrogen, nitrogen, or ammonia, and hydrogen.

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So, the reaction or the chemistry involved for the deposition of titanium nitride is like, this say let us take, $TiCl_4$ the source material which when reacts with the ammonia, it will give titanium nitride, apart from the by-product of hydrogen chloride, and nitrogen. So, this is one reaction one, when this titanium Cl_4 is used to it ammonia. Then, there can be another reaction as mentioned earlier, say $2TiCl_4$ plus N_2 plus $4H_2$, and in this case $2TiN$ will be deposited with hydrogen chloride, and in this case we have not used NH_3 rather, we have used a mixture of nitrogen and hydrogen gas. And the third one using $2TiCl_4$ and in this case, it is made to react with NH_3 and hydrogen, to

obtain TiN plus hydrogen chloride. So, in this case we use the ammonia and hydrogen for the reaction.

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CVD: TiN

Widely used as diffusion barrier-metal layer in metallization. Also deposited by sputtering.

CVD grown TiN can provide better step coverage than PVD grown TiN in deep submicron technology.

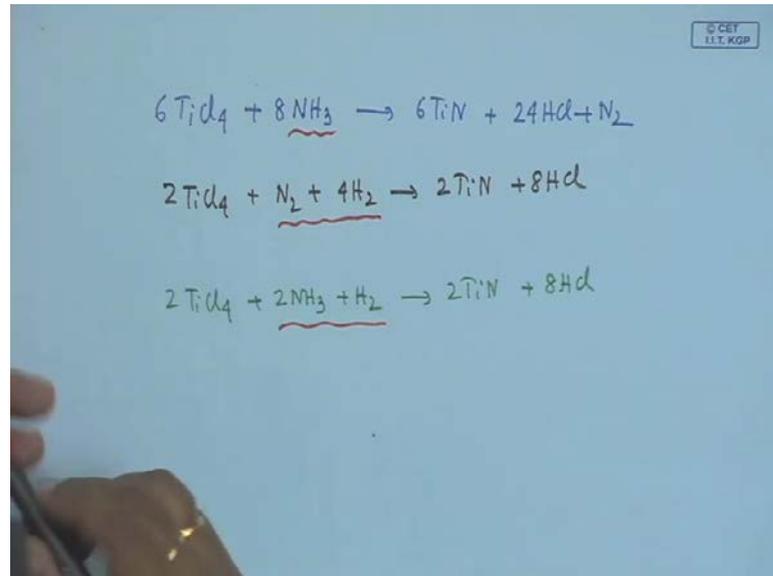
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Deposition temperature: 400 – 700 °C for NH₃ reduction and is higher than 700 °C for N₂/H₂ reaction.

The higher the deposition temperature, better the TiN film and less Cl incorporation (~5%).

Then, the deposition temperature is 400 to 700 degree centigrade for or NH₃ reduction, and is higher than 700 degree centigrade, at for N₂/H₂ reaction. So, obviously the higher the deposition temperature better the titanium nitride film, and less chlorine incorporation will be there.

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Because the product is hydrogen chloride and also we are using the TiCl_4 , so the chlorine will be incorporated in the TiN film, and it can be 5 percent, but as the deposition temperature will be higher, so the incorporation will be less.

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Aluminum Metallization

Al & its alloys: low resistivity

Deposited by PVD or CVD

Al: $2.7 \mu\Omega\text{-cm}$; Alloys: upto $3.5 \mu\Omega\text{-cm}$

Low-resistance, adheres well to SiO_2

Problems: Electromigration and Spiking

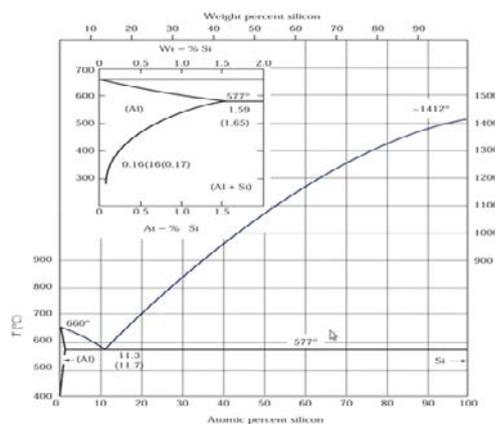
Then, it is the aluminum metallization, in aluminum metallization is very very important

in the sense, that it has very low resistive, say 2.7 micro ohm per centimeter, and its alloy has the resistivity of 3.5 micro ohm centimeter, and it its melting point is low. So, by PVD that means by thermal evaporation, one can make the aluminum metallization on substrates, and it has, it as it it adheres will to S i O 2, however it has the problem of electromigration, and spiking that we shall discuss in detail.

So, so far as the aluminum metallization is concerned, we see that aluminum has certain advantages, one advantage is adheres well to with S i O 2, next thing is that it has very low resistivity 2.7 micro ohm centimeter. Even, if we use the aluminum compound then also the resistivity is 3.5 micro ohm per centimeter, and it has very low temperature, so in the lab scale one can make, aluminum deposition using a normal thermal evaporation system.

However, it has the problem of electromigration and spiking, that we shall see and that has the direct bearing on the reliability, or the functioning of the device. Because the aluminum spiking can make the junction, if a junction is shallow, then it can short circuit, or in case of electromigration we shall find that, there can be open circuit or short circuit depending on the spile of the aluminum atoms, that means the because of the transport of the masses.

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Phase diagram of Al-Si system at 1 atm.

From S.M. Sze, Semiconductor Devices: Physics & Technology, 2nd edition (Wiley)

It is the phase diagram of aluminum silicon system at one atmosphere, and here we see that, this has some eutectic.

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Al-Si system shows eutectic characteristics: addition of either component lowers the system's melting point below that of either metal.

Minimum melting point (eutectic temperature): 577 °C corresponding to 11.3% Si + 88.7%Al.

Melting point: Si: 660 °C; Al: 1412 °C.

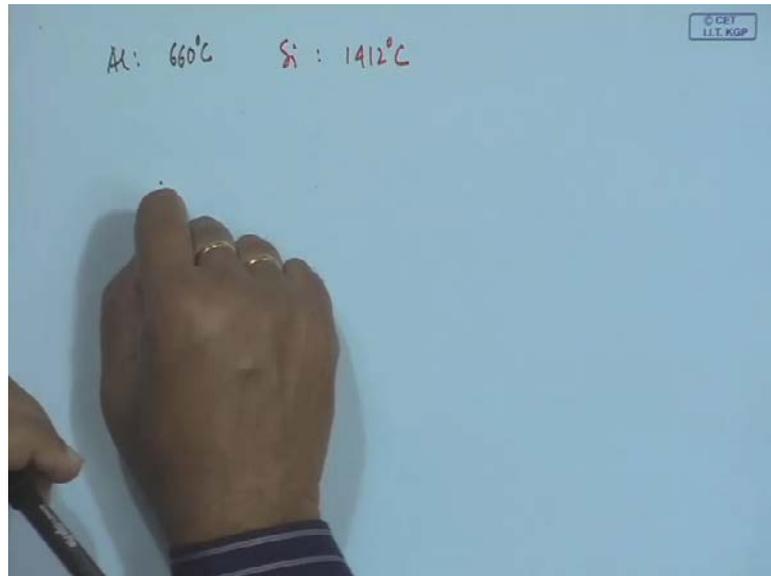
Inset Figure: Solid solubility of Si in aluminum:

0.25 wt% at 400 °C, 0.5 wt% at 450 °C and 0.8 wt% at 500 °C.

Whenever Al contacts Si, Si will dissolve into Al during annealing. The amount of Si dissolved will depend on (i) solubility at then annealing temperature and (ii) volume of Al to be saturated with Si.

Now, what is eutectic? aluminum silicon system shows eutectic characteristics, the eutectic means addition of either component lowers the systems melting point below that of either metal.

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Suppose, we have in this case aluminum whose melting point is 660 degree centigrade, and we have silicon whose melting point is 1, and silicon whose melting point is 1412 degree centigrade. However, from the phase diagram we can see that, there is an eutectic temperature using which it can melt below 660 degree centigrade.

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Al-Si system shows eutectic characteristics: addition of either component lowers the system's melting point below that of either metal.

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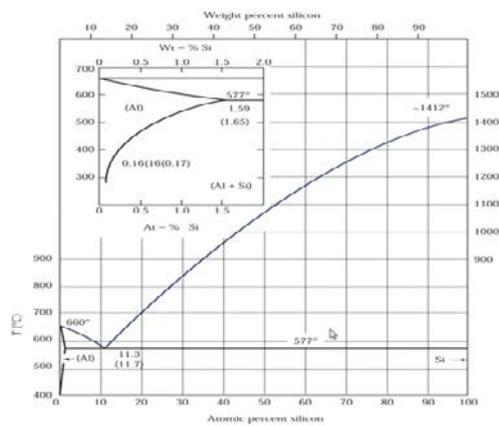
0.25 wt% at 400 °C, 0.5 wt% at 450 °C and 0.8 wt% at 500 °C.

Whenever Al contacts Si, Si will dissolve into Al during annealing. The amount of Si dissolved will depend on (i) solubility at then annealing temperature and (ii) volume of Al to be saturated with Si.

And this eutectic in this case we can see that, it is 577 degree centigrade, this is the 577 degree centigrade, and at this temperature we can see that 11.3 percent silicon, and 88.7 percent aluminum, 88.7 percent aluminum. Because it is the silicon percentage, so 11.3 atomic percent of silicon means the rest is the aluminum, which is 88.7 percent aluminum, or if you can weight percent, it is 11.7, so it will be 88.3.

So, eutectic temperature means the addition of either component lowers the systems melting point below that of either metal, either metal means silicon, it is 660 silicon is 1412 and aluminum is 660, so even it is less than 660 which is 577 in this case. Now, in the inset it is the solid solubility of silicon in aluminum, and from this curve we can see that with 0.25 weight percent, the solid solubility is 0.25 weight percent at 400 degree centigrade, 400 degree centigrade is 0.25 percent, then 450.5 percent and it is 0.5 percent, and then at 500 it is 0.8 percent.

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Phase diagram of Al-Si system at 1 atm.

From S.M. Sze, Semiconductor Devices: Physics & Technology, 2nd edition (Wiley)

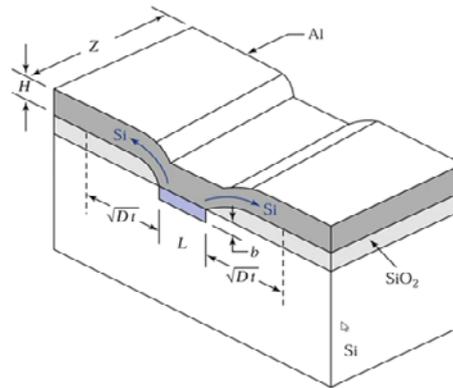
So, the solubility of silicon in aluminum has this kind of a value, which is evident from the inset curve of the phase diagram. So, from this two diagram what we see, one thing we see that silicon aluminum system has a eutectic which is 577 degree centigrade, and so it is important that for any processing, the temperature must be limited to 577 centigrade, if you want to deposit aluminum on silicon. And at the same time from the

inset of the figure, we can see that the solid solubility curve, and the solubility of aluminum in silicon, or the or the solubility of silicon in aluminum has different values, like 0.25 weight percent 0.5 weight percent 0.8 weight percent at different temperatures.

Now, whenever aluminum contact silicon, silicon will dissolve into aluminum during annealing, and the amount of silicon dissolved will depend on the solubility at the annealing temperature, and volume of aluminum to be saturated with silicon. So, these are the two factors on which the amount of silicon dissolved in aluminum will depend.

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Diffusion of silicon in aluminum metallization



From S.M. Sze, Semiconductor Devices: Physics & Technology, 2nd edition (Wiley)

Here, we see that this is the diffusion of silicon and aluminum, we have used a aluminum metal line and in contact with the, with with contact with an area Z into L , L is the length of the metal line, and ZL of ZZL is the area, and after annealing time t the silicon will diffuse a distance \sqrt{Dt} on both the sides along the aluminum line, from the edges of the contact, and D being the diffusion constant and of silicon.

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Al: 660°C Si: 1412°C

$D = 4 \times 10^{-2} \exp\left(-\frac{0.92}{KT}\right)$
for Si diffusion in deposited Al films.

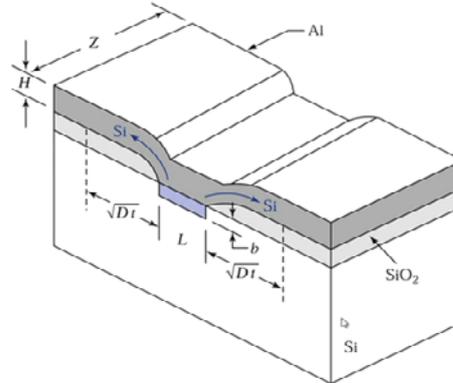
Volume of Si consumed
 $V \approx 2\sqrt{Dt} \cdot (HZ) \cdot S \cdot \left(\frac{\rho_{Al}}{\rho_{Si}}\right)$

Depth to which Si is consumed
 $b \approx 2\sqrt{Dt} \cdot \left(\frac{HZ}{A}\right) \cdot S \cdot \left(\frac{\rho_{Al}}{\rho_{Si}}\right)$

Now, what is the value of this diffusion constant D equals to 4×10^{-2} to the power minus 2 exponential minus 0.92 by KT , for silicon diffusion in deposited aluminum films, and if we assume that that this length of aluminum is completely saturated with silicon, if we assume then the volume of silicon consumed, it will be say V equals to $2\sqrt{Dt}$ multiplied by H into Z , H is this thickness, Z is this dimension. So, HZ is the area multiplied by the solubility of silicon in aluminum, S is the solubility of silicon in aluminum, and then the ratio of the density of aluminum to the density of silicon, so that is the volume of silicon consumed.

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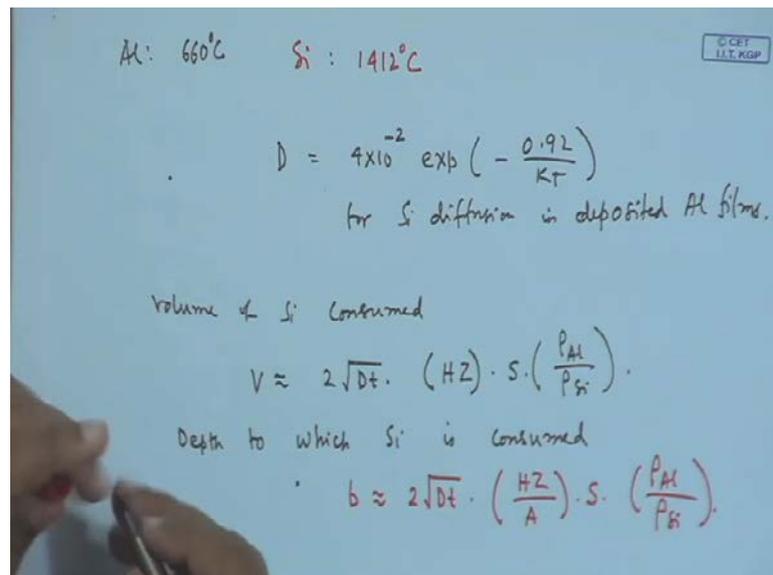
Diffusion of silicon in aluminum metallization



From S.M. Sze, Semiconductor Devices: Physics & Technology, 2nd edition (Wiley)

Now, if we if the consumption takes place uniformly, let us consider that the consumption of silicon will takes place uniformly over the contact area A , where A is Z into L , this is the contact area $L A$ equals to Z into L .

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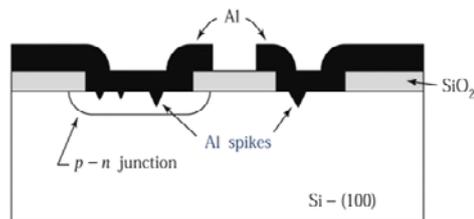
Then, the depth to which depth to which silicon is consumed will be say, b equals to in

this case say let us write down the the depth, b it is equals to $2 \sqrt{D t}$ multiplied by $H Z$ by A into S into ρ_{Al} by ρ_{Si} . Why because, we have considered that in this case the consumption takes place uniformly over the contact area A , over the contact area A which is Z into L , because this is the L and Z is this dimension, so Z into L , so this b value is very important that this is the depth to which silicon is consumed, but this is not uniform.

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In practical situation, the dissolution of Si does not take place uniformly but rather at only a few points. The effective area is less than the actual contact area thus b is much larger.

Actual situation in p-n junction area of Al penetrating Si at only few points where the SPIKES are formed.



From S.M. Sze, Semiconductor Devices: Physics & Technology, 2nd edition (Wiley)

In practical situation, the dissolution of silicon does not takes place uniformly, but rather at only a few points, so the effective area is less than the actual contact area, thus b is much larger, that means the effective area is less.

(Refer Slide Time: 36:56)

Al: 660°C Si: 1412°C

$D = 4 \times 10^{-2} \exp\left(-\frac{0.92}{KT}\right)$
for Si diffusion in deposited Al films.

Volume of Si consumed
 $V \approx 2\sqrt{Dt} \cdot (HZ) \cdot S \cdot \left(\frac{P_{Al}}{P_{Si}}\right)$

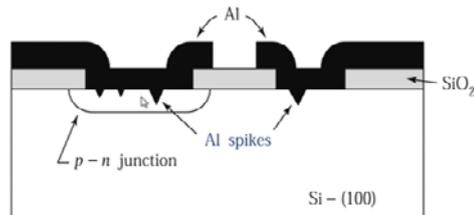
Depth to which Si is consumed
 $b \approx 2\sqrt{Dt} \cdot \left(\frac{HZ}{A}\right) \cdot S \cdot \left(\frac{P_{Al}}{P_{Si}}\right)$

Because it is not uniformly consumed had it been in uniform way, so A has certain dimension however, if this is not uniform, then a will be less, and so if A is in the denominator, if it is in if it is less then b will be higher. So, that means the b is much larger, this is the b that means the depth to which the silicon is consumed, and in actual situation in a p-n junction area of aluminum penetrating silicon at only few points, then that is the spikes so, we can see that many spikes are formed in the silicon.

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Actual situation in p-n junction area of Al penetrating Si at only few points where the SPIKES are formed.



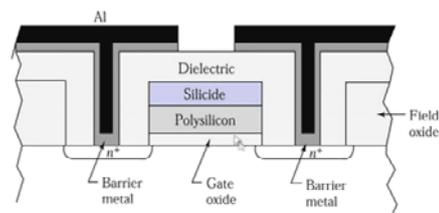
From S.M. Sze, Semiconductor Devices: Physics & Technology, 2nd edition (Wiley)

So, this is SiO_2 , this is aluminum, so since the silicon is dissolved in the aluminum, and so there will be spiking of the aluminum, because the silicon has consumed, so that is the spikes. Now, if the depth of the spike is such that, it is greater than the shallow junction, if there is a shallow junction, and the depth is comparable to that or even larger than that then, there will be obviously the short circuit.

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How to minimize Al spiking

- 1. To add Si to Al by coevaporation until the amount of Si contained by the alloy satisfies the solubility requirement.**
- 2. To introduce a barrier metal layer between Al and Si substrate.**



From S.M. Sze, Semiconductor Devices: Physics & Technology, 2nd edition (Wiley)

Now, one example we can give with this that, how to minimize the aluminum spiking? how to minimize the aluminum spiking? This spiking that we have shown earlier, how to minimize this, there are two ways using which, one can minimize the spiking. One is to add silicon to aluminum by co-evaporation until, the amount of silicon contained by the alloy satisfies the solubility requirement, so that means you put additional silicon and then using co-evaporation you deposit aluminum, so that it satisfies the solubility requirement, or you can use some barrier metal layer between aluminum and silicon. And generally, titanium nitrate, tantalum nitrate those metals are used, so one can use the barrier metal layer between aluminum and silicon substrate.

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Barrier Metal Layer

Low contact resistance with Si.

Will not react with Al.

Deposition & formation are compatible with existing process technology.

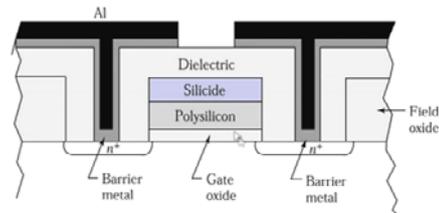
TiN : Titanium Nitride: stable for contact annealing temperature upto 550 °C for 30 min.

Now, so far as the barrier metal layers are concerned, it has it must have certain properties, it must have low contact resistance with silicon, it will not react with aluminum, and the deposition and formation are compatible with existing process technology. And with all such properties titanium nitride is found to be a stable one for contact annealing temperature upto 550 degree centigrade for 30 minute, that means if after metallization, with aluminum and silicon you anneal at 550 degree centigrade for 30, so titanium nitride will be will remain stable. But above 550 degree centigrade or for longer duration than 30 minute, it is not stable.

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How to minimize Al spiking

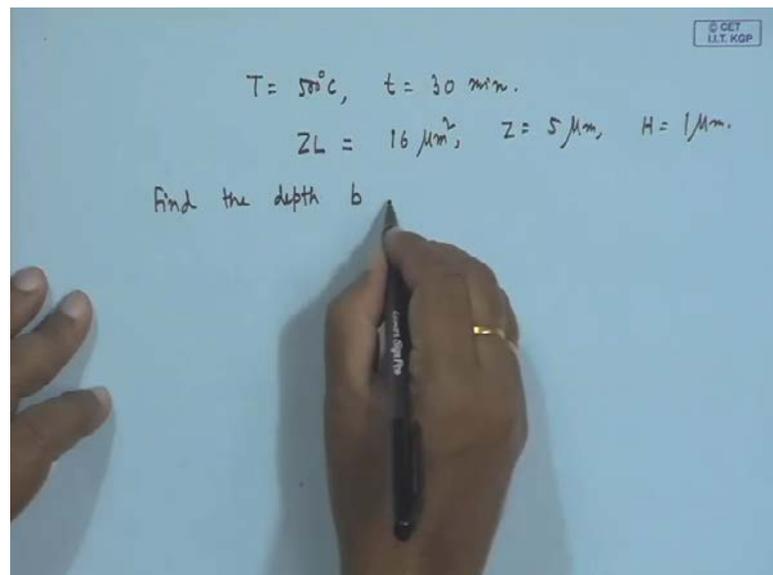
- 1. To add Si to Al by coevaporation until the amount of Si contained by the alloy satisfies the solubility requirement.**
- 2. To introduce a barrier metal layer between Al and Si substrate.**



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So, in this case the barrier metal can be titanium nitride, in certain cases we have seen that tantalum nitride is also used, so those are basically the refractory compound, refractory metal compound.

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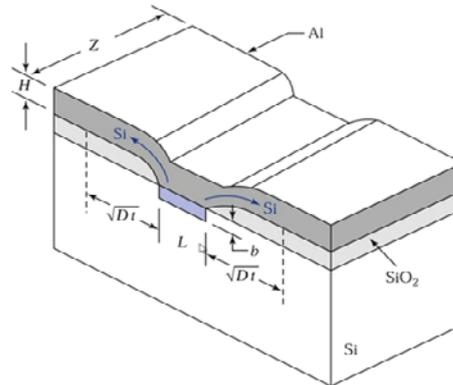


Now, with this b value let us take one example, that suppose T is 500 degree centigrade T

is 500 degree centigrade, and the small t that means time is 30 minute, Z L is given by 16 micrometer square with z equals to 5 micrometer, and H is equals to 1 micrometer.

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Diffusion of silicon in aluminum metallization



From S.M. Sze, Semiconductor Devices: Physics & Technology, 2nd edition (Wiley)

Find the depth b assuming uniform diffusion now, with this figure we can see that with this figure the values are L is Z L is given Z into L it is 16 micrometer square, Z Z is 5 micrometer square, and H is 1 micrometer square, then we have to calculate the thickness of b .

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$T = 500^{\circ}\text{C}$, $t = 30 \text{ min.}$
 $Z_L = 16 \mu\text{m}^2$, $Z = 5 \mu\text{m}$, $H = 1 \mu\text{m}$.
 Find the depth b

$D = 2 \times 10^{-8} \text{ cm}^2/\text{s}$ at 500°C
 Si in Al

$$b \approx 2\sqrt{Dt} \times \left(\frac{HZ}{A}\right) \times S \times \left(\frac{\rho_{\text{Al}}}{\rho_{\text{Si}}}\right)$$

$$= 2 \times 60 \times \left(\frac{1 \times 5}{16}\right) \times 0.8\% \times \left(\frac{2.77}{2.33}\right)$$

$$= 0.35 \mu\text{m.}$$

Al will fill a depth of $b = 0.35 \mu\text{m}$ from which Si is consumed.

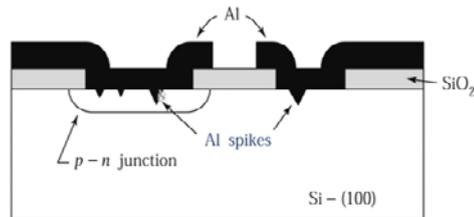
Now, we know that b is equals to $2 \sqrt{Dt}$, so that is equals to 2 into \sqrt{Dt} , \sqrt{Dt} is 60 how we can obtain, the value of D is equals to 2 into 10 to the power minus 8 centimeter square per second at 500 degree centigrade. Because the diffusion, it is the diffusion of silicon in aluminum, it is a diffusion of silicon in aluminum, and it is a temperature activated process, so at 500 degree centigrade is 2 into 10 to the power minus 8 , and small t is given as 30 minute, so if we convert and then multiply, it will come to 60 micron, that will be come to 60 micron.

Then, there will be H into Z , H into Z , H is 1 into Z is 5 by in this case there will be an area A , the area is 16 micrometer square that is the area 16 micrometers square into S , that is it is HZ by A , A is 16 , S is the solubility, that is we have to use the value of the solubility which is say 0.8 percent, this is 0.8 percent at this temperature of 500 degree centigrade, and it is 0.8 weight percent multiplied by the ratio of the density of aluminum to the silicon, which is 2.77 by 2.33 of silicon. Now, if we calculate this value, it comes to 0.35 micron, it comes to 3 . micron that means what is the implication of this value, that means aluminum will fill a depth of b equals to 0.35 micron from which silicon is consumed.

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In practical situation, the dissolution of Si does not take place uniformly but rather at only a few points. The effective area is less than the actual contact area thus b is much larger.

Actual situation in p-n junction area of Al penetrating Si at only few points where the SPIKES are formed.



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So, that means this spike in this particular problem, the spike depth to which it will go up to 0.35 micron, and if the shallow junction, remains within this dimension, so obviously there will be short circuit as the as had been discussed earlier.

(Refer Slide Time: 47:41)

Electromigration

For smaller devices (scaled down) current density become very high. High current densities can cause device failure due to electromigration.

It is the transport of mass (atoms) in metals under the influence of current. It occurs by transfer of momentum from the electrons to the positive metal ions. When a high current passes through thin metal conductors in ICs, metal ions in some regions will pile up and voids will form in other regions. The pile up can short circuit adjacent conductors whereas the voids can result in an open circuit.

Another problem associated with a aluminum is the problem of electromigration, it is the

problem of electromigration for smaller device say, because of the scaling down of the nano structure devices, current density become high, why current density become high? Because, the current density is divided by the area, as the area decreases, so current density, current density is the current divided by the area.

(Refer Slide Time: 48:15)

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$$T = 500^{\circ}\text{C}, \quad t = 30 \text{ min.}$$

$$ZL = 16 \mu\text{m}^2, \quad Z = 5 \mu\text{m}, \quad H = 1 \mu\text{m.}$$

Find the depth b

$$D = \frac{-8 \text{ V/s}}{2 \times 10^{-8} \text{ cm}^2/\text{s}} \text{ at } 500^{\circ}\text{C}$$

$$J = \frac{I}{A}$$

$$b \approx 2\sqrt{Dt} \times \left(\frac{HZ}{A}\right) \times S \times \left(\frac{P_{Al}}{P_{Si}}\right)$$

$$= 2 \times 60 \times \left(\frac{1 \times 5}{16}\right) \times 0.8\% \times \left(\frac{2.77}{2.33}\right)$$

$$= 0.35 \mu\text{m.}$$

Al will fill a depth of $b = 0.35 \mu\text{m}$ from which Si is consumed.

So, J equals to I by A , and if A becomes less the current density becomes very high, and with this high current density, with this high current density can cause device failure due to electromigration.

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Electromigration

For smaller devices (scaled down) current density become very high. High current densities can cause device failure due to electromigration.

It is the transport of mass (atoms) in metals under the influence of current. It occurs by transfer of momentum from the electrons to the positive metal ions. When a high current passes through thin metal conductors in ICs, metal ions in some regions will pile up and voids will form in other regions. The pile up can short circuit adjacent conductors whereas the voids can result in an open circuit.

Now, what is electromigration; electromigration is the transport of mass or atoms in metals under the influence of current, so if high current density is there, so there is a possibility that the atoms will, there will be a transport of the atoms, or there will be mass transport, it occurs by transfer of momentum from the electrons to the positive metal ions. So, the electrons are gaining the momentum, and they transfer the momentum from the high field to the positive metal ions.

When a high current passes through the thin metal conductors, in i integrated circuits metal ions in some regions will pile up, and voids will form in other region, so that means the uniform metal conductor will not remain as uniform, in some of the from the from some of the places, the metal ions will be removed due to the high current, and so the void will be formed in such places, and where the metal ions will be accumulated. Then, there will be a pile up the pile up can short circuit adjacent conductors whereas, the voids can result in an open circuit, so with this concept the problem of electromigration is very important, and it is found in case of aluminum.

(Refer Slide Time: 49:58)

Mean time of failure (MTF)

$$MTF \sim \frac{1}{J^2} \exp\left(\frac{E_a}{kT}\right)$$

Experimental $E_a = 0.5$ eV for deposited Al.

Low temperature grain-boundary diffusion is the primary reason for material transport.

How to increase the electromigration resistance of aluminum conductors:

Alloying with Cu (Al with 0.5% Cu)

Encapsulating the conductor in a dielectric

Incorporating oxygen during film deposition.

Now, Mean time of failure which is known as the MTF, that mean time of failure is related to the activation energy, as well as the current density, so obviously if the current density is very very less, then mean time failure will be very very high. But, if current density is very high, then mean time failure will be very very small, so that means within a few second or within a few minute, there will be a failure. Now, the activation energy which has been experimental, determined as 0.5 electron volt, and for deposited aluminum and from this value, one can consider that, the low temperature grain boundary diffusion is the primary reason for material transport.

Now, how to increase the electromigration resistance of aluminum conductors? there are certain process using which, one can and increase the electromigration resistance, one is the alloying with copper aluminum with 0.5 percent copper, one can be encapsulating the conductor in a dielectric or incorporating oxygen during film deposition.

So, these are the useful means using which one can increase the electromigration resistance of aluminum, so we find that for aluminum two important problems are there, two drawbacks are there, so those are the limitations of aluminum in spite of having very advantages, one is the spiking which can be rectified using some metal barrier, say titanium nitride as we have discussed, or one can use for higher electromigration

resistance for aluminum, to avoid the problem of electromigration associated with the aluminum, and that can be done by alloying with copper or incorporating oxygen during film deposition, or in case of encapsulating the conductor in a dielectric.

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Copper Metallization

High conductivity, high electromigration resistance (compared to aluminum)

Drawback:

- tendency to corrode under standard chip manufacturing condition
 - Lack of feasible dry etching method
 - Nonavailability of self-passivating oxide similar to Al_2O_3 on Al.
 - Poor adhesion to dielectric materials such as SiO_2 , low-k polymers, etc.
-

So, now because there are some problems with the metal, so is copper better. Now, we shall discuss the copper metallization is copper better, you see that copper has high conductivity, high electromigration resistance compared to aluminum, and to minimize the r c time constant. The copper is widely used, because the resistance of copper is very very small, with list with with low k dielectric, the copper is widely used.

Now, what are the drawbacks for copper? The drawbacks for copper are that, it has a tendency to corrode under standard chip manufacturing condition, so corrosion is there number two is lack of feasible dry etching method, dry etching is an important component for VLSI, and dry etching is not feasible in case of copper which is available in case of aluminum. Also, there is no such Al_2O_3 on aluminum oxides of copper which is known as the native oxide for self passivating, non-availability of self passivating oxides similar to Al_2O_3 on aluminum, and it has poor adhesion to dielectric materials such as, SiO_2 , low k polymers, etcetera. So it has many drawbacks but, because of the high electromigration resistance and high conductivity, one can use

the copper metallization.

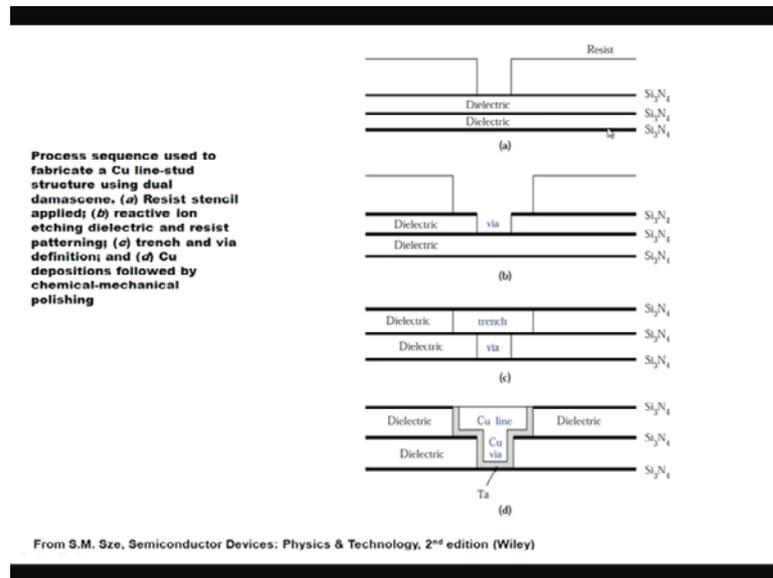
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Techniques for multilevel Cu interconnects

- **Pattern the metal lines followed by dielectric deposition (conventional).**
- **Pattern the dielectric layer first and fill Cu metal into trenches. Then remove the excess metal on the top surface of dielectric by chemical mechanical polishing and leave Cu material in the holes and trenches (Damascene process).**

Now, there are two techniques using which multilevel copper interconnects are made, one is the conventional method, pattern the metal lines followed by dielectric deposition, or one is known as the damascene process. In damascene or double damascene process the, you pattern the dielectric layer first and fill copper metal into trenches, then remove the excess metal on the top surface of dielectric by chemical mechanical polishing, and leave copper material in the holes and trenches. So, normally this damascene process or the or double damascene process is used in case of multilevel copper interconnection.

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And in this case, you see that in double damascene process generally photolithography and reactive ion etching is used, photolithography and reactive ion etching is used to make the trench and via, then copper metallization is done excess copper is removed by chemical mechanical polishing, and then this kind of process is known as the double damascene process.

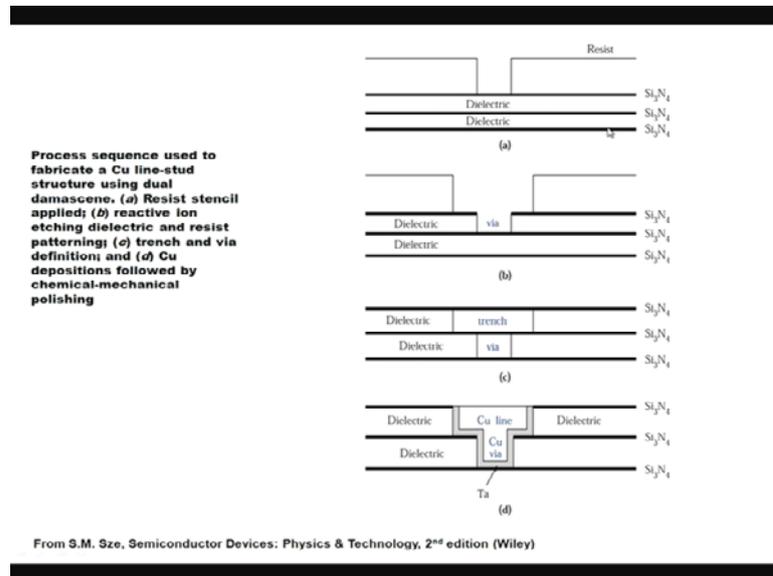
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Dual damascene process: the vias and trenches in the dielectric are defined using lithography and reactive ion etching steps before depositing Cu metal. Then a Cu chemical mechanical polishing process is used to remove the metal on the top surface leaving the planarized wiring and via imbedded in the insulator.

Advantage: via plug is now of the same material as the metal line and the risk of via electromigration failure is reduced.

In double damascene process, the vias and trenches in the dielectric are defined using lithography and reactive ion etching steps, before depositing copper metal.

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So, this is the last stage of copper metal deposition but, before copper metal deposition trench and via are made, first the via between two dielectrics, then the trench above the via is made by some lithographic and ion reactive ion etching process, you see here between different dielectric layers, we want to make a trench and the via, so lithography and reactive ion etching steps are used.

Then, a copper chemical mechanical polishing process is used, to remove the metal on the top surface leaving the planarized wiring and via embedded in the insulator, you can see that the via is embedded in the insulator. And what is the advantage? advantage is that via plug is now of the same material as the metal line, and the risk of via electromigration failure is reduced. So, this via and copper metal line are the same metal, so electromigration failure is not there, so that means you have to use some trench and via which will be defined by the lithographic process, and this is known as the double damascene process which is widely used in case of the copper interconnect.

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If we replace Al with Cu wire associated with some low-k dielectric ($k = 2.6$) instead of SiO_2 layer, what percentage of reduction of RC time constant will be achieved? (Given, resistivity of Al = $2.7 \mu\Omega\text{-cm}$ and that of Cu = $1.7 \mu\Omega\text{-cm}$).

Now, if we replace aluminum with copper wire associated with some low k dielectric instead of SiO_2 layer, what percentage of reduction of r c time constant will be achieved? So it is very easy that, you have to take the ratio of the resistivity of, copper to aluminum multiplied by the ratio of the dielectric constant of copper to low k dielectric to SiO_2 , and then 100 percent and it will come to about 42. So that means if one can replace the copper with aluminum, then we can find that 42 percent of the delay can be reduced.

So, if we summarize today's lecture, we can find that polysilicon deposition, we have undertaken, and then aluminum and copper, the associate problems of the aluminum was the electromigration and the spiking, which can be avoided by using some barrier metal etcetera. And finally, the copper it has some disadvantage compared to aluminum still, because of the resistance is very very less, it is widely used for making the low r c delay interconnect network.

Thank you.