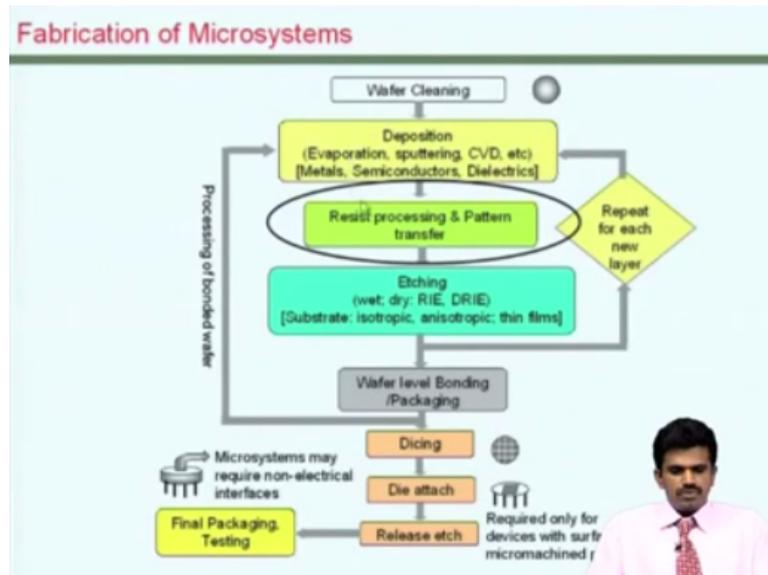


Micro and Smart Systems
Prof. K.J. Vinoy
Department of Electrical Communication Engineering
Indian Institute of Science – Bangalore

Lecture – 09
Approaches for Pattern Transfer

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I will talk to you today about various approaches that could be used for you know transferring patterns onto the way for building various microsystems. You are seeing this slide about the process flow required in building most microsystems. You have seen in a previous lecture in a various deposition schemes that are required for the you know depositing thin films onto this wafer.

So in today's lecture, we focus on how resist could be put on these wafers and how patterns could be transferred and onto the thin films and some of the required relevant steps in this context.

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Thin films used in MEMS

- > Thermal silicon dioxide
- > Dielectric layers
 - > polymeric
 - > ceramic
 - > silicon-compound
- > Polycrystalline silicon
 - > poly-Si
- > Metal films
 - > predominantly aluminum
- > Active Materials
 - > Ferroelectrics
 - > Piezoelectrics

Role of Thin films

- Structural
- Sacrificial
- Dielectric
- Semiconductor (epi-layers)
- Conductor

> Usually thin film materials may have multiple functions



Thin films used in MEMS include thermal dioxide of a silicon various dialectic materials these include polymeric materials, ceramic materials as well as silicon compounds in such as silicon nitride and silicon dioxide. We also come across polycrystalline silicon, which is usually known as polysilicon. This is a very good contact material. It is also used in the context of microsystems as a structural material.

We will also require several metallic films such as aluminum or gold for conductors requiring the processing of microsystems. Active materials, smart materials such as ferroelectrics and piezoelectrics are also used in building smart microsystems. These thin films can have typically multiple roles and one of the common example is the polycrystalline silicon as I mentioned this could be used either as a contact electrode or as a structural member for microsystems.

So these thin films can have these multiple roles but these roles can be defined only when the thin film is patterned into something. Otherwise, the film is sitting all over the surface, so it is only adding bulk to the surface of the wafer. So patterning of these thin films is essential to build devices, to build microsystems on a wafer.

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Objectives of Pattern transfer

- > **Selectively remove thin films**
 - > Electrodes
 - > Dielectrics
 - > Microstructures

Pattern transfer followed by etching of thin film

- > **Create doped regions**

Diffusion/ Ion implantation
Performed after defining a masking film

So to selectively remove these thin films to form such electrodes dielectric layer or insulating layers or microstructures, we need to transfer a pattern or create a pattern on the film on the surface of the wafer. So it is also sometimes required to create doped regions of a you know various semiconductor materials or layers on the wafer. This is usually done by diffusion and ion implantation, which is usually done after creating a masked film layer which is patterned and so in today's lecture we will talk about all these in the context of building microsystems.

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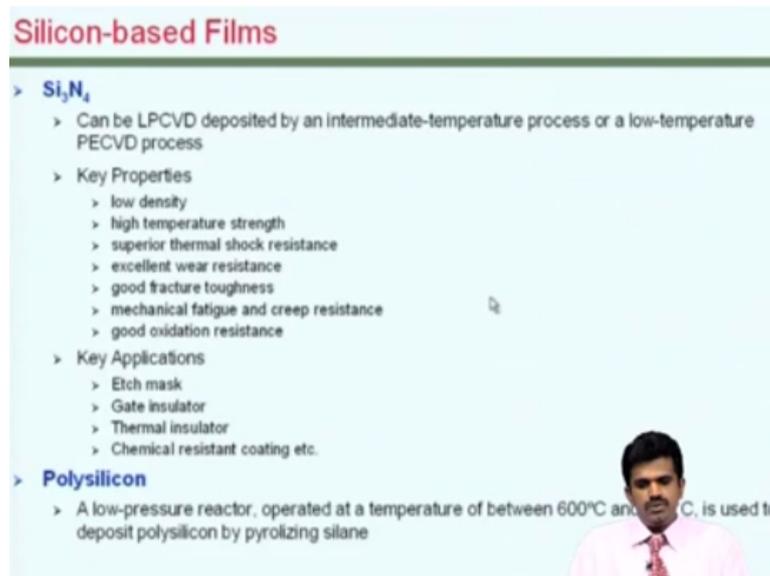
Commonly used Metals

- > **Aluminum**
 - > Basic electrical interconnections (common and easy to deposit)
 - > Non-corrosive environment only
 - > Good light reflector (visible light)
- > **Gold/ titanium/tungsten**
 - > Better for higher temperature
 - > Harsher environments
 - > Gold is good light reflector in the IR
- > **Platinum and palladium**
 - > Stable for electrochemistry

As you may have seen in previous other lectures commonly used metals in the processing of microsystems include aluminum, which is as I mentioned and there is a very simple material to be deposited very effectively onto silicon based surfaces. Another common example is gold, which usually require a sub-layer before that usually chromium or titanium is used for that purpose. We also come across platinum or palladium in several sensing applications

because of their special characteristics.

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Silicon-based Films

- > **Si₃N₄**
 - > Can be LPCVD deposited by an intermediate-temperature process or a low-temperature PECVD process
 - > Key Properties
 - > low density
 - > high temperature strength
 - > superior thermal shock resistance
 - > excellent wear resistance
 - > good fracture toughness
 - > mechanical fatigue and creep resistance
 - > good oxidation resistance
 - > Key Applications
 - > Etch mask
 - > Gate insulator
 - > Thermal insulator
 - > Chemical resistant coating etc.
- > **Polysilicon**
 - > A low-pressure reactor, operated at a temperature of between 600°C and 1000°C, is used to deposit polysilicon by pyrolyzing silane

We also have various forms of silicon dioxide used in the context of microsystems. It also come in the form of glasses and these are also used in microsystems. Another silicon based compound is silicon nitride, which could be deposited by LPCVD or PECVD techniques and has very interesting properties for building microsystems. Another silicon based film is known as polycrystalline silicon, which consists of small, small crystallite of silicon.

So within the crystallite it is a crystal of silicon but between crystallites there are grain boundaries because of which it is not a single crystal structure, it is a polycrystalline structure of silicon and still it has very good characteristics that are similar to that of single crystal silicon especially from the mechanical point or properties point of view and hence polycrystalline silicon is also widely used for microsystems.

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Polymeric Materials

- > **Photoresists**
- > **Polyimide**
- > **PMMA**
- > **SU-8**
 - > for wide range of thickness
 - > Thick resist
 - > Structural material in microsystem

Wide range of applications
 Microelectronics - coils, capacitors etc.
 Micromechanics - sensors, prototyping etc.
 Microfluidics- biochips, micropumps etc.
 Packaging - microconnectors, Chip Scale packaging, etc.
 Magnetics, Others like Flat panel displays, microoptics etc.

Polymeric materials used in microsystems include photoresist (SU-8) (06:59) and other polymers such as PMMA and polymethyl methacrylate and one of the materials that is becoming fast popular in the context of microsystems is SU-8, which can be used for a wide range of thickness, you know up to millimetre thickness. And hence it is used when the one need thick structural members or for you know thick resist materials and moulds and other microstructure applications.

So there are a wide range of applications possible for SU-8 in building microsystems.

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Patterning Thin films

- > **Lithography**
 - > Photolithography
 - > Litho - stone + graphein - to write
- > **Liftoff**
- > **Advanced**
 - > x-ray, Difficult
 - > electron beam Nano-scale

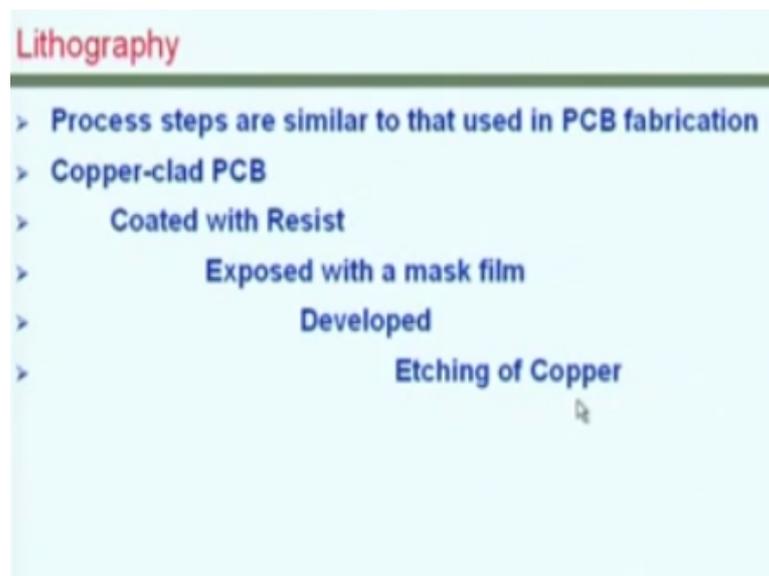
Most common in Microsystems

Now let us look at how these can be patterned. One of the very popular technique is known as lithography, which is usually based on visible light and hence it is called photolithography. They use a UV beam for the processing for the exposure in this particular context. There is a

variant I would say of the approach with some significant changes in the process steps required to and is called lift-off process and we will describe this a little later in the lecture.

There are also other advanced techniques based on electron beam or an x-ray for specialised applications especially for high precision geometries to be patterned.

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Lithography is a very common process for building printed circuit boards. In this case, if you have seen a printed circuit board, a bare printed circuit board it is essentially a copper clad dielectric material. And what is usually done there is that this copper clad material is coated with some kind of a resist material.

And then this resist material exposed after it secured is exposed with a mask film so that certain regions of this is exposed whereas the other regions which are hidden by the mask are not exposed to the UV light and then the resist film is then developed, which would essentially create hollow spaces through which the copper on the printed circuit board is etched. So that we can have traces on the printed circuit board.

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Mask

- > A stencil used to repeatedly generate a desired pattern and resist coated wafers
- > Consists of optically flat glass / quartz plate coated with an absorber (opaque to UV) pattern of metal. (eg, 800 Å thick Chromium layer)
- > Usually the mask is kept in direct contact with the photoresist while exposing to UV.
 - > This results in 1:1 image on the wafer (contact lithography).
- > Pattern on the mask
 - > Use CAD (L-edit) for drawing
 - > Use LASER plotter (resolution)



What we need to do to build microsystems to pattern microsystems is something similar. So the first thing that we need to have is a mask. A mask is essentially a stencil used to repeatedly generate the desired pattern of resist pattern, which is then transferred onto the resist coated wafers. It consists of the mask used in microsystems and like in the case of printed circuit board where typically a film is used.

Here it consists of a flat glass or quartz plate coated with chromium or similar material. And then this is your known pattern and kept as the stencil for using reproducing several devices or several layers with the same pattern. So you know creation of mask is also critical and these are usually done by 1:1 transfer of an image which is first created using a CAD tool typically people use, soft commercial software known as L-edit.

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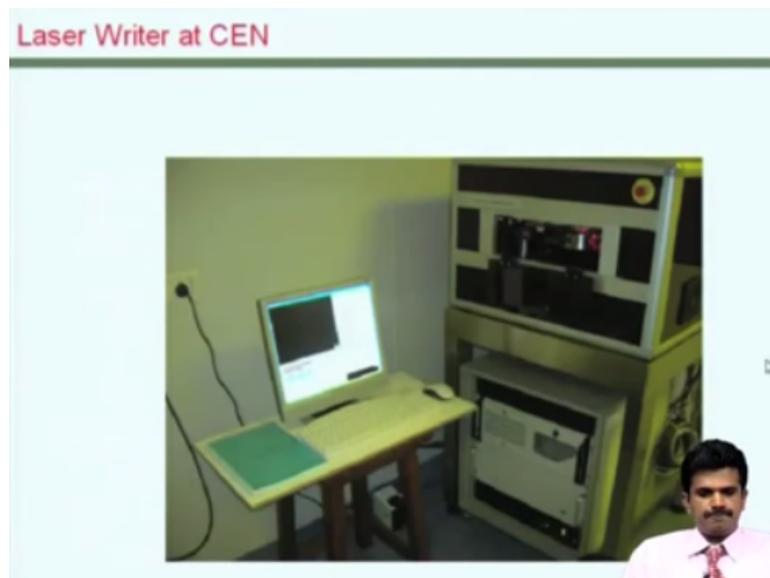
Laser Writer

- > Wave length of the laser is 405nm (GaN solid state laser)
- > Minimum feature size achievable : 1-2 μm
- > Various formats for drawings
 - > GDS, DXF & CIF formats can be used
- > High resolution multi layer patterning capability using alignment marks
- > Variable pixel to pixel exposure available – Gray level patterning
- > can be used for direct pattern generation on any substrate (including curved substrates) using photolithographic principles without using a conventional mask plate
- > Can also be used for patterning several materials including SU-8

And several of laser based bloating or you know writing schemes are available for transferring patterns onto the mask. One of the laser writer is based on a solid state laser source at 405 nm wavelength, which can have feature sizes up to 1 to 2 mm as low as 1 to 2 mm and it can you know it typically take various forms of drawing fires and you know has extended capability in terms of you know multiple layers and gray level.

And can be used, this can even be used to transfer the pattern directly onto the wafer as well not necessarily always to the wafer, always to the mask itself and you know both direct writing option as well as mask writing options are possible with today's laser writers. So several materials could be pattern not just the common photoresist using these laser writers of today.

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One example of a laser writer available with the facility in my institute is shown in this picture here.

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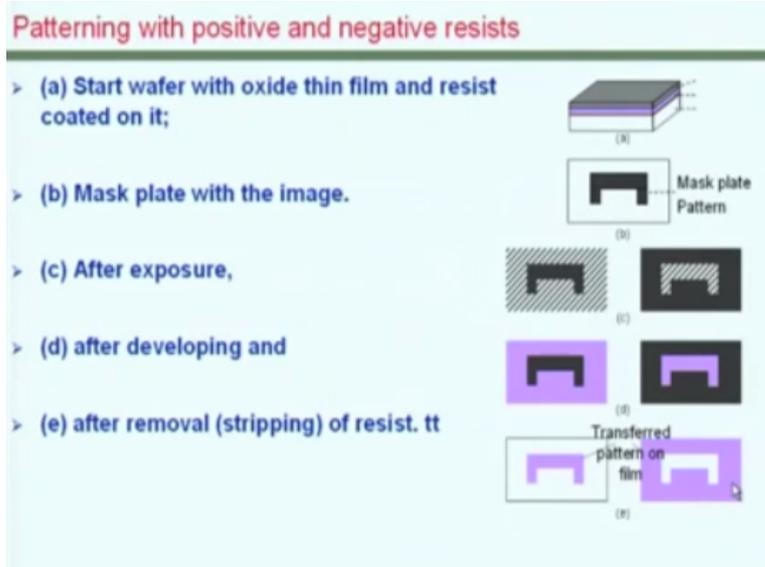
Resists used in Lithography

- > **Resist**
 - > Polymer base resin
 - > Changes structure when exposed
- > **Resist consists of**
 - > Sensitizer
 - > controls photochemical reaction
 - > Solvent
 - > enables spin casting
- > **Types (tones) of resists**
 - > Positive tone
 - > Photochemical reaction weakens polymer
 - > e.g., PMMA (poly methyl metacrylate)
 - > Negative tone
 - > Exposed resists hardens by crosslinkage of polymer main chains



The resist material that is used in microsystems fabrication is also slightly different from what is used in the printed circuit board fabrication. This has in the other is polymer based resin which essentially changes its structure when exposed to the particular UV light. And it consists of the sensitizer and the solvent as in the other case. And we can get positive and negative tone resist materials commercially. And could be used for the fabrication of microsystems.

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The difference between the positive and negative photo resist is illustrated in the schematic here. Let us say that we have a pattern like this on the mask plate and is being transferred onto the wafer after it is transferred when you have a positive resist you get exactly the same and when you have a negative resist you have the opposite of that transferred onto the resist layer.

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Comparison of Negative and Positive Resists

Parameter	Positive Photoresist	Negative Photoresist
Commercial Examples	AZ 1350J, PR120	Kodak 747, SU8
Adhesion to Silicon surface	fair	excellent
Cost	expensive	relatively cheap
Developer process tolerance	small	wide
Suitable for lift off process	yes	yes
Minimum feature size with UV	< 0.5 μm	<2 μm
Opaque dirt on clear portion of mask	Not very sensitive	pinholes
Resistance to plasma etch	very good	Not so good
Step coverage	better	Not so good

There are some differences in the way these resist materials could be used and that is obviously why both these types are available. If there are some dirt on the mask plate that would result in you know what are called pinholes in the negative when we use negative photoresist.

Whereas the chances of forming pinholes is almost negligible and almost never possible in the case of photoresist. On the other hand positive photoresist is typically more expensive. Positive resists are usually used when better precision with lower feature size are required. The step coverage in positive resists are usually better than negative photoresist

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Positive and Negative Resist materials

- > **Positive photoresists**
 - > poly methyl methacrylate (PMMA).
 - > diazquinone ester + phenolic novolak resin
 - > sensitive to UV light in the range 300 to 400nm
 - > can be developed in alkaline solvents such as potassium hydroxide, ketones or acetates.
- > **Negative photoresists**
 - > typically two component bisazide rubber resist or azide sensitized poly isoprene rubber.
 - > less sensitive to optical and x-ray exposure but are more sensitive to electron beam.
 - > Xylene is a common developer for negative resists

RESIST	ZONE
Kodak 747	Negative
SU 8	Negative
AZ 1350J	Positive
PR 102	Positive

There are several examples of positive and negative photoresist materials there are used in

typical laboratory environments.

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Patterning: Photo Lithography

- > Objective: To pattern SiO₂ layer
- > Oxide by wet oxidation
- > Resist coating
 - > Spin coating
- > Soft baking
 - > resist contains up to 15% organic solvent
 - > removed by soft baking at 75-100°C for ~ 10 minutes
 - > Release stress, improve adhesion of the resist
- > UV exposure
 - > Water mask alignment
 - > UV lamp used to illuminate the resist should have,
 - > Proper intensity
 - > Directionality
 - > Spectral characteristics
 - > Uniformity across the wafer
- > Development
 - > transforms latent resist images joined during exposure into a relief image
- > Post baking
 - > To remove residual solvents
 - > Annealing of film to improve adhesion
 - > Improves hardness of the film
 - > done at 120°C for approximately 20 minutes
- > Etching of SiO₂
- > Resist striping

The slide also features a small diagram of a layered structure with a red top layer, a black middle layer, and a white bottom layer. A presenter is visible in the bottom right corner of the slide frame.

Now let us see how photo lithography could be used for the fabrication of a microsystem in this particular case for patterning a thin film layer. What we show here is patterning an oxide layer on a silicon wafer. So what we need to do first is obviously to form this oxide layer on the silicon surface. This as I mentioned in another lecture on formation of thin films. This could be done by dry or wet oxidation.

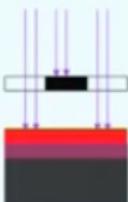
It is also possible to have SiO₂ films, silicon dioxide films on silicon surface by you know various other depositions schemes such as LPCVD. So let us say that we have a silicon wafer and it is let us say oxidised to form these oxide thin film. To transfer the pattern, as in the case of printed circuit board it is a sample that I sighted earlier the first step required is to coat a resist.

And this is done by spin coating. In spin coating what we do is we put a few drops of the resist material appropriate on the surface and hold it onto to this vacuum chuck in a spinner and spin the wafer at several 1000 RPM. After it is spun what you get is a uniform thickness of the resist on this surface. It is then taken for a what is known as a soft baking, which is usually done by putting this in an oven or a hot plate at about 80 degree centigrade for about 10 minutes.

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Patterning: Photo Lithography

- > Objective: To pattern SiO₂ layer
- > Oxide by wet oxidation
- > Resist coating
 - > Spin coating
- > Soft baking
 - > resist contains up to 15% organic solvent
 - > removed by soft baking at 75-100°C for ~ 10 minutes
 - > Release stress, improve adhesion of the resist
- > UV exposure
 - > Wafer mask alignment
 - > UV lamp used to illuminate the resist should have:
 - > Proper intensity
 - > Directionality
 - > Spectral characteristics
 - > Uniformly across the wafer
- > Development
 - > transforms latent resist images joined during exposure into a relief image
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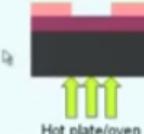



After that it is exposed to the UV beam by after with putting the mask on top of this. Usually the mask is placed directly on top of this. So that there is little diffraction happening or chances of diffraction at the edges of the mask. But it also has a issue that sometimes you know the debris from the resist can get attached to it and the mask plate by itself may get contaminated but usually it is done at this kind of a distance it is done at closely to the surface.

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Patterning: Photo Lithography

- > Objective: To pattern SiO₂ layer
- > Oxide by wet oxidation
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 - > Spin coating
- > Soft baking
 - > resist contains up to 15% organic solvent.
 - > removed by soft baking at 75-100°C for ~ 10 minutes
 - > Release stress, improve adhesion of the resist
- > UV exposure
 - > Wafer mask alignment
 - > UV lamp used to illuminate the resist should have:
 - > Proper intensity
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 - > Uniformly across the wafer
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 - > transforms latent resist images joined during exposure into a relief image
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- > Etching of SiO₂
- > Resist striping

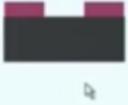



After it is exposed this film is developed by inserting it into in a path and you know when you are developing the unexposed region of the resist goes away. So what we have is a clear window through which we can essentially etch the film of the oxide, but not quite yet because the resist material that is here may not stand the chemical reaction that agent that you will be using.

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Patterning: Photo Lithography

- > Objective: To pattern SiO₂ layer
- > Oxide by wet oxidation
- > Resist coating
 - > Spin coating
- > Soft baking
 - > resist contains up to 15% organic solvent.
 - > removed by soft baking at 75-100°C for ~ 10 minutes
 - > Release stress, Improve adhesion of the resist
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 - > Improves hardness of the film
 - > done at 120°C for approximately 20 minutes
- > Etching of SiO₂
- > Resist stripping



Can be used for patterning metal and dielectric thin films

So to do that we again heat it, so that it sticks well to the surface and it does not go away when it is exposed to let say the acidic reagents that are required for etching the silicon dioxide. So when it is kept in this with path where it is, you know, you can etch the silicon dioxide and after that we can strip the resist by (()) (20:59) and various methods.

So what we get finally is a thin layer of silicon dioxide which was you know deposited by various approaches including oxidation, but patterned by the lithography contents. So as you could see from here there are several important things that are important steps to be followed for patterning any of these materials including metallic films on the wafer surface.

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Mask Aligner (Double sided) at CEN/IISc



Exposure modes	Constant Dose, Constant Time, Periodic
Alignment	X, Y: +/- 5mm, Theta +/- 3.5°, 0.06µm alignment resolution
Contact modes	Soft contact, Hard contact, Vacuum contact, Vacuum+Hard contact, Proximity
Microscopes (Top and bottom)	Split field with two objectives (3.6x, 5x, 10x, 20x.)
UV Lamp	Standard NUV for 350 - 450nm, 350W to 500W-Power
Printing Resolution	Depends on contact modes, contact pressure and process parameters.
Best achievable is 1 micron	

To transfer the pattern accurately on to the wafer surface we use what is known as a mask

aligner. In a mask aligner, we can accurately position the mask plate over the wafer. You may ask why is it critical. In a typical process flow of building a microsystems or an IC, we need to know, register where the reference points are so that the subsequent layers one over the other are aligned with respect to some non-references.

So it is possible to do that by accurately positioning the mask plate above the wafer. So we intentionally create alignment mask in every layer and every processing layer and these are required to be carried through till the end of the processing so that proper alignment would be possible. So in this particular case, what you see is a double sided aligner in which case you can see it from 2 directions from the top and bottom and that is also important in the context of building microsystems.

In Microsystems we as you may see, you may want to process some part of the device on, let us say that top surface of the wafer and some part in the bottom surface. So an alignment between the top surface to the bottom surface is also important and that can be done using, what is called a double sided aligner.

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Etching of thin films

- > **Silicon Nitride etching**
 - > 1%HF → 60nm/min
 - > 10%HF → 500nm/min
 - > H₃PO₄ → 10nm/min (180C)
- > **Silicon Dioxide Etching**
 - > Buffered HF → 100-250nm/min
 - > HF (very fast)
- > **Etch rates do vary depts on how the film was deposited (film quality)**
- > **Copper or Nickel**
 - > FeCl₃
- > **Gold**
 - > Aqua regia or Iodine
- > **Chromium**
 - > Aquaregia or HCl

The slide features a presenter in a pink shirt and tie in the bottom right corner.

To etch the thin films, we have seen silicon dioxide in the previous example, where you know one could lose buffered HF. When you use silicon nitride, various concentration of HF or even phosphoric acid could be used. It is the rates do depend on various properties and how the film is actually deposited. You may also want to you know pattern various metals and different compounds are used for etching them.

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Theoretical limits of Lithography

- > Smallest feature size by projection lithography is the same as the λ of the UV source
- > Factors affecting resolution
 - > Diffraction of light at the edge of an opaque feature in the mask
 - > Non uniformity in the wafer flatness
 - > Debris between mask and wafer
- > For $\lambda = 400\text{nm}$ $Z=1\mu\text{m}$ resolution is approximately $1\mu\text{m}$
- > Extreme ultraviolet lithography
 - > Requirements
 - > Reflective optics for camera.
 - > New resists.
 - > Imaging should be done in vacuum

As I mentioned, the lithography used in microsystems are a similar to what is done in a printed circuit board fabrication but in printed circuit board fabrication we usually get an accuracy of about 2 mL, which is about 50 microns whereas as I have mentioned earlier, it is possible to get about 1-2 micron in a typical lithography process used for building microsystems.

This is done based on by extending the lithography technique by accurately controlling various parameters used in the exposure as well as in developing, having in creating the thin film of the resist and things like that. One of the key parameters that affect the resolution in building in transferring pattern is the diffraction as I mentioned it depends on the separation, its effect will depend on the separation but it primarily depends on the wavelength.

So when you really want high resolution structures, you may want to use lower wavelength dips. The thickness and the proper positioning is also critical in terms of you know controlling and repeating in the production of the various patterned layers. You will also come across extreme UV lithography for because of these reasons when one would want to stretch the limits of lithography.

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New generation lithography techniques

- > **X-ray lithography**
 - > No need for vacuum.
 - > Flood exposure is possible
 - > Resolution- $0.5\mu\text{m}$, registration $\sim 0.2\mu\text{m}$
- > **Electron beam lithography**
 - > An electron source that produces a small diameter spot
 - > A blanker for turning the beam on and off
 - > Two electrostatic plates for directing the electron beam to the substrate
- > **Ion beam lithography**
 - > Resist is exposed to energetic ion bombardment in vacuum
 - > Point-by-point exposures with a scanning source (liquid gallium) or flood exposure with H^+ , He^{2+} or Ar^+ .

There are several new generation techniques used in lithography for high resolution geometries. Not so much in the context of microsystems but usually in the context of sub micrometer technologies for CMOS. It is also possible to use the electron beams for patterning layers in these applications. Even ion beams could be used for this purpose.

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E-beam Lithography

- > Smaller electron wavelengths makes E beam lithography capable of very High resolution. The wavelength of the electrons in a 10 kV SEM is then $12.3 \times 10^{-12} \text{ m}$ (12.3 pm)
 - > Line of 13nm width achieved
 - > Dots of 20 nm Diameter achieved
 - > Direct Write
 - > Nano manipulation
- > **Applications**
 - > Nano lithography with sub 20 nm resolution
 - > Fabrication of photonic crystals, Gratings
 - > Optical devices, holograms, micro lenses
 - > Three-dimensional structures
 - > CMOS process and device development
 - > E-beam induced deposition and etching
 - > Nano probing and electrical measurements
 - > High resolution SEM inspection



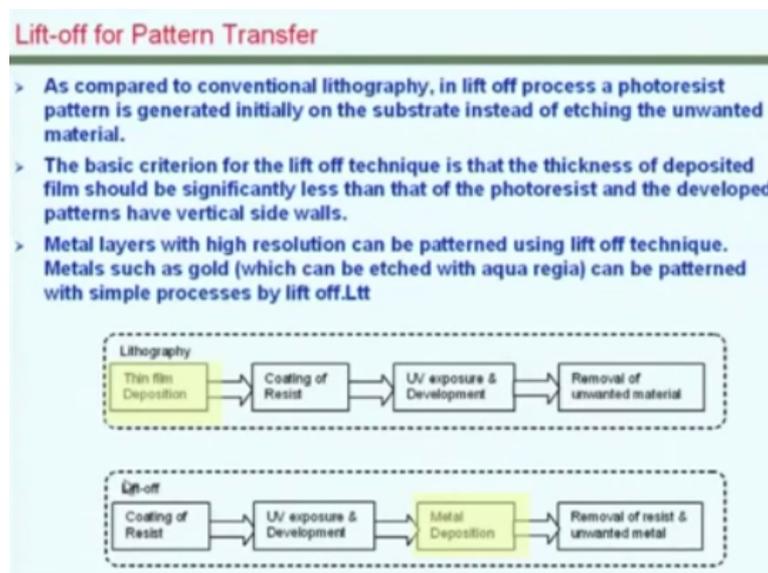
What you see here is an example of an E-beam lithography in our facility for patterning you know, a small dimension geometries in such as dots of several times of nanometers or lines of nanometers width and this is possible by using PMMA resist and using exposure using an electron approach rather than the UV lighting as you see so in the previous examples.

So the process steps are somewhat similar, use spin coat to PMMA resist and then the sample is loaded on to the equipment and the patterns are transferred using E-beam lithography and

then it is developed (()) (28:50). So it has various applications, the E-beam lithography has applications in nano lithography up to an even lower than, you know 20 nanometer resolution.

And it has significant applications in photonics because these dimensions come close to, you know the wavelengths that could be used and the gratings that could be created for various optical devices. It is also possible to extend these for 3 dimensional structures for microsystems applications or for CMOS applications. Some of these equipment available for the E-beam lithography can also be used for nano probing and high resolution SEM inspection of the layers that are formed.

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Lift-off technique is another pattern transfer approach which is somewhat similar yet different from their lithography approach. In a standard lithography approach what we do is first deposit the thin film and then coat it with a resist and then expose and develop and after that you remove the unwanted material whereas in lift-off what is usually done is, you first coat resist and then you know transfer the pattern by UA exposure and after that deposit the thin film usually, metal thin films such as gold are patterned by using lift-off technique.

As you may know for etch in gold, usually aqua regia is used which is a nasty chemical. There are other chemicals that could be used but still you know it is usually preferred to go with a lift of approach for the patterning of accurate patterning of films such as gold. So when the resist is removed, the unwanted metal will go and we will see that soon. So with lift-off technique, we can get high resolution geometries patterned and is as I mentioned it is

typically used for gold less.

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Detailed Steps involved in Liftoff

- > Objective: To create a pattern of Gold on an oxidised Si wafer
- > Oxide by dry/ wet oxidation
- > Resist coating
- > Soft baking
- > UV exposure
- > Development
- > Gold deposition (sputtering)
- > Liftoff

Can be used for patterning metal and dielectric thin films

So as in the previous example of photolithography, the objective in lift-off is also the same, it is to pattern a thin film layer and in this example we look at how to have a patterned layer of gold formed by the lift-off technique. We start with the silicon wafer and next step is not the deposition of gold because that is what we do if we were doing photolithography. In the case of lift-off, what we need to do is basically to coat resist.

But what we normally see in practice is that the gold does not add well with the silicon and in many practical applications, we do not actually put gold on to the silicon. So in this particular example, we have a wafer which is actually oxidised or coated with a thin layer of oxide before the resist is formed and this is not what is to be patterned. This is put essentially for other reasons.

So then we put the resist first, and then soft bake it and then expose it and then we develop that resist and we develop that resist and you do not necessarily how to do the hard baking, we do, what we do next is the gold deposition. Now if the resist coating is substantially thick and the coating scheme used for the gold does not have the step coverage. What you can see is that there is a gap between this.

So now if we put it in a solvent in which this resist can be dissolved as the resist goes away along with that the metal on top of it will also go away. So what remains there is a patterned layer of gold. So as you could see the sequence of events are slightly changed in the in during

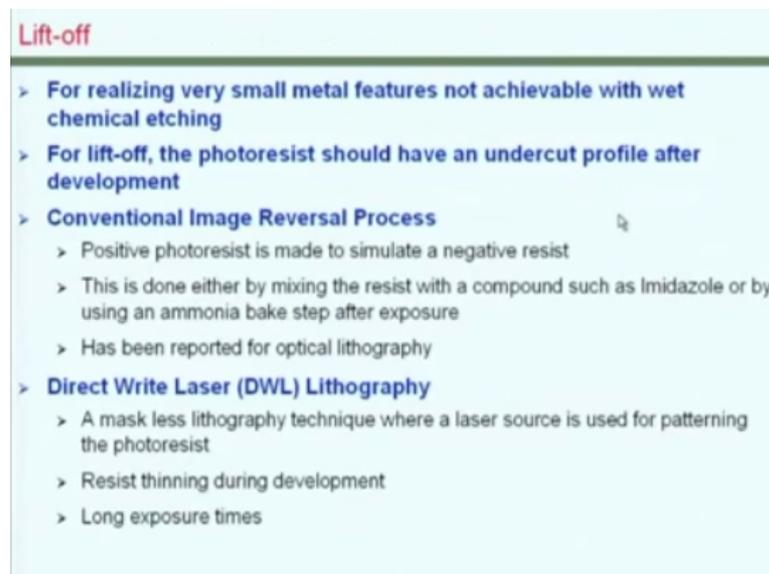
for processing for pattern transfer by lift-off and what you have avoided in this particular case is etching of the target, of the gold layer.

If you were to do the same thing by lithography after the pattern transfer, we would be doing the etching of the gold. That would have required aqua regia and you know other chemical such as iodine for a example. But in this case, that is avoided. But what is critical in this case is to have the you know a step coverage, so that there is no continuity between these gold layers and possibly a good thickness of the resist can ensure that.

But we cannot just keep on increasing the thickness of the resist because if you have it too thick, it may not you know develop well, it may not expose well when you use a normal unit. So we need to have some kind of a compromise between the thickness and the coverage. There are some innovative schemes which could be used so that there is a discontinue, we can ensure that there is a discontinuity between these films.

So that the final removal by dissolving the resist material would result in removal of the unwanted metal and not the metal that you would need to keep over there. So the lift of technique in fact can be used for various materials including metals and dielectrics.

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Lift-off

- > For realizing very small metal features not achievable with wet chemical etching
- > For lift-off, the photoresist should have an undercut profile after development
- > **Conventional Image Reversal Process**
 - > Positive photoresist is made to simulate a negative resist
 - > This is done either by mixing the resist with a compound such as Imidazole or by using an ammonia bake step after exposure
 - > Has been reported for optical lithography
- > **Direct Write Laser (DWL) Lithography**
 - > A mask less lithography technique where a laser source is used for patterning the photoresist
 - > Resist thinning during development
 - > Long exposure times

So in lift-off, we can have very fine resolution features by wet chemical processes. What is critical as I mentioned is that the dummy layer, the photoresist layer that you are using should have an undercut profile after development so that there will be a discontinuity between the top and bottom metal layers. There are several approaches, you know as you have seen here

the pattern transfer is done similar to what is done in the case of lithography.

It is also possible to use the direct writing option as I mentioned earlier for this purpose, which is essentially a mask less approach. We are directly writing on to the surface of the wafer.

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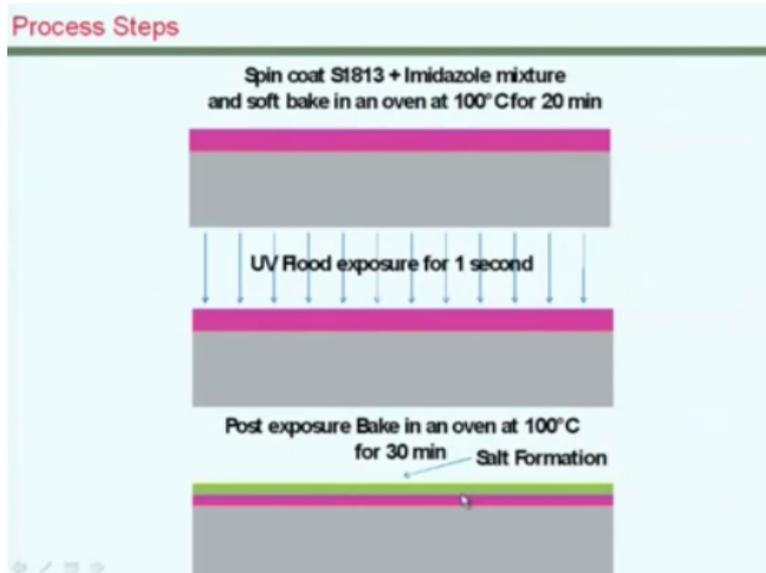
Lift-off by surface Modification

- > **Difference**
 - > For every 2ml of positive photoresist, 27mg of Imidazole is added
 - > Imidazole acts as a catalyst in the decarboxylation reaction of the exposed photoresist regions
- > **During post exposure bake, the rate of decarboxylation speeds up, thereby forming Indene, a salt, which is insoluble in photoresist developers.**
 - > This salt formation is limited only to the top surface of the resist because of the short duration of UV flood exposure.
 - > The remaining bulk resist is still photoactive and behaves like a positive photoresist.
- > **The formation of the salt creates a difference in the solubility of the top surface and bulk of the resist in the developer, leading to an undercut profile upon development.**



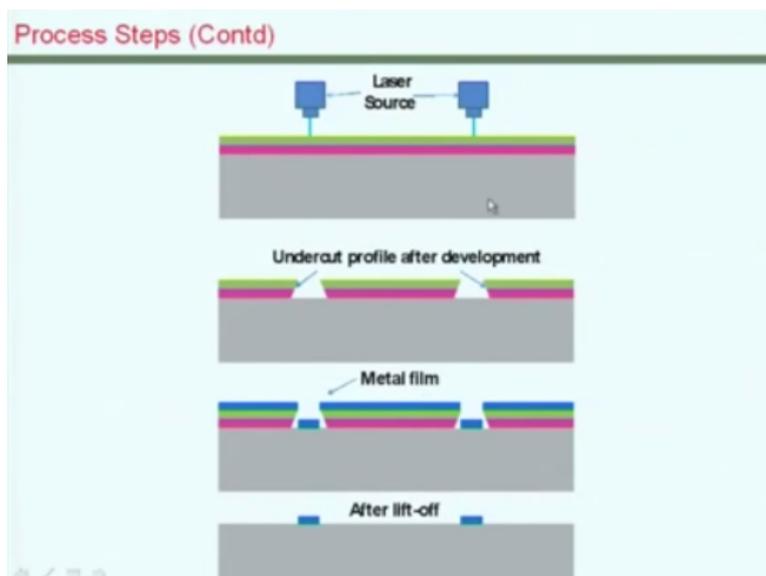
So in this case, because the exposure characteristics, you know certain precautions have to be taken to ensure good you know step coverage so that there is a discontinuity between the films that would be formed. To do that, one of the approaches that has been developed in our centre is based on modifying the resist material and it is called an image reversal process. In this case, after when it is baked after the exposure. Some compounds are formed on the surface which would enable the undercut.

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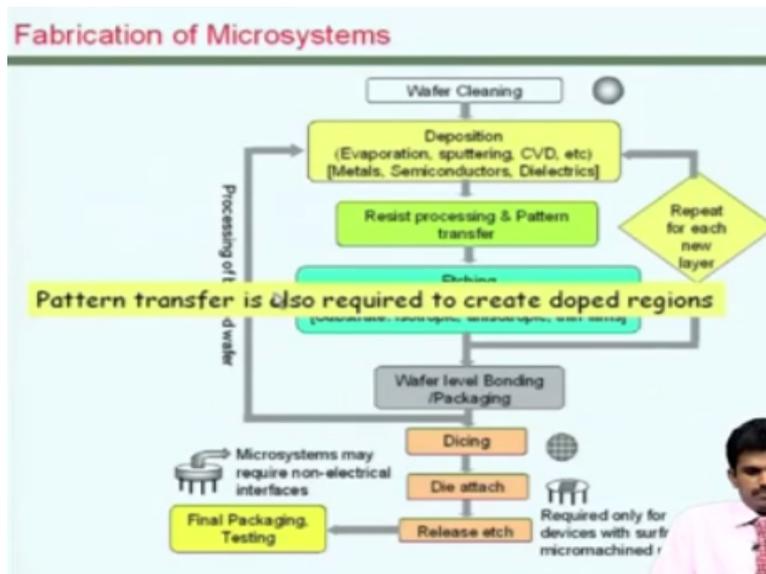
So as you would see here what we do is that on to the wafer we spin coat this modified compound and then when it is exposed, this salt is formed on the surface.

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And after that you know when you are actually doing the pattern transfer by the laser source, there will be an undercut. And this undercut will help in having a discontinuity between the metal film on the top and the metal film below. So when the resist material is dissolved in the solvent, the metal film on the top will go away and the one below will not be taken along with it. So that will stick better with the surface when we follow this modified approach.

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So as you see from the flow of events required for building microsystems. Pattern transfer could be used here for building these, you know films patterned. It is also required to create doped regions as I mentioned previously

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Diffusion and Ion Implantation

- > For doping of semiconductors, controlled quantities of impurity atoms are introduced into the selected regions of the surface through masks on the top of the wafer.
- > Diffusion and Ion implantation are common methods for this.
- > N and P regions can be formed for active semiconductors
- > Also used as etch stop layers
- > Diffusion
 - > Wafer placed in a high temp furnace and a carrier gas is passed. Boron and phosphorus are commonly used dopants
 - > The deposited wafer is heated in a furnace for drive in, oxidising or inert gas to redistribute dopants in the wafer to desired depth
 - > Silicon dioxide is used as the masking layer

Make	Tempres
Temperature Range	800-1200 °C
Dopant Source	POCl ₃
Bubbler Gas	Nitrogen (0.4ft ³ /min)
Carrier Gas	Nitrogen (4 ft ³ /min)
Flow rate of Oxygen	0.6 l/min

Make	Tempres
Temperature Range	900-1200 °C
Dopant Source	Boron Nitride Disc
Process Ambient	Nitrogen
Flow rate of N ₂	4 ft ³ /min

Doped regions are required for semiconductor devices. It is a very commonly known that we would need N and P type regions in any semiconducting device with various doping levels. Diffusion and ion implantation are 2 approaches used for this purpose. Such diffused or doped regions are also useful as also known as etch stop layers. An etch stop layer is a region where the chemical reaction characteristic of the surface is different and usually much lower than the remaining.

So when some regions of the surface is doped, it reacts less with the reagent and hence, this

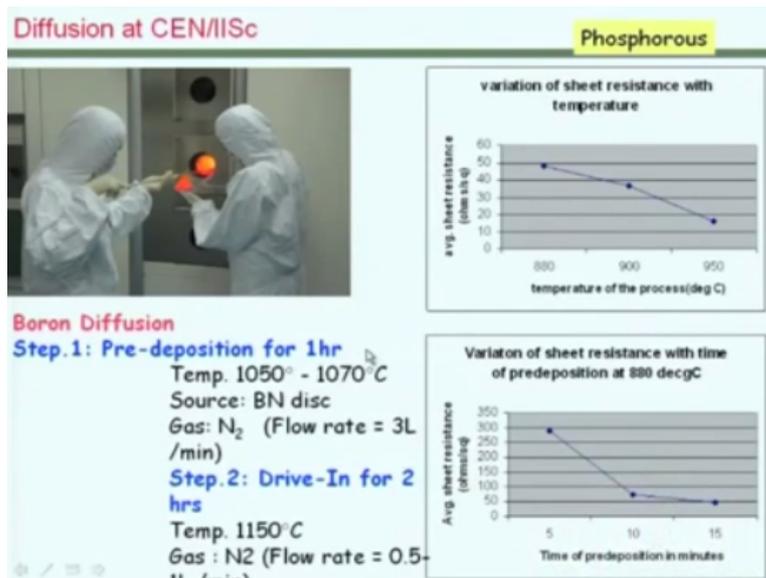
cannot be dissolved as compared to other regions and that is very useful in building certain geometries on the silicon wafer. Hence, diffusion is an important step in, you know, transferring pattern. After transferring pattern in building microsystems. N and P type regions can be formed by depositing either phosphorus or boron material on to the silicon. It is done at extremely high temperatures in a, you know, in our case it is a tempress furnace.

There are different options available and you know, you have, you typically have the nitrogen gas as the atmosphere. The dope N by itself is coming from either a compound of phosphorus or silicon which is essentially the source of the respective materials. In this cases, you know, when we really want to only, you know diffuse on to certain regions of the surface, we obviously do not want to diffuse everywhere.

We need to have defined a masking layer and usually silicon dioxide is used as the masking layer. So the silicon dioxide is first patterned by the approach that we have seen so far and then region of the wafer is you know diffused with these compounds to diffused within these high temperatures to get the doped regions of the wafer. And the diffusion as the name indicates means there is some kind of a you know a diffusing happening over there.

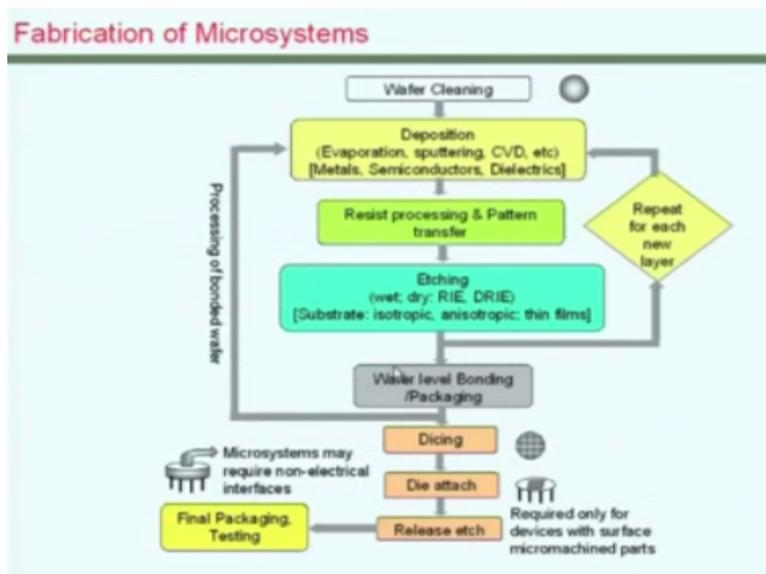
Strictly what is happening is that. From the source of the dope and first the phosphorus or boron is transferred and a sort of deposited on to the surface of the wafer. After that we do a process typically known as a drive in which include some kind of a oxidation or invert gas atmosphere which helps in redistributing the dopant into the surface of the wafer, into the some depth of the wafer. So that we can have a uniform coverage to certain depth on the wafer.

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So these 2 steps are typically used in process in you know realising such diffused regions or doped regions. As you see here is a, you know, a pair of operators working with a furnace used for diffusion in the facility here and this graphs indicate the process parameter used for phosphorus and what you see here is the process parameters used for the diffusion of boron and as I mentioned both of these are important in various context for the fabrication of a, you know different top regions of silicon.

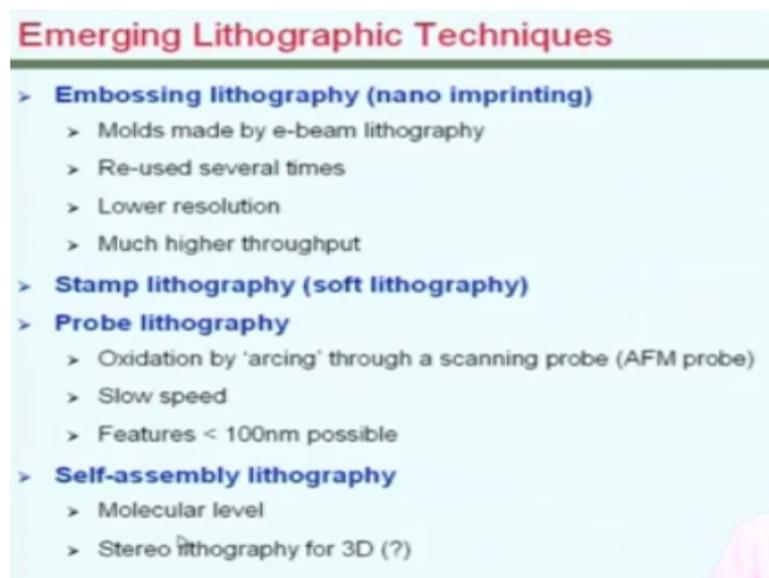
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So as you see here, the pattern and the building of microsystems would recur a series of such deposition and patterning steps to be repeated. So as you recall the, you know, various materials are used for building microsystems and these material thin film layers are individually patterned one at a time for building microsystems.

But still as you could imagine, lithography is a plan our process. This process would, can only be used for transferring a pattern on to the surface or a film on the surface of the wafer. Now how do we extent these approaches into building microsystems. So, we will touch upon how this can be done to realise some microstructures and how these processes that we have seen here could be extended for billing microsystems.

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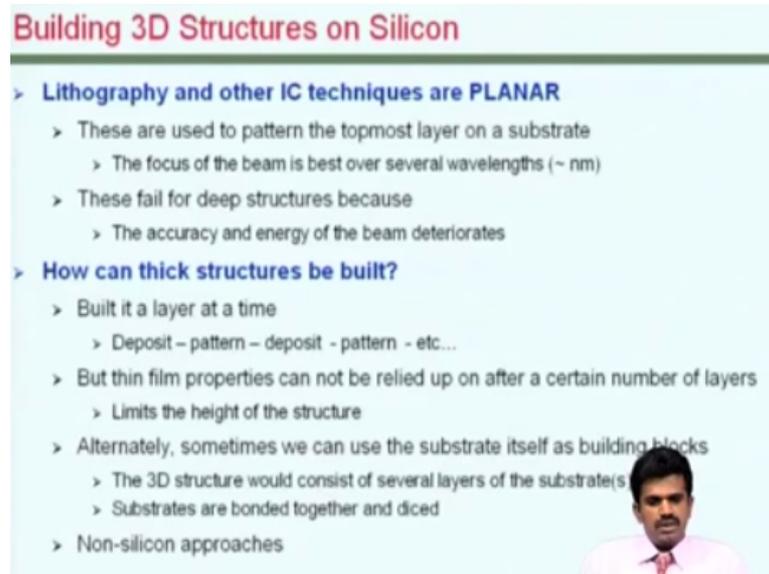
In this context, it is interesting to note some of the emerging approaches for lithography. There are techniques such as nano imprinting which are emerging for you know, mold which basically make use of moulds made by the e-beam lithography which as I mentioned can result in high resolution geometries and these moulds are essentially reused multiple times, so that we can get better resolution geometries at higher throughput.

So the cost of production using e-beam is basically shared because we are reusing the mold. So this approach by itself become, you know, a low cost approach for building microsystems and in another similar approach is based on what is called stamp lithography or soft lithography which also basically used initial mold made by the high resolution approaches and reusing them for productionising different devices.

It is also possible to use a technique known as probe lithography which essentially use oxidation by arcing for the pattern transfer. In building microsystems, on strictly speaking, even nano technology based systems, it is possible to use what is known as self-assembly for their overall structure.

So this is essentially a molecular level process and can be extended for 3 dimensional structures by techniques known as stereo lithography. We will talk about some of these in more detail in another lecture where we talk about polymeric materials and microsystems based on polymeric materials.

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Building 3D Structures on Silicon

- > **Lithography and other IC techniques are PLANAR**
 - > These are used to pattern the topmost layer on a substrate
 - > The focus of the beam is best over several wavelengths (~ nm)
 - > These fail for deep structures because
 - > The accuracy and energy of the beam deteriorates
- > **How can thick structures be built?**
 - > Built it a layer at a time
 - > Deposit – pattern – deposit - pattern - etc...
 - > But thin film properties can not be relied up on after a certain number of layers
 - > Limits the height of the structure
 - > Alternately, sometimes we can use the substrate itself as building blocks
 - > The 3D structure would consist of several layers of the substrate(s)
 - > Substrates are bonded together and diced
 - > Non-silicon approaches



So we will see how 3 dimensional structures can be patterned on silicon using lithography. The lithography technique as I mentioned is essentially a PLANAR technique. We can only use it for patterning the topmost layer because the beam that is used for exposure is only capable of having only certain thickness. So it does not go deep into the structure and only pattern, the resist layer in most cases.

And you know, in many cases it fails to, when you really have dope structures. So how do we build thick structures and how do we you know realise moving structures based on lithography. We still build one layer at a time and pattern one layer at a time but we can arrange this their sequence in such a way that you know, we can remove material below one layer.

For example, you can have a dummy layer and create a structural layer above this dummy layer and later selectively remove this dummy layer to create moving space. You have to remember that when you have multiple thin films their properties could be different. So the choice of materials used in these multiple thin films is critical in realising such structures for microsystems applications.

It is also possible to use the windows created by the etching processes that we have seen as the mask and further on dig into the silicon wafer by etching the silicon wafer. So we can use approaches to such approaches to remove the silicon from the substrate itself selectively obviously to build what are known as bulk micromachined structures. There are also approaches based on non-silicon materials such as ceramics and polymers.

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Silicon Micromachining

Based on Photolithography

- > Photolithography defines regions on silicon wafers where machining is done.
- > Machining includes etching, doping and deposition of thin films.
- > Fabrication of three-dimensional structures with complex forms only in two dimensions is possible.
- > Extension to 3D structures can be accomplished to using wafer bonding.



So we will now briefly see how these can be done for silicon micromachining. In silicon micromachining, the processors are essentially based on photolithography and it is used for somewhat 3 dimensional structures in complex forms but you know essentially lithography as we have seen is a planner approach. We need to tweak it to get this 3 dimensional approach, 3 dimensional structure.

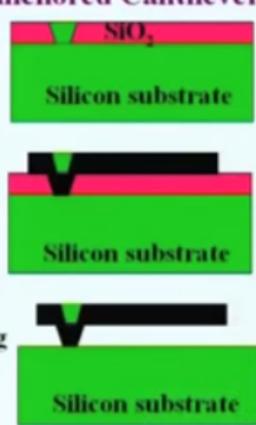
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Surface Micromachining

➤ Microstructures are fabricated on a Silicon substrate by deposition and selective etching of multiple layers of structural and sacrificial films

Polysilicon is structural layer and SiO₂ is the sacrificial layer

Steps to realize a Poly anchored Cantilever



Patterned Polysilicon

Free standing Cantilever

Surface micromachining is one of the common approaches scheme of events required for fabricating such structures. What is done here can be explained based on the process steps that you have seeing in deposition and patterning. What we need to do on top of the silicon wafer is to first form a silicon dioxide layer which is to patterned to create this hollow space.

And then deposit a second layer which in this stage consists of polysilicon and then make it to freestanding by removing the (()) (55:06). Polysilicon as I mentioned is a good structural material and that can be used for microsystems applications. And this is obviously a structure that is freestanding. Hence, this layer which was deposited second is known as the structural layer.

The layer, the dummy layer that was removed is known as the sacrificial layer because it is removed afterwards. So in the final device you do not see that sacrificial layer, what you see is a free standing cantilever. So as you could see, we only need to deposit and pattern to form a freestanding cantilever structure. There are several interesting new answers which are very critical in realizing such structures repeatedly.

We will see some of these in subsequent lectures, when we go deep into surface micromachining and bulk micromachining for the fabrication of microstructures but as you could see is essentially the deposition and patterning of materials, suitable choice of materials and the control of their deposition schemes, that is important in building such microsystems. Thank you very much.