Nanoelectronics: Devices and Materials
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Lecture - 09
High-k gate dielectrics

Today we will look at one very important issues today that is Direct Tunneling Current.

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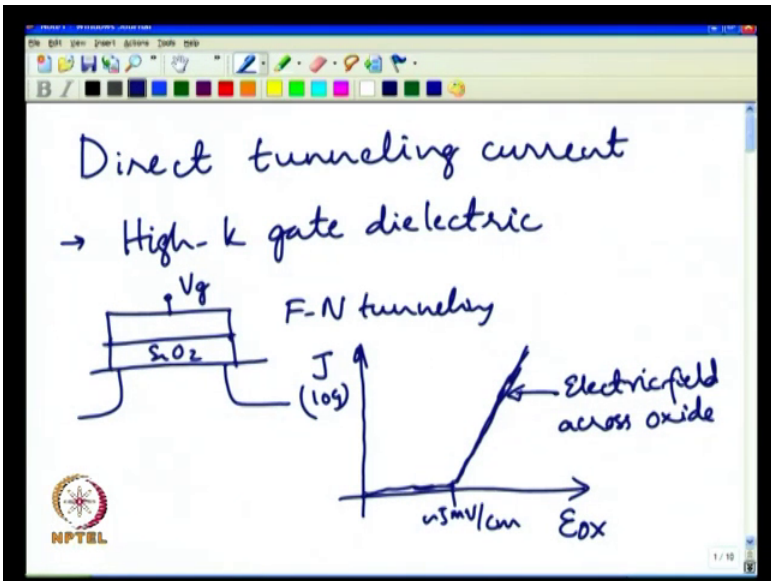

And you know then we will see that you know in order to overcome this problem, we need to use what is called High-k gate dielectric. So, in the last class we had seen that when you have this m o s transistor with silicon oxide as gate dielectric when you start applying voltage even though you are well below the breakdown limit of the silicon oxide, you can start conducting through silicon oxide and that we said is Fowler-Nordheim tunneling right and we also discovered that the Fowler-Nordheim tunneling is essentially a function of electric field across (Refer Time: 01:22) that is if you were to plot your electric field as a function of current density, with current density in a log scale you will see that initially there is very little current and then you know it will take off exponentially. And hence you see this linear dependence in log linear plot, and this happens at about 5 mega volt per centimeter or so.

And then I mean now if you continue to increase the electric field eventually you will reach the breakdown as well. And if you recall we said what is very crucial here is electric field across the oxide right and this E that we are plotting here is really electric field across oxide, I mean if you want to be more precise you call it E ox which indicates what is the electric field across the oxide, what it essentially means is the following right if it is only dependent on electric field.

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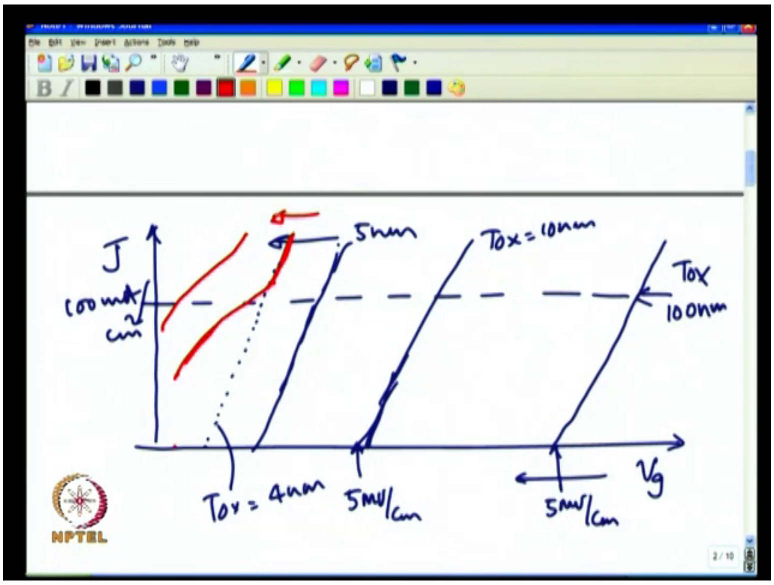

Then if you were to sort of plot this as a function of gate voltage, the current density and you would expect that you know if you see this kind of behavior for 100 nanometer thick oxide.

Let us say this is oxide thickness is 100 nanometer and at this voltage across 100 nanometer you are able to produce an electric field let us say which will an equivalent current density of let us say 100 milli ampere per centimeter square, and if you recall what I had told you last time is that at about 10 megavolt per centimeter electric field, you start seeing current density of the order of 100 milli ampere per centimeter square. Now if you go to a different oxide thinner oxide let us say 10 nanometer for example, then what you would expect is that because oxide thickness is coming down to produce the same electric field and same currents I need to apply lower voltages correct. So, all that will happen is that this curve will sort of translate as is along the voltage axis, right.

In order words you may say that the curve will look something similar here, this is for T ox is equal to 10 nanometer the shape will look almost similar right it is only the voltage translation and if you have anything between 10 and 100 nanometer, you will have series of curves which will lie somewhere in this area and here again at this voltage you have an electric field of the order of 5 mega volt per centimeter, that will corres this voltage will correspond to that electric field because oxide is thinner and for a thicker oxide in order to produce the same electric field you need to go to much larger voltage correct.

I mean that is what would you expect and as you start scaling down instead of 10 you know if you came down to 5 nanometer, you know you would expect that you know this should again continue to sort of look like this, that is what the Fowler-Nordheim theory says. Now what happens really is that as we scale start scaling this further and further, 5 nanometer and below even at 5 nanometer you start seeing some departure from this expectation and more particularly let us consider a case of 4 nanometer right let us say I have a 4 nanometer, based on Fowler-Nordheim theory say I need to get the current which looks like this.

Let us say this is for T ox is equal to 4 nanometer, but very interestingly what happens is that you may see this behavior at very large electric field, but meaning corresponding to larger voltage, but as you start scaling the voltage rather than current going down like this you will see that the current will actually tend to look like this, there is a huge shoulder in other words even at lower voltages which corresponds to electric field of less than 5 mega volt per centimeter could be 4 mega volt, 3 mega volt 1 mega volt per centimeter. You see significantly large leakage current and this let us say 4 nanometer in three nanometer you may size something like this you know this this could be even more serious.

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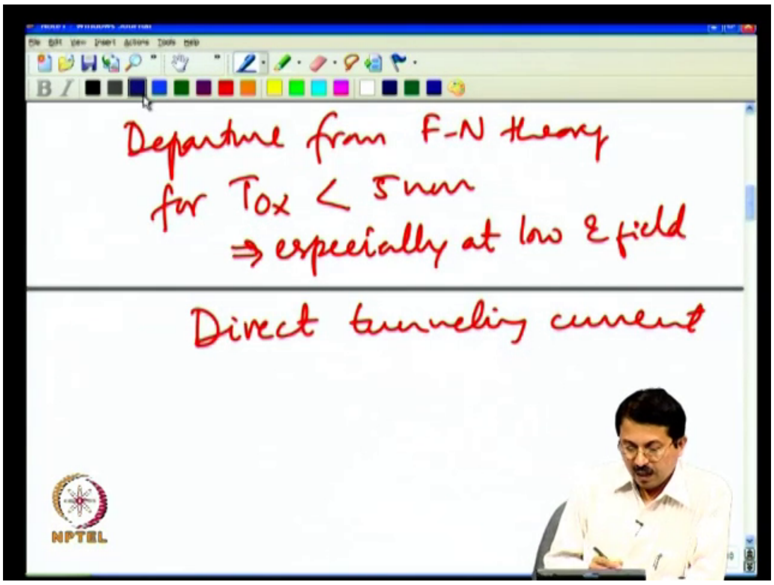

So, in other words you start seeing a departure right from F N theory, for oxide thickness in the range of less than 5 nanometer and this is especially at low electric field and this phenomenon is what we call direct tunneling current. Now let us try to understand what is really happening here and if you look remember the Fowler-Nordheim tunneling theory what we had said is that.

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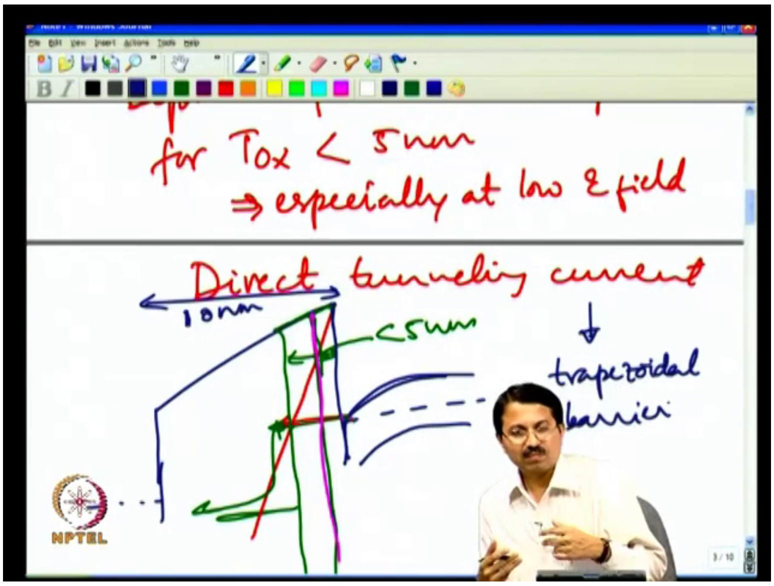

You have an m o s structure which is a thick gate oxide here and this is your silicon right you apply voltage the bands out bent and these electrons needs to tunnel through into the oxide, but at lower gate voltages you do not see that as you start increasing the gate voltages, this band bending starts looking like this and that is when you start seeing this direct current.

Now, let us imagine a situation when this say situation is for an oxide, which is as thick as 100 nanometer or you will let us say even 10 nanometer. Now let us imagine a situation where my oxide is not as thick its only 5 nanometer in other words it would or let us say 4 nanometer whatever it is then it will look something like this correct this is where you have your oxide boundary and this is where you have your gate electrode. Now you see what is happening here this distance is now comparable to the tunneling distance which would have anyway happened due to the Fowler-Nordheim theory right there is tunneling distance is less than 5 nanometer, you start seeing electrons going into the other side.

Now, the fact that the oxide to begin with itself is less than 5 nanometer, even when you have a very low electric fields electric fields are indicative of this band bending; low electric fields, but there is this gate electrode and there are these empty states and these electrons can easily tunnel through in a load energy state and get collected in the anode that you have at the gate this is positive voltage and this is negative voltage right.

So, as this distance starts coming down instead of 5 nanometer, let us say I have just one nanometer thick. In one nanometer thick this problem is even more series severe because even when you have very low electric field for very low gate voltage, the tunneling distance from substrate silicon into the gate electrode because gate electrode is right here now, that is extremely small that is one nanometer. So, you will see a huge tunneling current. So, as a result of that the direct tunneling current is simply because of the fact that my gate oxide thickness itself is in the regime, where carriers can easily tunnel through less than 5 nanometer and.

In fact, this tunneling is really called you can remember Fowler-Nordheim tunneling, we said tunneling through a triangular barrier because when the carrier were tunneling the barrier looked like a triangular barrier whereas, direct tunneling is really you know, so called tunneling through trapezoidal barrier. Accordingly there is you know slight difference in the tunneling current expression and there are very well developed models again you know you have an exact expression, analytical expression which gives you the tunneling current in direct tunneling current regime let us not really look at that equation

But let us try to conceptually understand that direct tunneling is a very severe problem when gate oxide thickness is less than 5 nanometer and so, much so that even at the operating gate voltages you one volt or even less than a volt 0.5 volt, you can have a huge tunneling current going through the gate oxide, and that is what we call a direct tunneling current and that is why you see a departure from Fowler-Nordheim theory as per (Refer Time: 10:20) tunneling you should not have any current, because of the direct tunneling you have huge current.

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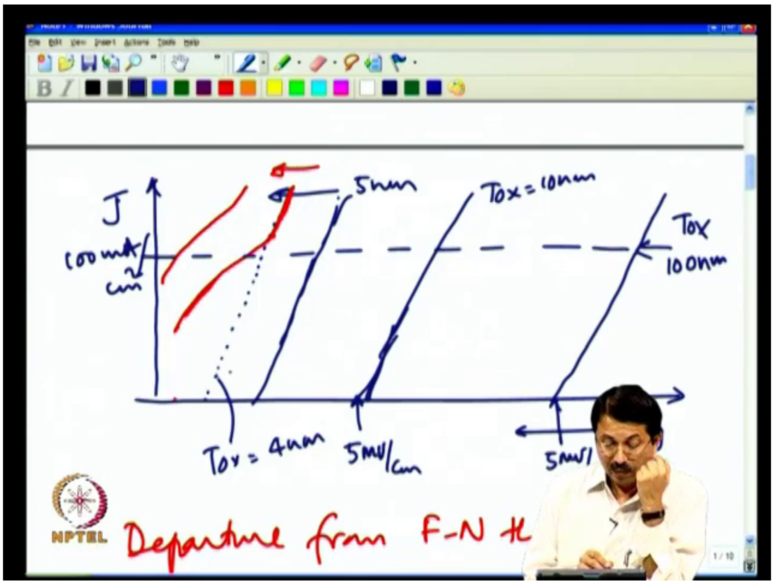

Now as you start increasing the field, eventually if you have a very high electric field this barrier again starts bending very severely and you may again approach a case where the tunneling is happening through a triangular barrier, at very high electric field at that point you know your tunneling current will be as predicted by your Fowler-Nordheim tunneling current. That is why at large electric field it may agree with the prediction, but at a lower electric field and lower gate voltage, it will completely depart from the f n prediction ok.

So, this is the problem with the direct a leakage current, you know in other words direct leakage current.

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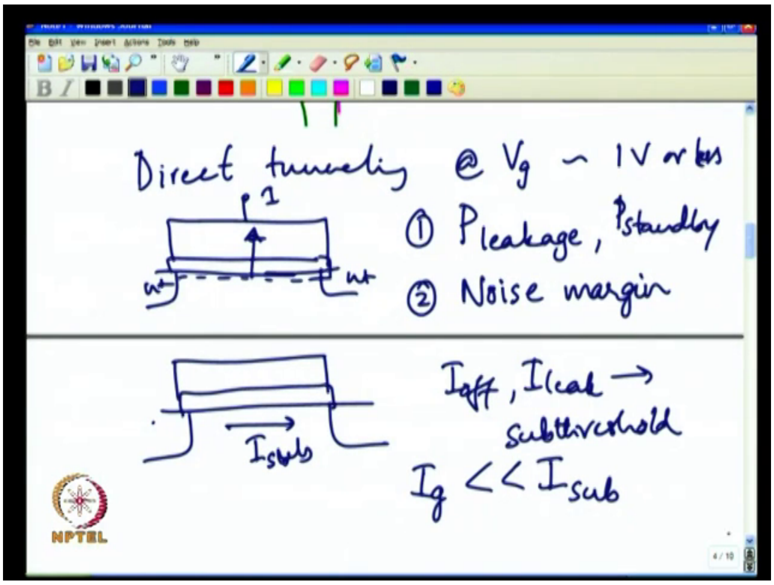

Direct tunneling current can happen at gate voltages as low as one volt or less, you see one volt is a operating voltage of a transistor. What it means is that if I have this transistor let us say n channel transistor, I have applied one volt which is the operating voltage of the transistor and you have all these carriers electrons sitting here, they will easily tunnel through this and result in a very large leakage current through the gate oxide.

So, now this is a very serious issue, its very serious issue for two reasons right; obviously, it is a very serious issue because you increase your leakage power or so called standby power. When the chip is in standby state transistor is not switching, you should not have any leakage right. But you know as you know in a circuit there is a steady state logic some gates are at one some gates are at 0 and so on and so forth. So, you have very large leakage current and not only that you can also have an impact on you know reliability such as for example, noise margin especially if it is a you know memory device for example, you can leak the over charge through this gate oxide tunneling which is not a very good thing right.

So, these are very serious problems you know and typically you know the figure of merit that we would like to put you see is that when the transistor is off if it is a n channel or p channel remember, when the transistor is off there is this. So, called sub threshold leakage current correct that is also a leakage current is a transistor, but that leakage current is a current flowing from source to the drain correct. So, typical off state current or leakage current in transistor is really sub threshold current. One figure of merit to you is when to decide when to use this oxide or when not to use this oxide is to say that my gate induced leakage current, I can tolerate maybe when it is about 10 percent of this conventional off state current, but if this gate induce leakage current starts becoming comparable to this sub threshold current, then there is a another big leakage component for your transistor right.

So, typically you do not want your gate current to be comparable to sub threshold in other words, you really want to I g to be as small compared to the sub threshold current and your sub threshold current of course, is your typical off state current right in a transistor you know.

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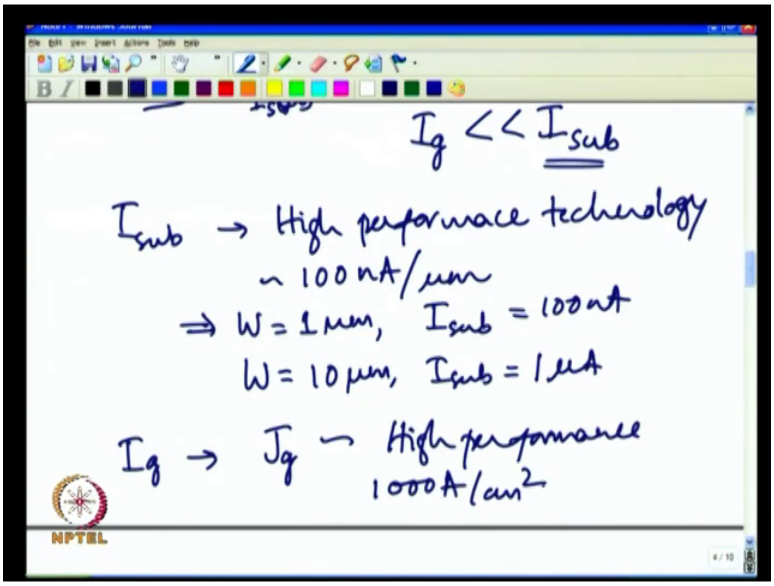

Typical sub threshold current that we see in a high performance technologies in high performance technology, what we mean here is that the technology or the transistors that are used to make a very high end high end microprocessor which need to be very fast transistor, they also tend to have large leakage current. The typical off state sub threshold leakage current expect today for this kind of technology is of the order of 100 nano ampere per micro meter.

Remember I had told you all the currents typically that is the on current and sub threshold off current of a transistor is always specified as current per unit width, what it means is that this per micro meter it means that if your width is 1 micro meter then your sub threshold off state current is 100 nano ampere. On the other hand if your width of the transistor is 10 micro meter, then accordingly your leakage current will increase 10 times right.

So, that will become you know 1000 nano ampere or 1 micro ampere. So, that is how we specify this. Now when we talk of the gate leakage current, the gate leakage current speck I gs right instead of I g we give current density speck just as the off state current here we normalize with respect to width of the transistor because depending on what is you width you scale it width right you get the appropriate on current and of current. The leakage current is going through the entire gate area and hence it makes more sense to give a specification in terms of current density.

So, typical current density specification again depends on what technology you are looking at, let say if it is a high performance technology again we can say that my J g current gate current density specification could be something like 1000 ampere per centimeter square that is you know the number looks huge, but you know it is per centimeter square if you were to scale it micro meter square correct you know you divide it by 10 to the 8, 1 centimeter is 10 to the 4 micro meter and one centimeter square is then to the 8 micro meter square.

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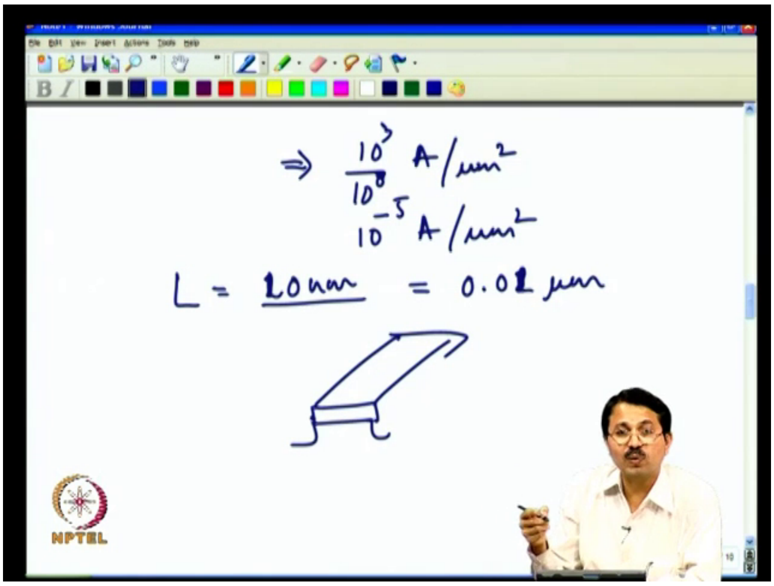

So, this is also equal to you know 10 power 3 by 10 power 8 ampere per micro meter square correct right or you know what is that it is essentially 10 to the minus 5 ampere per micro meter square. So, that is a kind of current density that we are talking about. This is for very high performance technology right and accordingly you know one can also convert this you know into an equivalent if you know what is the gate length of the transistor right then you can you can factor that in and you can convert it into appropriate speck which looks like ampere per micro meter if you wish right for example, what I meant there is that let us say my length is you know specified.

Let us say this is something that I am doing for a 20 nanometer kind of a technology. So, what is 20 nanometer? 20 nanometer is 0.02 micro meter correct. So, then what would happen essentially is that you know just to keep simple let me make it 10. So, that know I do not have multiply with the factor of 2. So, your 100 nanometer is 0.1 micron and 10 nanometer is 0.01 micro meter correct. So, then what you can do is that you can say for this length of a transistor then you can specify this gate leakage current in terms of ampere per micro width. Then depending on what is your width because you are going to make this transistor with 10 nanometer length and your width could be variable depending on what is your width you multiply with that width and you get the total current density correct.

In other words you can take this number and you know what will happen is that, if I have to express this in terms of ampere per micro meter of width just as our my sub threshold current density current speck is also ampere per micro meter width of the transistor then it would essentially look something like this.

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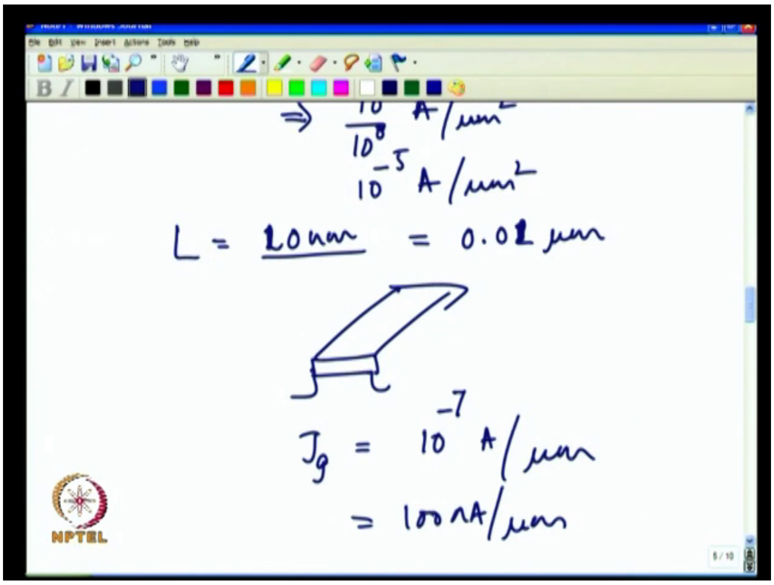

Your J g will look like you know this is 10 to the minus 5 and this is 10 to the minus 2, 10 to the minus 7 ampere per micro meter right and you know what is it its essentially about 100 Nano ampere per micro meter because 10 to the minus 6 is 1 micro ampere ok.

So, this is 100 Nano ampere per micro meter. So, what I tried to do with all this round about calculation is that would the reason why we chose thousand ampere per centimeter square is that given a transistor of certain width and let us say length of the order of 10 to 20 nanometer, your leakage through the gate is becoming comparable to your conventional leakage because of the sub threshold conduction. Now that is a problem because, there used to be only one conduction mechanism leakage conduction mechanism sub threshold.

Now, there is a gate leakage beyond this I do not want to really have any more leakage because then your off state leakage is just not governed by your sub threshold leakage your off state leakage is governed by your gate oxide leakage that is the worst thing to happen and that is why we come up with a specks like this you know thousand ampere per centimeter square or the same thing can be expressed as I said 10 to the minus 5 ampere per micro meter square right these are the different ways of doing the same specification or you could call the same specification as for a length which is well defined you know this will translate into something like 100 nano ampere per micro meter width of the transistor right the crux of the matter here is that gate leakage direct gate leakage is a serious problem at the operating voltage of the transistor, unless we do something you know we will have a huge problem in terms of.

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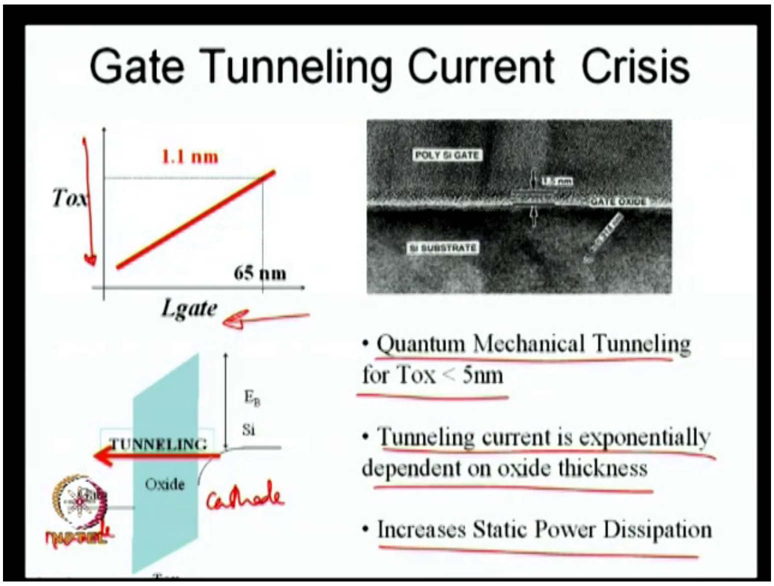

Controlling this and that is what is shown here right what this is telling you here is that you know as we scale down the technology decrease in the gate length, we have to decrease the oxide thickness and this is how a typical 65 nanometer technology or as 90 nanometer technology will look this is a transmission electron micrograph showing silicon ultra-thin silicon oxide which is of the order of 1.5 nanometer and a gate electrode.

And if you shrink the length further you need to shrink this further and that is when there is a huge leakage current tunneling current and quantum mechanical tunneling current for T ox less than 5 nanometer starts happening which is called direct tunneling current, tunneling current is an exponentially dependent on oxide thickness a very small decrease in oxide thickness results in a huge leakage and this results is static power dissipation as well as various other problem that we talked about. If you do business as usual you know we will have to scale oxide thickness silicon oxide, thickness less than a nanometer you see sometimes we fail to understand the magnitude at this length scales.

What is nanometer? Nanometer is 10 angstrom, 1 layer of silicon oxide is 5 angstrom it is as if you have only two layers of silicon oxide that is it. That is how thin it is you have silicon one layer of silicon oxide another layer of silicon oxide, even if one layer is missing in some region it is a deviation of 50 percent you cannot tolerate that and that is where we said if I decrease it further there is no way I can build chips. So, what do you do? You need to think of something else and that is the concept of what is called high k dielectrics.

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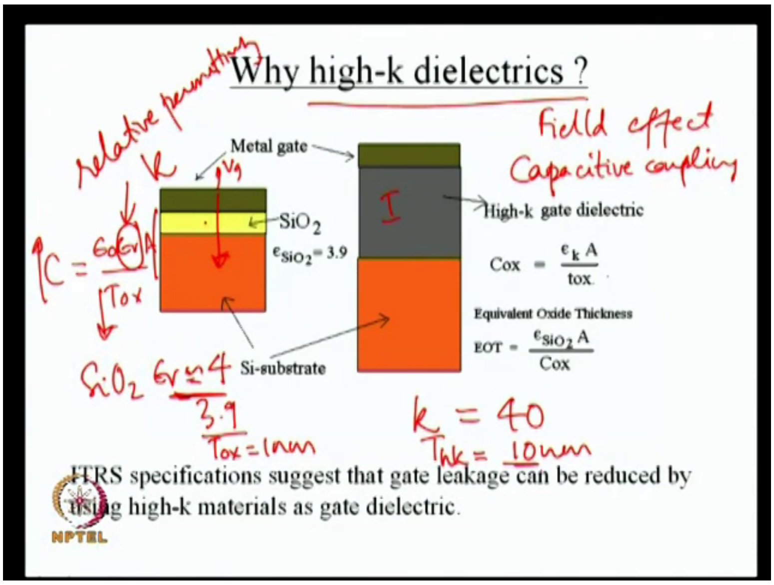

It is a very simple idea if you think about it; we are building transistors by growing silicon oxide on silicon why did we scale silicon oxide? Because we were scaling gate length the drain was coming closer to the source.

If you recall drain induced barrier lowering and all those effect the gate electrode should also be bought very close to the channel otherwise you lose gate control right in other words I need to enhance field effect from the gate now what is the field effect due to? The field effect in an f e t is due to capacitive coupling correct your gate voltage that your are applying here will capacitively couple to the channel, the very reason why we wanted to decrease oxide thickness is to enhance that coupling capacities that in turn enhances the field effect. Now this is what we did we wanted to enhance capacitive coupling the easiest way for us to do was decrease oxide thickness, because you do not need to worry about anything else grow the oxide for shorter time you get thinner oxide, but then we heater would lock the road block is this you cannot decrease oxide thickness any further.

If you do that you have a huge current going through this, then we discover look the capacitance equation has another term here and do not worry about area we typically we look at per unit area capacitance epsilon is a constant we cannot do much about epsilon naught free pace space permittivity epsilon r is a relative permittivity and this is what we also call as k, epsilon r or k are the symbol that are used interchangeably and we said look I need to increase capacitance as device physics dictates because drain is coming closer to source, I need to have more capacitive coupling, but why do you want to decrease T ox; necessarily why do not you keep T ox where it is or even increase T ox to suppress leakage current and choose a different material all together which has large k value what is k of ep Si O 2 Si O 2 epsilon r is approximately 4 3.9 to be precise, but let us say 4 round it off to 4 that is your relative permittivity and what we are saying is a following.

Instead of silicon oxide which has epsilon r of 4. Let us choose an imaginary material which is an insulator and that has a k value or epsilon r value 40. Then we are saying if this is the case rather than using one nanometer of Si O 2, if you were to use this whatever high k thickness which is 10 nanometer they are equivalent correct equivalent in the sense they produce same capacitance, capacitive coupling here and here is exactly same right.

So, that a very very interesting observation right and what it means is that as soon as you increase this to 10 nanometer, what is 10 nanometer? 10 nanometer is the distance between let us say your cathode here and the anode, electrons are trying to go from cathode to anode because these two electrodes came.

So, close to each other less than 5 nanometer there is so much huge leakage current why not increase that distance. So, if you increase that distance direct tunneling is suppressed altogether. And you still do not lose any device physics in terms of building a good transistor threshold voltage control because you have same capacitance coupling and hence the name high k gate dielectric, it is a gate dielectric and it is replacing silicon oxide with some other new material and this is what is illustrated here.

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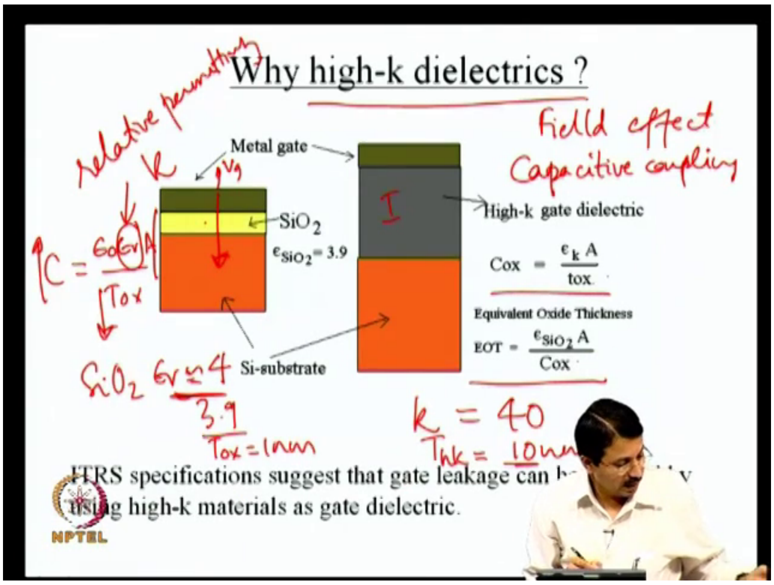

And in this context we use a term a called E O T and E O T, you know essentially means that you know rather than this I will give this is expressing total capacitance right if you go back to per unit area capacitance, what we are saying here is that let me ok.

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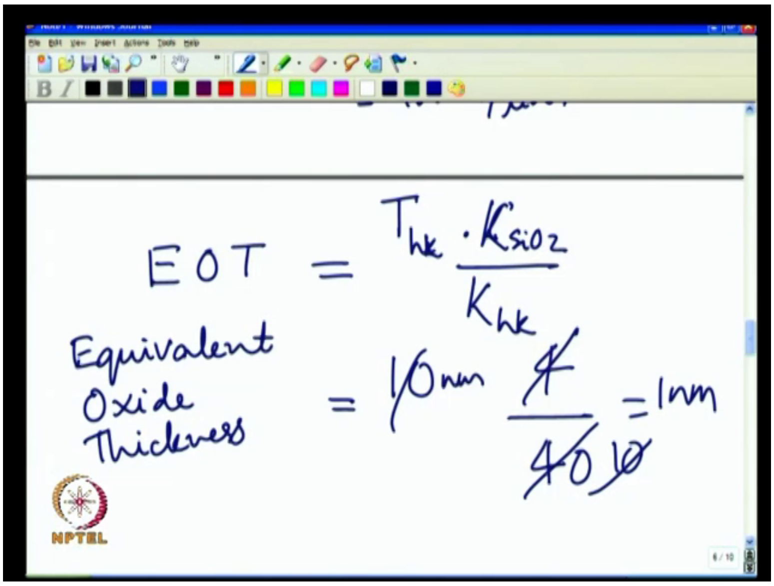

So, we define a term called E O T or it is essentially called equivalent oxide thickness. It is defined as T high k, I will just say h k or t k k indicates it is a high k material times epsilon r of silicon oxide which is you know 4 let or 3.9.

Or let me just say k of Si O 2 divided by k of that high k material, this is how we define the so, called E O T what E O T means is that even though I have used a thicker material it is equivalent of using a silicon oxide of this thickness. In other words if I use at 10 nanometer material insulator, which has a k value as I mentioned of 40, then it is equivalent of using one nanometer Si O 2 that is the meaning of E O T. In literature if you see recent literature you see this term quite often E O T of one nanometer or we have achieved E O T of sub one nanometer using hafnium oxide gate dielectric.

It does not mean that the physical thickness of hafnium oxide is one nanometer or 0.8 nanometer it just means that it is equivalent to using silicon oxide of one nanometer, but. In fact, I used hafnium oxide which maybe 5 nanometer or 8 nanometer depending on what is its k value you see and that is the concept of this E O T this is a very important concept to remember ok.

So, that is why we need high k gate dielectric ok.

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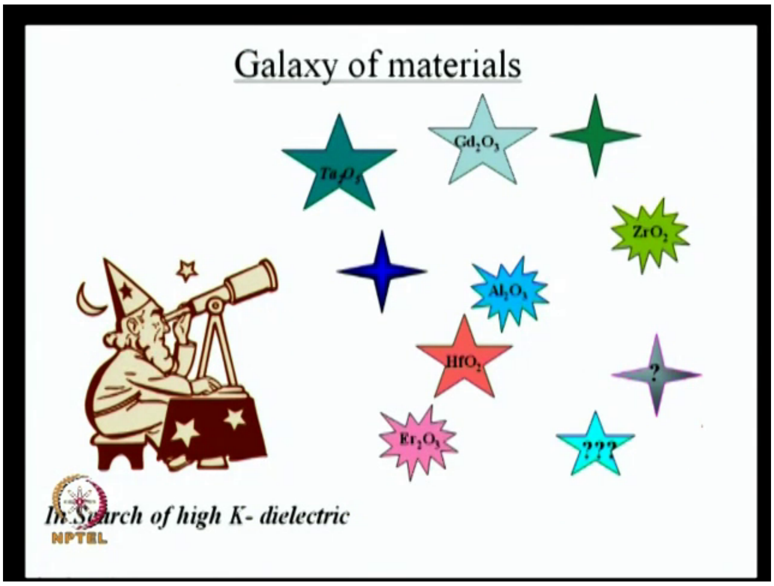

Now, what high k gate dielectric? You know there is huge possibilities right is there a basis in choosing this right all these are you know some examples of high k gate dielectric.

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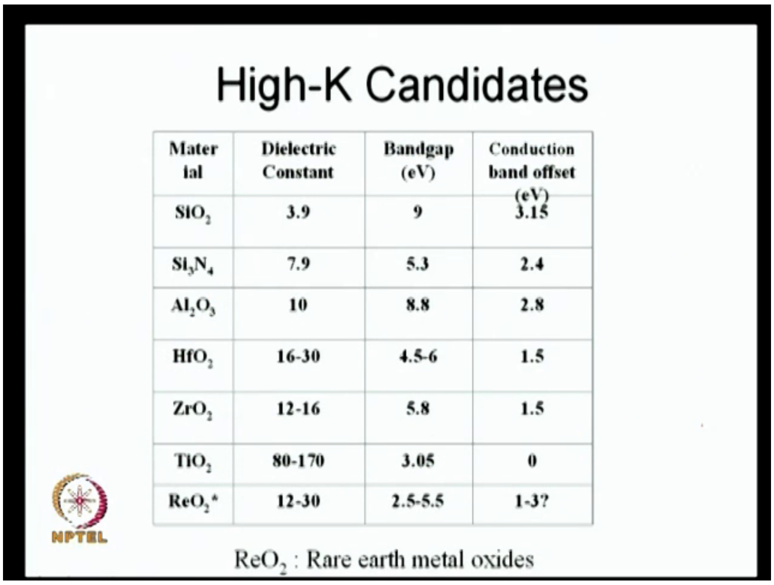

Right this for example, silicon oxide is our conventional gate dielectric.

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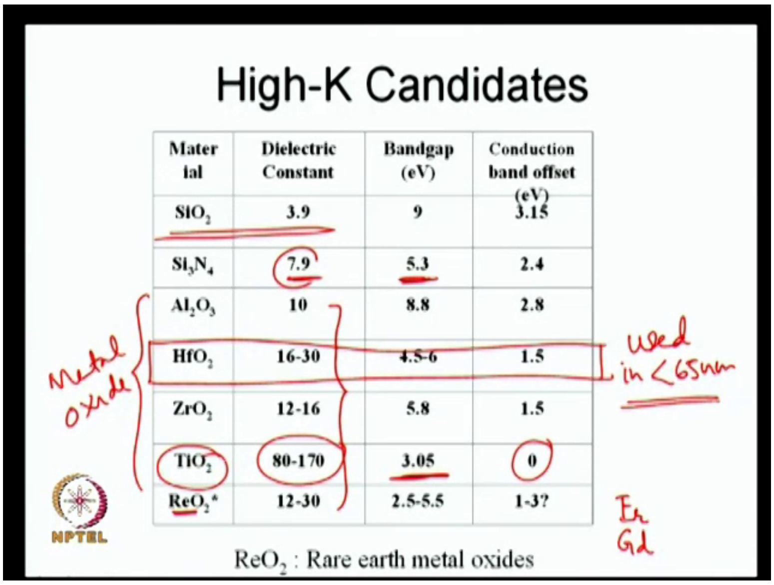

So, what are the additional properties that we are looking at in high k gate dielectric. Dielectric constant is one thing we want to go to a thicker I mean higher k value. So, that I can use thicker insulator material, but band gap is also an equally important property not just band gap, we also say band off set is an important property. So, what we mean by that essentially is ok.

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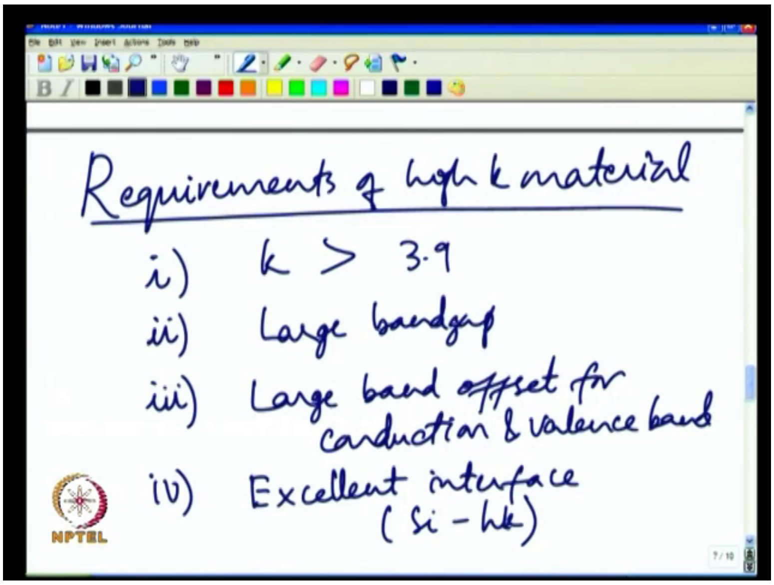

So, let us say what are the requirements right one is of course, k is greater than 3.9 that is very obvious right otherwise we cannot make the film thicker. The next one is that large band gap and along with large band gap we also need it does not just sufficient to just have large band gap, but large band off set for conduction and valence band both. This is a important requirement, then we need to have a excellent interface what is this interface? Silicon and high k interface remember we said reason why silicon technology is. So, successful is that we can build excellent fets in silicon because silicon oxide silicon combination is.

You know god given right given an excellent properties at the interface in terms of surface passivation now can I get the same surface passivation using this new material, instead of having 10 to the 10 per centimeter square interface traps, if you have two orders of magnitude higher traps, then you know you are throwing all the advantages having high k because your mobility will be so low and your threshold voltage could be so high that you can never build a transistor. So, that is an important aspect then.

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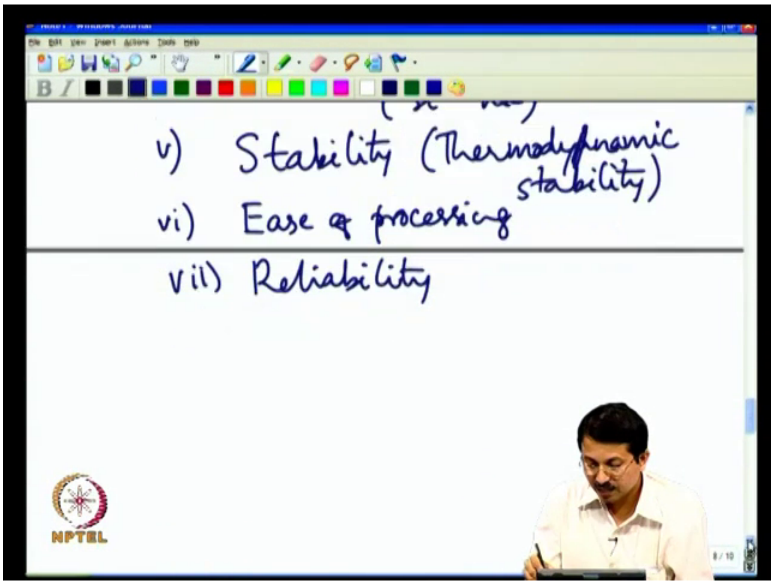

Stability; we sometime call it thermodynamics stability; what we mean by this is the following. Remember after you do your gate oxide you do various other processes you see and those are all high temperature processes.

You may have gotten a very good high k material, but subsequently can it withstand all other high temperature processes or whether it starts disintegrating right. So, that is a very important consideration and then if you can do all this then you ease of processing how do you process it I mean are there process techniques available, to put this di high k dielectric on top of silicon because in case of silicon ox silicon oxide it was very easy expose silicon to high temperature to oxygen ambient you get silicon oxide, but how complex are these new processes and then of course, one last, but not the least is reliability.

Remember we talked about the time dependent dielectric breakdown and all that you have made a high k dielectric with all these properties, but is it going to sustain the operating electric field over 1 year 10 year or what have you we need to meet all these requirements only then you can build you can replace silicon oxide with high k gate dielectric.

You may be surprised that the research on high k gate dielectric is at three decades old, people have being looking at alternate materials to replace silicon oxide for last 30 years and it is very recently just about 5 years ago that we were successfully able to replace silicon oxide with hafnium oxide. Now most of the state of the art manufacturing technology all the chips that are made are not made on silicon oxide dielectric gate dielectric they are made with hafnium oxide, gate dielectric why did it take three decades to get to this point because of all these conflicting requirements, you may be able to satisfy one, but may not be able to satisfy others right.

So, why do you need large band gap? It is very obvious right the band gap when we are talking of band gap what we are saying here is that your silicon.

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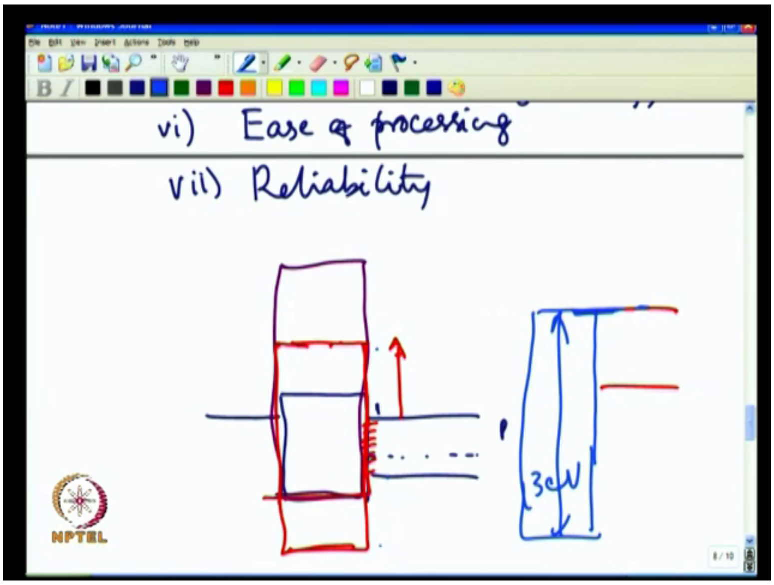

Which is one point one e v and let us say I build n channel transistor with polysilicon gate, the n plus polysilicon gate will have Fermi level here and this is a p type silicon which will have a Fermi level below the intrinsic level ok.

Now, you need to interpose an insulator here right. If this insulator were to have a very very low band gap remember this off set is important because that will determine what is your tunneling current. Let alone direct tunneling you would not follow what I am tunneling remember of course, direct tunneling may not be there, because we are making a thicker film because k is large you see, but if this off set is small the Fowler-Nordheim tunneling has a one very important factor in exponential term that is barrier height, and in silicon oxide I have a barrier height of 3 electron volt here for electrons, about 4 electron volt for holes.

So, what we are saying is that we need to have a new material, which has a reasonable band gap also band off set I do not want all band off set to appear for electrons and no band off set to appear for holes that is not good it is good for n channel transistor electrons cant tunnel, but your t channel transistor holts can easily tunnel through you see. So, that is why we say not just large band gap, but also reasonable band off set in other words. If you are looking at two situation where in both have same band gap let us say this is one case, this is some band gap x. And there is another material which gives the same band gap, but this material has quite a good band off set, but both electrons and holes whereas, this material has good off set for electron, but it is very crappy for holes.

So, your p channel will not work. So, that is why we had this two requirement going together large band gap along with that band off set for conduction and valence band; excellent interface is obvious because these are the interface states you want to make that the interface states are as low as possible. Stability as I mentioned all the subsequent high temperature processes it should withstand ease of processing is obviously important in terms of manufacturability and reliability is also very important right and this is why you know you should look at some candidates.

I will illustrate that too through maybe this example here look at TIO 2 very nice k 80 to 170 high k, but band off set for electrons is good band gap is good or reasonably good, but band off set for electrons is 0, that is in other words what it means is that for TIO 2 if you have silicon here, if you make a TIO 2 on top of silicon then TIO 2 will look something like this TIO 2 has a band gap of three electron volt, but it has zero band off set with respect to conduction band of silicon that is not a good thing that as I say you need to have a band off set for conduction band, band off set for valence band.

So, in spite of the fact that it has such a high k its of you know no use really for us whereas, silicon nitrate it has a nice band gap good band off set for both electrons and holes I have not listed the valance band off set, but k is marginally higher than oxide. So, that is why we did not really spent too much effort in silicon nitrate, because even if you go there maybe after two generation you will have to replace silicon nitrate.

Again most of the metal oxides these are all metal oxides, have reasonable k values depending on which oxides that you are look at you know aluminum oxide of the order of 10 hafnium oxide anywhere between 15 to 30, zirconium oxide 12 to 16. The variation depends on how did you prepare that oxide, you know it could be varying depending on that condition. There are clause of oxide called rare earth oxides she is represented as ReO 2 rare earth family is in periodic table if you recall such as erbium, erbium oxide or gadolinium oxide right all these are essentially your rear earth oxides. So, there are lot of candidates.

So, has to really look at all the requirements and as I have already mentioned today this this is already being used in sub 65 nanometer technology, we are already using hafnium oxide gate dielectric. Only then we are able to get E O T of less than one nanometer I could not have your silicon oxide less than one nanometer because I am doing this you see what is this essentially telling you is the following right.

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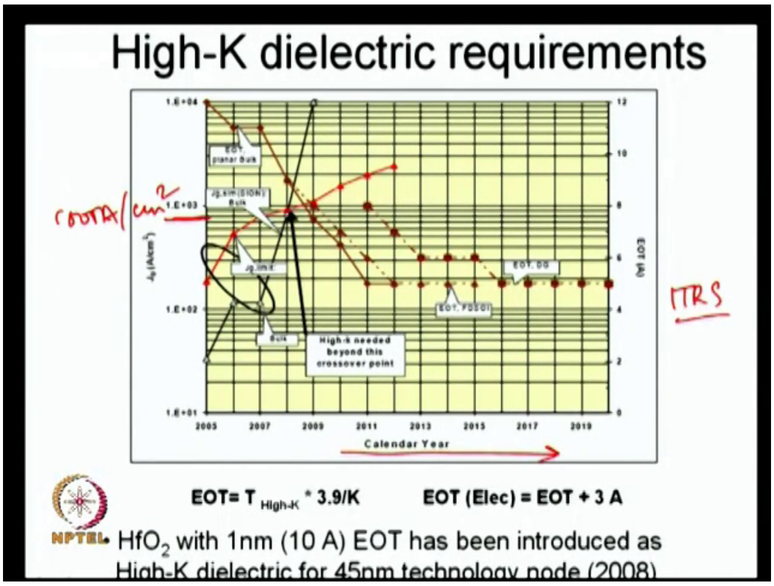

This is a calendar year this is taken from ITRS road map that we talked about in one of the and this here you know you what you have here is called J g limit, J g here is given as ampere per centimeter square I told you that one e 10 to the 3 is 1000 ampere per centimeter square, that is what we discussed a while ago 1803.

Now you know the J g limit could be different depending on which technology you are looking at, older generation technology you may have more stringent newer generation technology because your sub threshold leakage itself is increasing, you can effort to have little more gate leakage current also. So, what this is showing here is a J g limit how it is being altered over generations.

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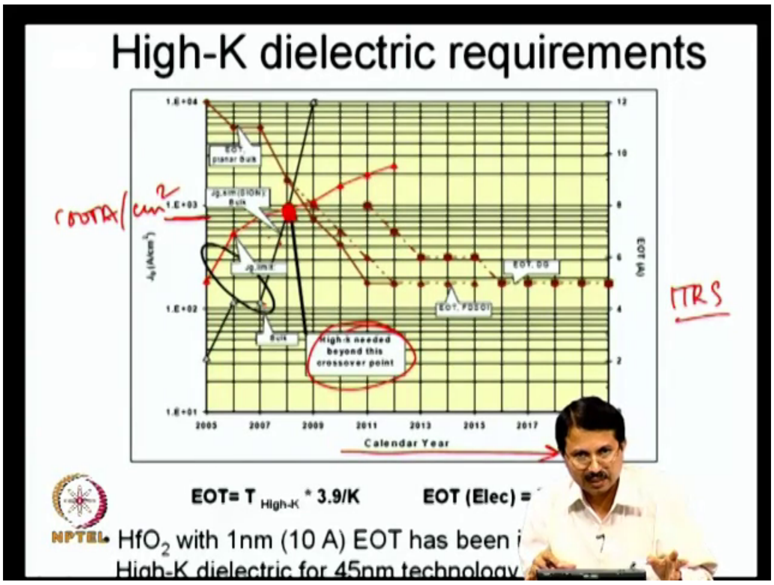

For different kinds of technology this is called bulk technology this is you know now what is also plotted here is that this here transition point, what it is telling you that in a bulk cmos technology as I am going along the calendar year I am shrinking my gate length. And hence I have to shrink my gate oxide that is when the gate leakage is increasing exponentially. And when the gate leakage hits this limit beyond that I cannot use silicon oxide meaning of this graph and that is when it is says high k needed beyond this cross over point that is when you must replace this silicon oxide with a high k gate dielectric right.

So, it is the same thing that is depicted in a slightly different fashion here.

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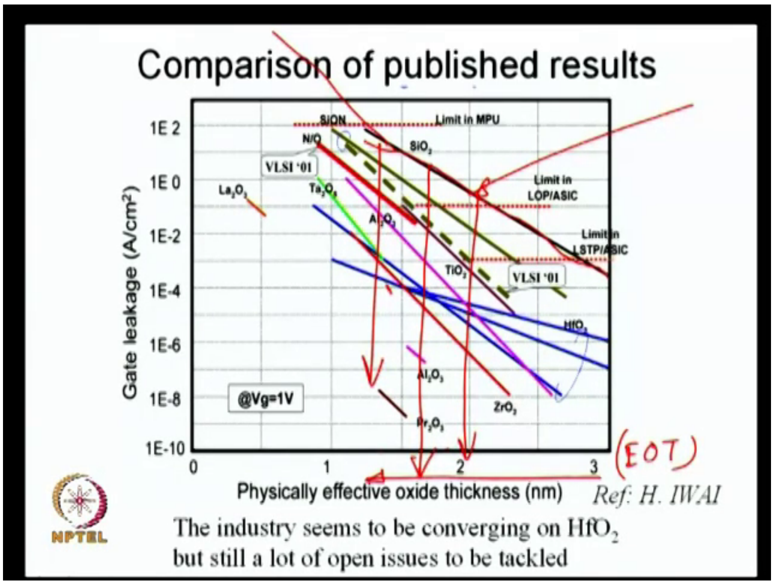

Now, what is shown here is a very interesting graph right based on various data reported in the literature, on x axis I have physical thickness right E O T right in case of silicon oxide it is really physical thickness, but in case of high k it is an E O T value. So, this what I am plotting here is E O T. If you continue to use silicon oxide as I decrease gate oxide thickness this current increases exponentially and you know go over this is 100 ampere per centimeter square this is 1000 ampere per centimeter square you are above the leakage speck when I go to different materials right.

Such as hafnium oxide is here, zirconium here, proscenium oxide, aluminum oxide this is from various groups in literature, but in all these cases for the same E O T you are able to bring down the leakage current at any given point that is the idea. So, I am still at the same E O T as if I am using Si O 2 of that thickness, but I can have maybe few orders of magnitude lower leakage current because I am using a new insulator.

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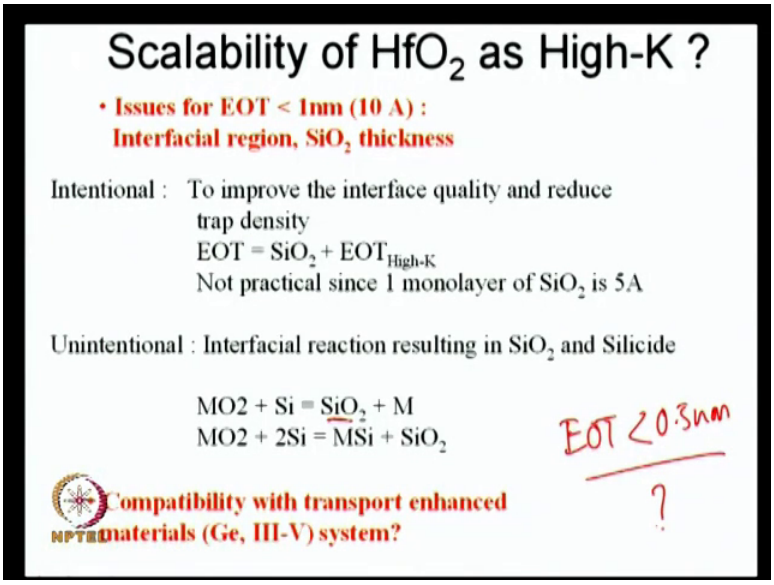

Well, it is not clear whether hafnium oxide which we are using now is scalable you know in the next 5 to 10 years because in the next 5 to 10 years.

We may have to reach a E O T of 0.1 nanometer per less than 0.5 nanometer, that is very very thin E O T value the problem is twofold right because whenever to try to put high k on top of silicon invariably you end up having a very thin silicon oxide either intentionally or unintentionally, sometimes intentionally because if you have a very thin silicon oxide you get a very nice interface. Remember silicon oxide has that excellent property of minimizing the traps right as we have discussed right.

So, that can happen intentionally by growing it less than a nanometer kind of a thing or unintentionally sometime because sometimes you may have a interfacial reaction subsequently, if it is not very stable during high temperature processes. The metal oxide in general some m o two can react with silicon and can give Si O 2 and m or it could also form silicide, which is not a good thing right. So, there is a practical problem especially to get for E O T less than 0.5 nanometer can we do that I think jury is still out there.

I mean we do not know that we will have to wait and see what could happen or whether there are alternate materials.

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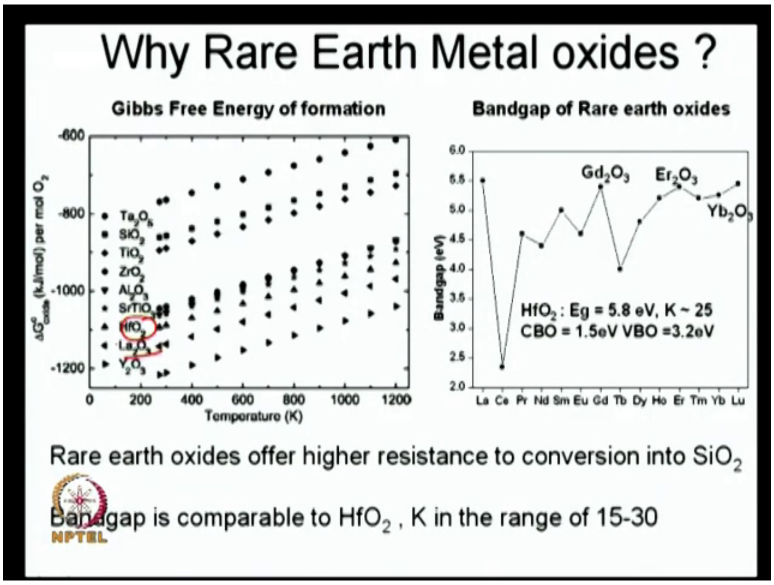

You see there are lot of efforts that are still ongoing you know especially there are these so called rare earth materials such as lanthanum oxide which is illustrated here, you know what is shown here is that this is so called Gibbs free energy of formation what it means is that it just indicates how stable is this oxide for subsequent thermal processing the lower the better.

If the lower this is more stable it is it would not react with the silicon to form a artificial layer and some of these rare earth metal oxides also have reasonable band gap. So, a lot of work going on oxide such as lanthanum oxide, erbium oxide gadolinium oxide to see whether these oxide can replace hafnium oxide in the next few years.

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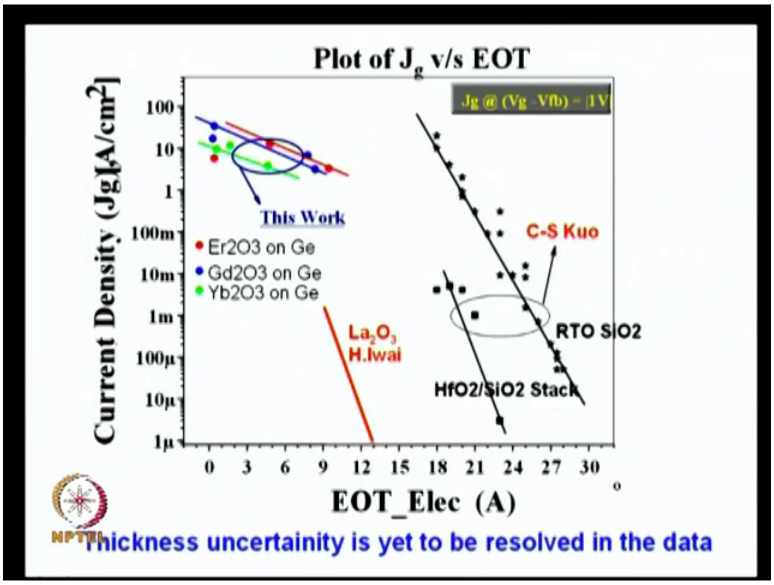

But this is a very interesting evolving area at present we do not know what will happen later.

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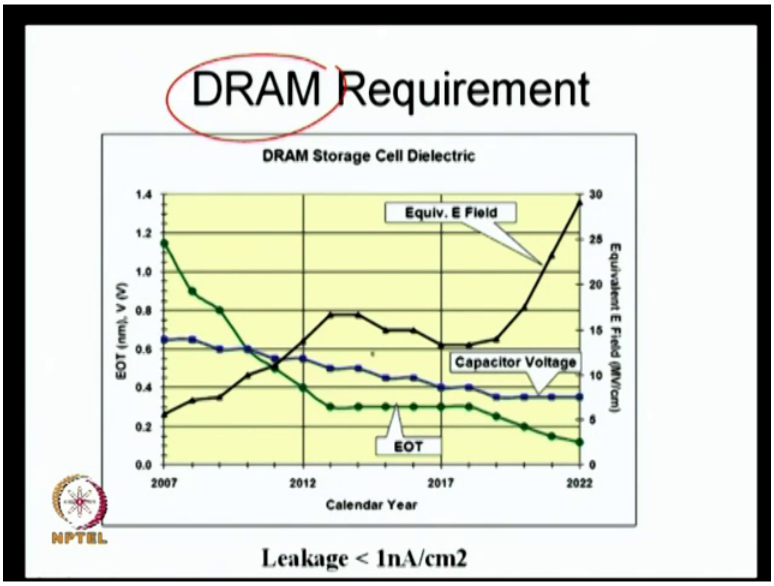

In the context of high k gate dielectric, I may also bring up towards the end of the lecture now in next 5 minutes or so, that there is another place where high k gate dielectrics are required those are to build dynamic random access memories. If you have studied dram at some point in time dram is the simplest memory cell you can imagine all that we have is at every memory cell, memory cell you know is a two dimension array of pixels at each pixel. We have a control transistor and a storage knob or a C storage.

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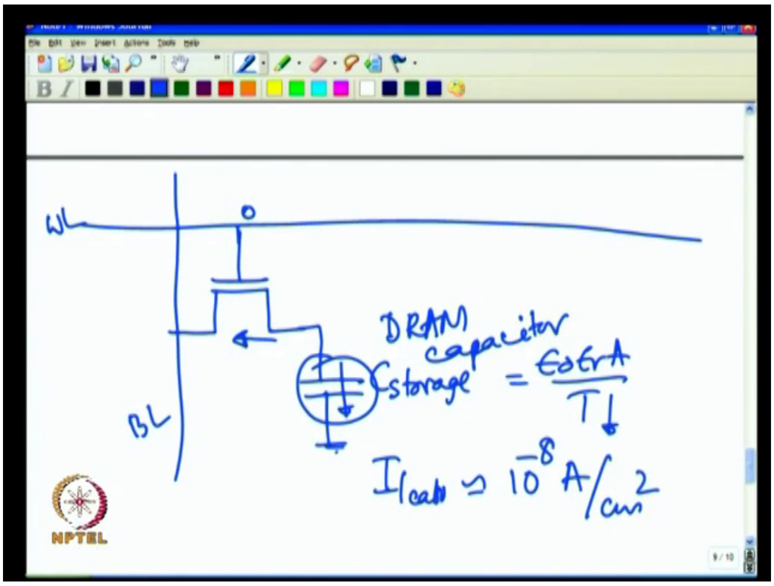

This is also called dram capacitor, this is what typically is called your word line of the memory and this is what is called a bit line of your memory correct your memory is essentially a two dimensional array of word lines and bit lines, bit line is where you read out the data word line is where you apply the control signal to read a particular bit from the memory array. So, the way it would work is that this is the most compact memory cell you can ever imagine, ok.

Although in the recent days there are few very interesting memories that are emerging to replace and to miniaturize the memories further in future, but currently if you were to compare drams static rams and flash memories drams are the most compact that is why your you know storage the higher storage, that you have in computer apart from the hard disk is essentially drams because you can build very high density memory using drams. You store a charge here and whether you have stored a charge or not stored the charge that is your logic one and logic 0.

When you store a charge this charge, it should not leak out if you have stored one, but in drams there is this problem of leakage, leakage is either due to sub threshold leakage now it becomes very clear for you otherwise you might ask if I apply zero why should the try let us charge leak, but there is always a sub threshold leakage current you see and that can leak the charge and similarly you can have junction leakage and so on and so forth and that is why in drams there is something called refreshing whenever you read data from dram you should also refresh that you rewrite that and even if you do not read the data you will to refresh it quite often you need to minimize the refresh time you need to minimize refresh cycles. The way to do that is to store as much charge as possible and hence I need to have as large capacitance as possible and capacitance being epsilon naught epsilon r A by T you can certainly scale T.

But you cannot scale T very significantly because again you have leakage current in addition to this transistor leakage current, you can have a dielectric leakage current just like any dielectric you have Fowler-Nordheim tunneling and direct leakage tunneling and leakage current specks in drams are several orders magnitude stringent compare to leakage current specks through gate oxide capacitor in high performance transistor.

For example the dram leakage current speck through this capacitor is of the order of 10 to the minus 8 ampere per centimeter square. Compare and contrast this with the gate oxide leakage current speck of thousand ampere per centimeter square that we are talking about. So, here the problem is even more severe I really need to make sure that I make it really thick reasonably thick. So, that my leakage current is well within this speck and hence if I need very large capacitance I need even higher k values, whereas hafnium oxide with k of 15 16 20 may be for your transistor for dram you may need k of 50 100; so again in dram.

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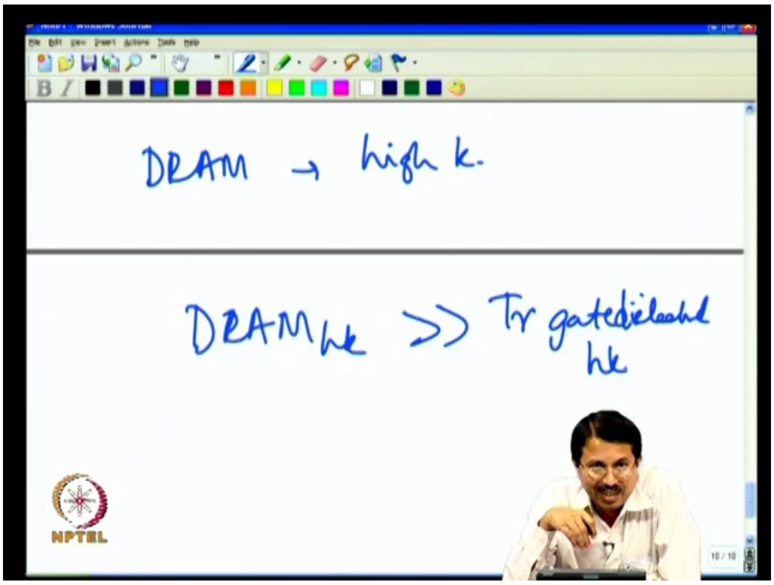

You need high k, such that your dram high k should be much much higher typically than your transistor gate high gate oxide or gate dielectric high k value, because the leakage current speck here is very very stringent compare to the leakage current speck here, but there is also one saving grace here although its more stringent in terms of the leakage current specification.

Remember that when you build a dram capacitor we are not really necessarily looking at an any interface with silicon, because this is a completely different beast here there is no current flowing under this capacitor right, whereas here.

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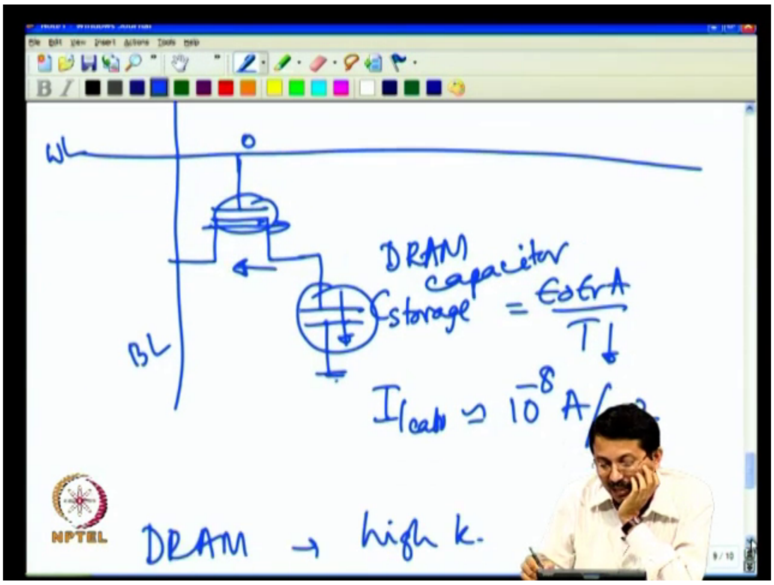

Under this gate oxide capacitor there is a current flowing from source to the drain. And hence you also need to have an extremely good mobility here extremely good interface at least that is not a very serious constraint here and that is why typically the dram capacitors high k capacitors are.

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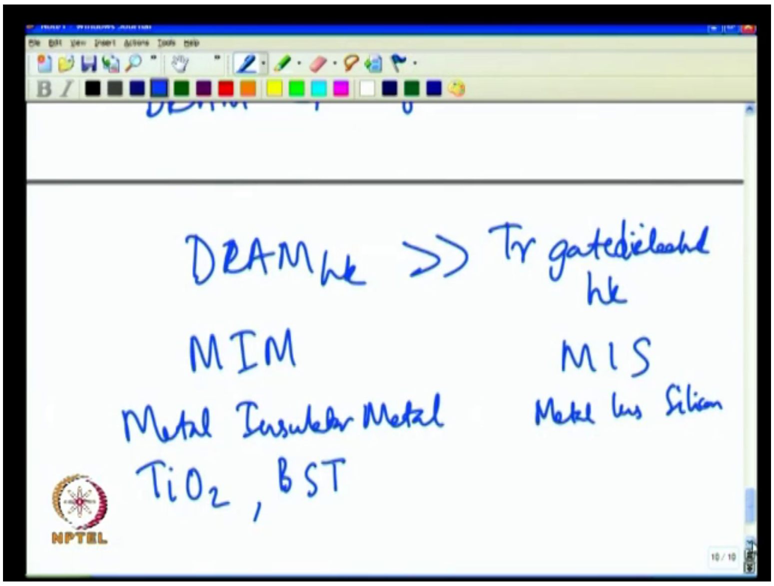

What we call MIM capacitor which is metal insulator and metal capacitor, as oppose to the transistor which is MIS capacitor, which is metal insulator and silicon or semi-conductor in general, but in this case silicon right both.

Are high k material in one case it happens to be part of a transistor and hence you have metal insulator and silicon, whereas here you have metal insulator and metal because it is only a capacitor to do a high k dielectric and storage and that is why you know here various other materials are really being looked at such as for example, you know TIO 2 and some material called BST, which stands for barium strontium titanate all these have huge k values like 100 150, whereas here I do not need to go to 100 150 you know beyond certain limit there is no need to increase k value in a transistor structure that is another very important point that I want to bring up here, if you are looking at transistor structure.

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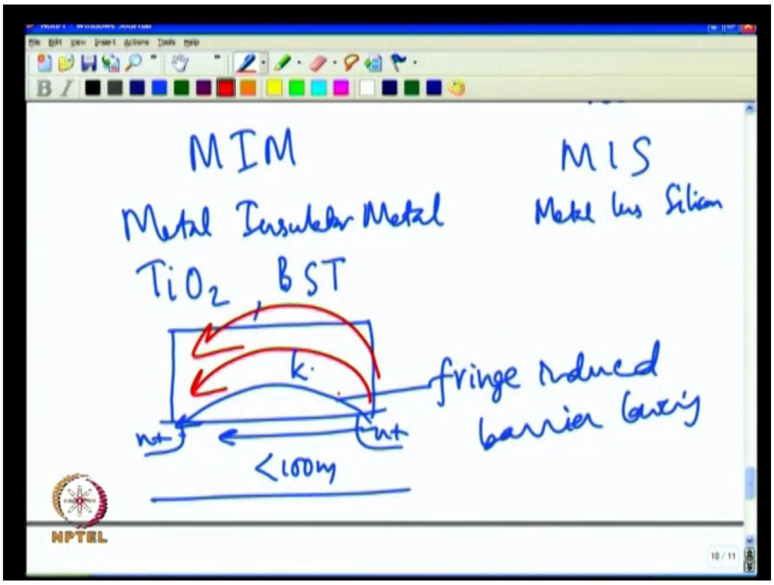

What is the advantage of using a very high k, I can make it very thick you see isn't it if the k is low I have to make it much thinner.

So, if you have a very high k, you remember this is a huge k value then in a very short channel transistor less than 100 nanometer. Remember we talked about drain induced barrier lowering that drain electric field coupling directly to the source. Similarly when you have a high k material here and huge opening, to speak you can really have what is called fringe induced barrier lowering, what it means is that there is a fringing field and that fielding fringing can start becoming more and more powerful as your k value starts increasing more and more. So, the message is the following we need to first recognize why are we increasing the k in the very first place.

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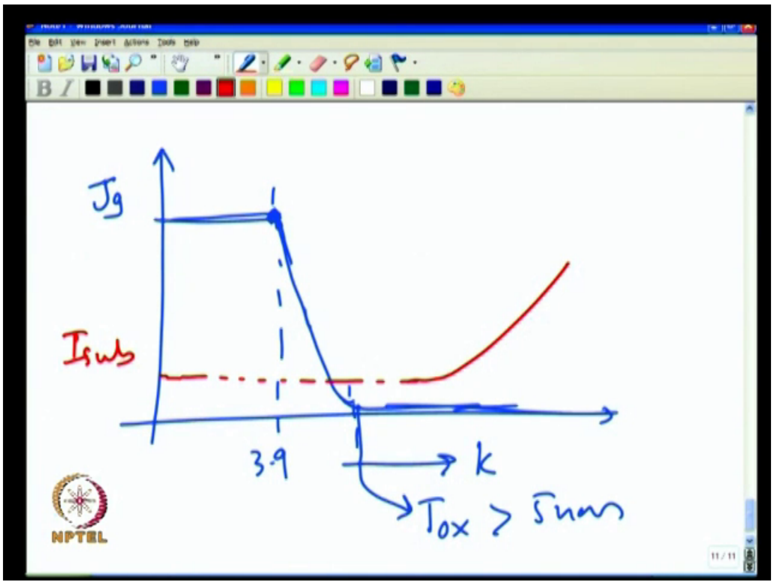

In the very first place we are increasing k remember 3.9 k is silicon oxide, silicon oxide has a high leakage current here this is the point. By increasing k value you can make thicker insulator, but as soon as you reach a thickness of 5 nanometer or so, your direct tunneling current is just suppressed completely, beyond that increasing the thickness has absolutely no value for you right. In other words if you were to look at this decrease in leakage current what happens is that it just gets spread here at some k value which corresponds to a thickness of 5 nanometer or more if you increase the k value.

And increase the thickness beyond 5 nanometer, you do not see any benefit on the other hand what could happen if you look at your sub threshold leakage. Now let us say I have some sub threshold leakage if I start increasing the k unnecessarily you do not gain in terms of any further reduction, but you may actually lose in terms of your sub threshold leakage starting to increase why could this happen? This could happen due to so called fringing field induced barrier lowering.

So, the message is that in transistor it does not help you to go beyond a certain k value just do whatever is required for you what is it that why are you doing it you are doing it to make J g 0. Once you get J g 0 do not overdo it if you overdo it you will essentially undo all the advantages. On the other hand for memories drams it helps you to get as high k value as possible because we are not really talking of a transistor structure there it is only an MIM structure ok.

So, let me then summarize direct tunneling is serious issue in today's technology unless we replace the silicon oxide with high k gate dielectrics we cannot build transistors today. And we have successfully done it below 65 nanometer regime, hafnium oxide has successfully been used, but it is not clear whether we can continue to use hafnium oxide. In the next 5 to 10 years, there may be other candidates as well drams also require high k gate dielectrics.

So, we will stop the lecture here.