

VLSI Data Conversion Circuits
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Lecture - 53
Optimal DAC Segmentation

This is VLSI Data Conversion Circuits lecture 53. In the last class we were discussing a various tradeoffs between binary and thermometer code at DACS or decoded DACS and we saw that when the INL is concerned it does not really matter whether you binarily decode the digital data and drive the elements of the DAC. Or if you thermometer decoding drive the elements because I_{n-1} which is the major of the deviation of the analog output from the ideal analog output alright depends only on the total number of elements which are on.

And whether the DAC is realized as a binary decoded version or thermometer decoded version the total amount of a current that is being generated which depends on the total strength of the elements being on remains the same. And therefore, it makes sense that the INL the worst case INL which happens at mid code is independent of whether you decode it either way. On the other hand the d_{n-1} which is a major of the deviation the step size from the ideal step size has a huge peak at mid code, when you do a binary decoding of the digital data alright.

And the reason for that huge peak is that when you get two the mid code transition of the DAC that is 0 followed by all ones to 1 followed by all 0's ideally the change in the output of the DAC must be simply one step. And unfortunately as we discussed the last time this one step is be being realized as the difference between two large numbers. And if there is error in each of these large numbers, it is a not all surprising that when you take the difference; the mean value of the difference is indeed one step as we want.

However, the variance of the step size is very large because the errors in these two large numbers are uncorrelated. And that definitely is not the case in the thermometer decoded version because to increase the output of the DAC by one step every time all that we are doing is add one extra element right which gives you that one step.

So, the variance of the step size is simply the variance of that individual step that we add and therefore, the DNL performance for the same variance of the individual step size.

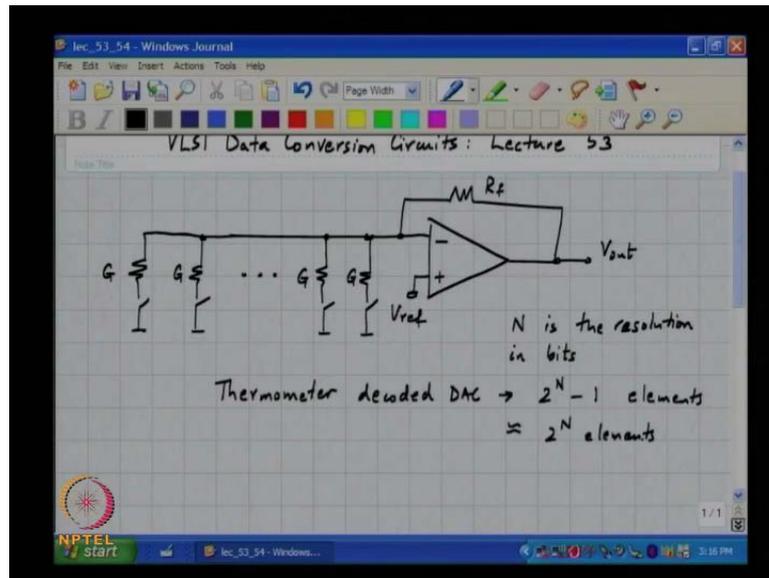
The variance when you of the DNL for a thermometer decoded version is much smaller than what one can achieve with purely binary decoding. Unfortunately when you decode the input data into a thermometer code the complexity of the logic becomes very, very high and it is exponentially related to the number of bits correct.

Because you know if you have a 2 to the 5 number of levels, which is the 5 bit converter converting from a binary to a thermometer code involves 5 input wires and about 32 output wires right. On the other hand if you have a 10 bit converter you have 10 input lines and 1024 output lines. So, you can see that the complexity of the decoding logic grows exponentially right and since the complexity of logic grows exponentially one can roughly say that the area occupied by the digital decoding portion.

Where also go up exponentially because I mean complexity wise we mean number of gates and if you have a larger number of gates presumably the area require to hold these larger number of gates on an IC will also increase; therefore, the area is exponentially related to the number of bits. Then we were wondering if there is not a middle path between 1 extreme where we have binary decoding which will make the decoder very easy and the matching requirements on the elements very hard right.

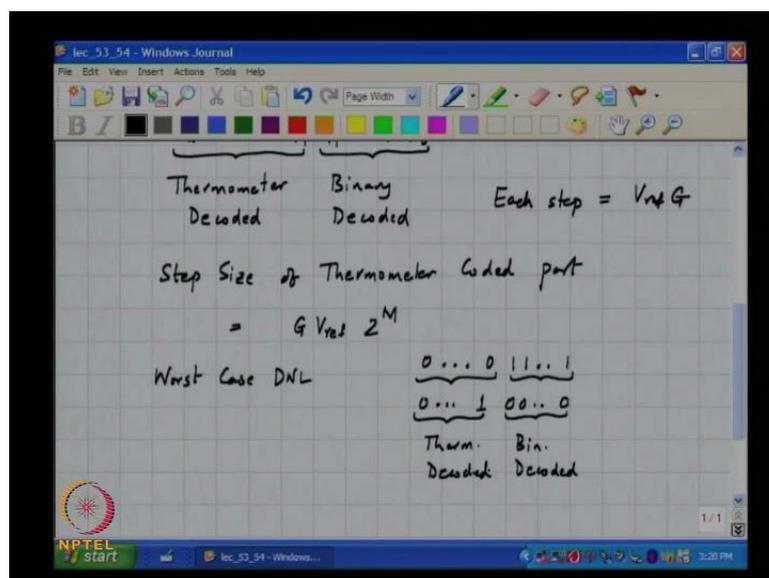
On the other extreme we have the thermometer decoding where the decoding becomes very hard and the matching requirements on the elements is quite relaxed. So, it is clear that if we kind of you know walk in the middle where we decode part of the input word through binary decoder. And the rest of it through thermometer decoder, then we most likely achieve complexity of the decoder which is manageable along with relaxed matching requirements on the individual elements of the DAC right.

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So, let us continue where we left of the example we were looking at is this the R F is simply a resistor which converts voltage to current this was say V ref. And we had conductances in this fashion each of them connected to ground and controlled by a bunch of switches. Now in the all thermometer case all these will have identical conductances and you will have roughly 2 to the N is the resolution of the DAC in bits. Then a full thermometer will have 2 to the N minus 1 elements for large N you can approximate this as 2 to the N elements right now.

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Let us say we want only to partially thermometer decode the input digital word is of the form $b_0 b_1 \dots b_{m-1} b_m \dots b_n$ this part is decoded in thermometer fashion. Whereas, so these are the b_n these are binary decoded the last time we saw why it make sense to decode the m s b's in a thermometer fashion rather than the l s b's. So, let us now try and figure out what the $d_n l$ is for this case you understand. So, what are the step sizes of the thermometer coded version let us assume each l s b is nominally V_{ref} times g .

It should be.

Student: 2 to power n minus times.

G times V_{ref} times 2 to the power m is that clear, see this will be l s b times 1 this will be l v s b times 2 this will be l s b raise to 2 to the m minus 1 right; which means that the l s b of the most significant portion of the digital word will be 2 to the m does it make sense all right now when do you think you will have the worst case $d_n l$.

Student: When b_n is 0 all other ones.

Pardon.

Student: Change to g

Student: D_m is equal to

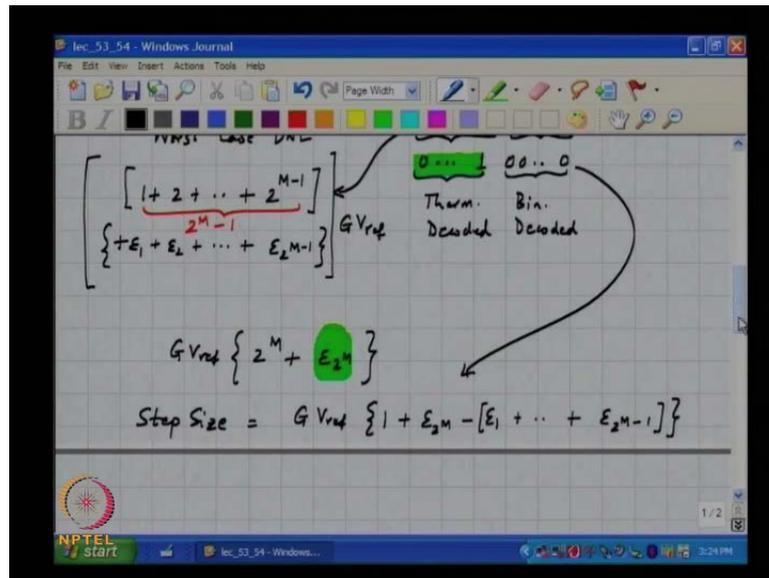
B_n or v_n or b_{m+1}

So, worst case DNL occurs when you have all 0 's followed by all ones and

Student: ((Refer Time: 12:20))

1 followed by all 0 alright. So, this is the binary decoded part and this is the thermometer decoded part let us now try and calculate what this worst case DNL is the analog output.

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In this case should be G times V ref which is the step size multiplied by.

Student: 1 ((Refer Time: 13:17))

1 plus 2 and so on all the way up to 2 raise to M minus 1 all right plus the errors involved in each 1 of these.

Student: Individual

Individual conductance's which is E 1 plus E 2 plus and so on E 2 to the M minus 1 times G times V ref all right; on the other hand the analog output here should simply be 2 to the.

Student: G ((Refer Time: 14:39)).

G times V ref times 2 raise to the M plus E of the 2 raise to the m alright. Now, can you comment about these errors and these errors are they correlated or are they not correlated.

Student: They are not because there are from different sources.

These guys are coming from the binary code decoded version, these guys are coming from the thermometer DAC. So, they should be no correlation between the errors in the thermometer decoded portion and the binary decoded portion they are coming from

different elements. So, the step size therefore, will be the difference between the 2 analog outputs which will be.

Student: ((Refer Time: 15:59))

What is this character

Student: ((Refer Time: 16:03))

This is 2 to the M minus 1 all right and therefore, step size is G times V ref times 1 plus E 2 to the M minus E 1 up to E 2 to the M minus 1 alright.

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The screenshot shows a Windows Journal window with the following handwritten content:

$$\text{Step Size} = G V_{ref} \{1 + \epsilon_{2^M} - [\epsilon_1 + \dots + \epsilon_{2^{M-1}}]\}$$

$$\sigma_{DNL}^2 = \sigma_{\epsilon_{2^M}}^2 + \sigma_{\epsilon_1}^2 + \dots + \sigma_{\epsilon_{2^{M-1}}}^2$$

$$\sigma_{\epsilon_{2^k}}^2 = 2 \sigma_{\epsilon_1}^2, \dots, \sigma_{\epsilon_{2^{M-1}}}^2 = 2^{M-1} \sigma_{\epsilon_1}^2$$

$$\Rightarrow \sigma_{DNL}^2 = \sigma_{\epsilon_1}^2 + 2 \sigma_{\epsilon_1}^2 + 4 \sigma_{\epsilon_1}^2 + \dots + 2^M \sigma_{\epsilon_1}^2$$

The journal window also shows a toolbar with various drawing tools and a status bar at the bottom with the NPTEL logo and the text 'lec_53_54 - Windows...'.

So, the sigma D N L when normalized to the step size is simply.

Student: ((Refer Time: 16:54))

Is simply of the sigma square of the D N L is sigma square of E 2 to the M plus sigma E 1 square and so on plus sigma E 2 to the M minus 1 square does it make sense alright; now let us recall the sigma E 2 square is what in terms of sigma E 1 square.

Student: 2 times.

Is 2 times sigma E 1 square and please note that sigma E 1 represents the standard deviation of.

Student: Single conductance

Of a single current or single the conductance in this particular case correct and you make larger G's by simply taking these unit g's and putting them in parallel if you want 2 G you put 2 G's in parallel; if you want 1024 G you take 1000 and 24 unit conductance's and put them in parallel. So, you can relate the sigma squares of all these elements using that is 2 to the M minus 1 times sigma E 1 square correct is this clear. So, therefore, which means sigma D N L square is simply sigma E 1 square plus 2 sigma E 1 square and so on plus 4 sigma E 1 square and so on up to.

Student: ((Refer Time: 19:32))

2 to the.

Student: M minus 1

Why 2 to the M minus 1.

Student: Because ((Refer Time: 19:41))

This goes all the way from E 1 to E 2 to the M.

Student: Minus 1.

Minus 1 and you have this term which is 2 to the M, so this must be therefore, 2 to the M times sigma E 1 square.

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Area

$$\sigma_{DNL}^2 \propto \frac{(2^{M+1} - 1)}{Area}$$

$$\sigma_{INL}^2 \propto \frac{1}{Area}$$

$$Area \propto \frac{(2^{M+1} - 1)}{\sigma_{DNL}^2} \times \frac{2^{M+1}}{\sigma_{DNL}}$$

$M = N \rightarrow$ Binary DAC
 $M = 0 \rightarrow$ Thermometer DAC

And this summation is approximately 2 to the M plus 1 sigma E 1 square strictly speaking it is 2 to the M plus 1.

Student: Minus 1

Minus 1, so if you want to be aspirating accurate all right please note that M stands for the numbers of bits being decoded in a.

Student: Binary.

Binary fashion alright, so once you need to check is to make sure that for M equal to 0 you must get.

Student: Variance single

The variance of a single element which is definitely what you are getting is it not. Now, to achieve a certain DNL please note that as designers we are interested in finding what levels of matching one must have in the unit element. In this case that single conductance G, in other words we are interested in what we should make sigma E 1 in order to achieve a desired sigma DNL right that is the design problem is this clear. So, the last time around we discussed how one was going to achieve a better sigma E 1 right.

Let us say you had some element a some conductance G with a sigma E 1 which is not which is way to high what could you do to improve sigma E 1.

Student: ((Refer Time: 22:19))

[FL] increase the area right. So, and finally, what how did we conclude if you want to increase sigma or decrease sigma by factor of 2 you have to increase sigma by.

Student: ((Refer Time: 22:35))

You would increase the area by 4. So, in other words you must bear in mind that sigma E 1 square is proportional to 1 by area alright. So, given a sigma DNL what will we do. So, in other words if sigma DNL is fixed from the specification then if M is fixed for a given resolution right. Then we need to go and figure out what sigma E 1 is all right and once we know what sigma E 1 is we can go and figure out how large we need to make the size of the unit conductance in this particular example; in order to achieve that sigma E 1 alright.

We still have not figure out though how one is going to choose M which is how we segment the DAC does it make sense alright. So, sigma E 1 square is proportional to 1 by area, so that could mean that sigma DNL square is proportional to 2^{m+1} times 1 by area and this 1 by area this area refers to the area of the E 1 itself does it make sense; now sigma INL on the other hand how does it depend on m.

Student: ((Refer Time: 25:17))

[FL]

It is independent of sigma.

Sigma I N L is independent of m, but is dependent on.

Student: Area

Area, so sigma INL square is also dependent on is proportional to 1 by area alright, one important thing to note is that as the degree of segmentation goes on reducing. In other words as M becomes larger and larger and goes towards N which will result in a fully.

Student: ((Refer Time: 26:05))

M equal to N is a binary DAC and M equal to 0 is a fully thermometer DAC as the segmentation becomes 0 in other words it is a fully binary DAC we see that the sigma

DNL square becomes very, very large or equivalently the area of the unit element required to achieve a given sigma D N L becomes 2 to the m plus 1 approximately divided by the desired sigma square you understand. So, let me put that down here, so the area desired is proportional to 2 to the m plus 1 minus 1 by sigma DNL square, which is approximately 2 to the m plus 1 by sigma DNL square.

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Area $\propto \frac{(2^{M+1} - 1)}{\sigma_{DNL}^2} \times \frac{2^{M+1}}{\sigma_{DNL}^2}$

Area $\propto \frac{1}{\sigma_{INL}^2}$

Total Area of the DAC
 = Area of unit elements \rightarrow
 + Area of decoder (digital)

On the other hand the area of the unit element has no relationship with the desired sigma INL square alright what are we trying to do now, so what we are trying to do is to figure out if there is a sweet spot with respect to choosing the degree with which one segments the DAC right and what I mean what is our objective function.

Student: ((Refer Time: 28:33))

Presumably the object function is to try and make sure that the DAC occupies as little as spaces possible to achieve a given sigma DNL and sigma INL right. So, as far as the user of the DAC is concerned he or she does not really care about what you do inside as long as the specs are met correct. And as far as D C performance is concerned the specs would be the sigma D N L and the sigma INL or in a more practical case the worst case DNL and the worst case INL and assuming everything is Gaussian and so on.

The worst case DNL and INL can be related to the sigma DNL and sigma INL right which means that you can always take the spec from which you can figure out what sigma DNL and what sigma INL you need to hit.

Now, given the sigma DNL and sigma INL I need to figure out what choice of segmentation will result in a DAC with the least amount of area why do I even believe that there is a there is an optimum.

Student: No because the area of the decoder increases when there is more thermometer.

Correct.

Student: Or else will you increase the binary portion the area of the current sources themselves they are increasing.

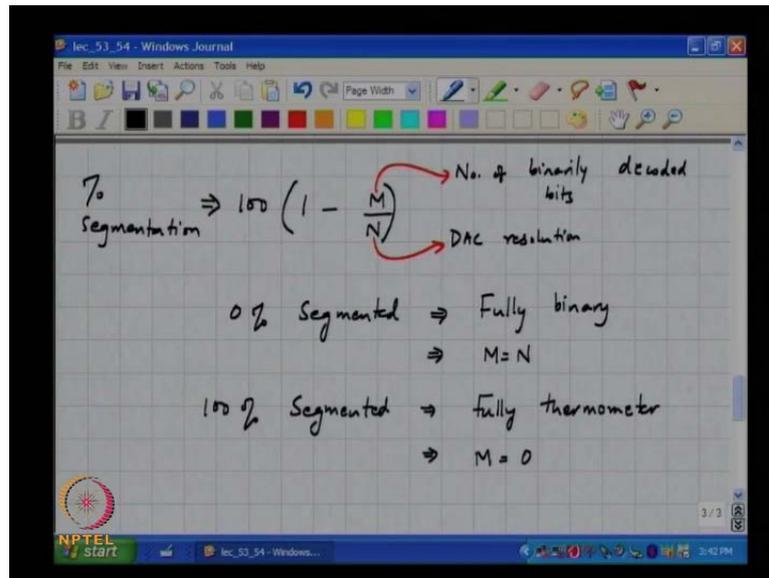
Ok.

Student: So, you have

So, that is a quite right we believe that there will be a sweet spot because if we choose a completely binary architecture the area of the current sources becomes very large right; because as we just saw there if the unit element is proportional to 2^{M+1} alright. On the other hand the area in total is given by; is the total area of the unit elements plus the area of the decoder. This is a digital circuit right, what is the area of the unit elements how many unit elements are there in an n bit DAC how many unit elements will be there.

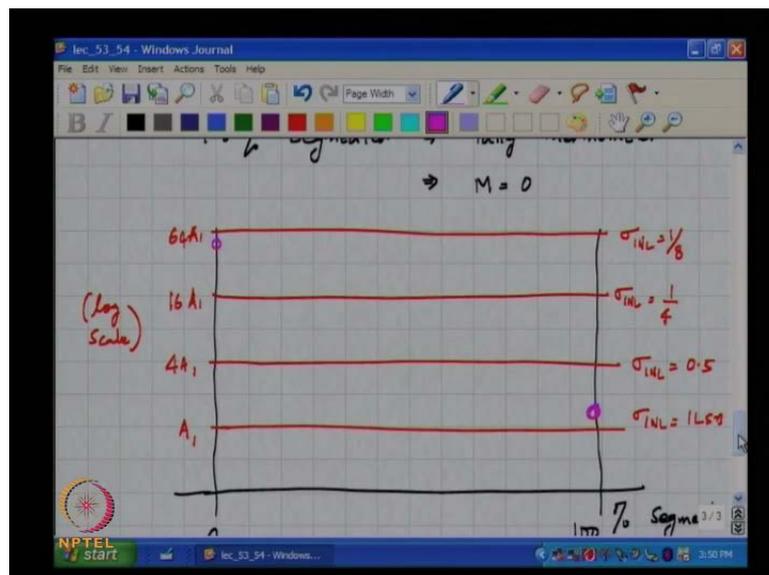
So, 2^n times the area where this a these two are the same all right plus area of the decoder. So, the area of the DAC can be roughly split up as some of the analog areas if you call these unit elements analog and the digital area where the digital area is simply the area of the decoding logic correct.

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Now, to make life simple let us define M by N, M is the number of binary decoded bits n is the DAC resolution. So, if you want to call 100 percent segmentation as a fully thermometer DAC then the percentage segmentation must be defined as 100 times 1 minus M by N right. So, if M equal to N you have 0 percent segmentation, so 0 percent segmented means it is fully binary. So, also means M equals N 100 percent segmented means as this is fully thermometer, which means m equal to 0 does it make sense.

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Now, let us plot the percentage of segmentation on the x axis this is 0 percent and this is 100 percent. So, this corresponds to a binary DAC this corresponds to a thermometer all right. So, to achieve a given sigma INL right let us plot the area of the unit element which also is the analog area to a within a constant please note that for a given resolution it is 2^N is a constant. So, the area of the unit element multiplied by some constant number gives you the total analog area.

So, to achieve a given INL right the degree of segmentation is of no consequence and therefore, given this one can go and find this you understand alright. Because, we saw in the in the last class that it is the sigma INL which is the worst at the which is the largest at the mid code right depending on whether you do N point INL or if you do best fit the constant of proportionality will change, but it will roughly be of the form square root of 2^N to the that sigma will be the sigma of the unit element times square root of 2^N .

And depending as I said last time around it will depend on whether you do end point or best fit or something, but whether you do I mean if you define it consistently the same way this is independent of the segmentation. Therefore, regardless of the segmentation the line the area required to achieve a given sigma INL remains constant right. So, let say let us for simply for argument sake say this corresponds to a sigma INL of a say I do not know 0.1 LSB is just an example.

In other words for in order to achieve a sigma INL of 0.1 LSB this is the amount of area required for the unit element which also is equivalent to saying this is the analog area required for all these elements in the DAC. Because, the analog area is simply the area of unit element multiplied by 2^N correct. Now, what can you say about a if I wanted for instance sigma I N L of 0.5 LSB what should happen to this line.

Student: Go down

The line should go down or go up

Student: Go down

Student: Go up

If you want sigma INL of what did I say point.

Student: 0.5.

0.5 I said 0.5 LSB is what I meant. So, if I want sigma INL 0.05 LSB the area must go up by a factor of 4 if I want the sigma INL to go down by further factor of 2 it should go up from this line by a factor of sixteen right. So, in other words a linear decrease in the INL should cause an exponential increase in the area right. So, if I plot this on the on a log scale you will keep this you will have equal spacing's right for example, let me just start off with more fine.

So, let us say this corresponded to sigma INL of say one LSB and this is some area a 1 let say this is this will correspond to a sigma INL of half LSB this is correspond to a sigma INL 1/8th 1/16 and so on right.

So, in this case this must be A this must be 4 A 1, 8 A 1, 16 A 1 and so on right. So, this is a log scale 1, 2 1 by 4 if I divided by that has to be 16.

Student: 16 A 1, 64 A 1.

So, 16 A 1 this must be 64 A 1 thank you alright. Now, let us see what happens to the DNL clearly to achieve a given sigma DNL the area must be a function of the percentage segmentation correct. So, for a given sigma DNL if I had some area needed for a fully thermometer decoded DAC right can you comment on what will happen when I go fully binary. In other words this represents the area needed for the unit element to achieve a given sigma DNL all right when the DAC is fully thermometer decoder.

Now, can you comment on what happens when the same DAC is realized as a fully binary decoded version what would the area required be It will increase and it will increase exponentially.

Student: 2 power

Because it is it is proportional to

Student: 2 to the power.

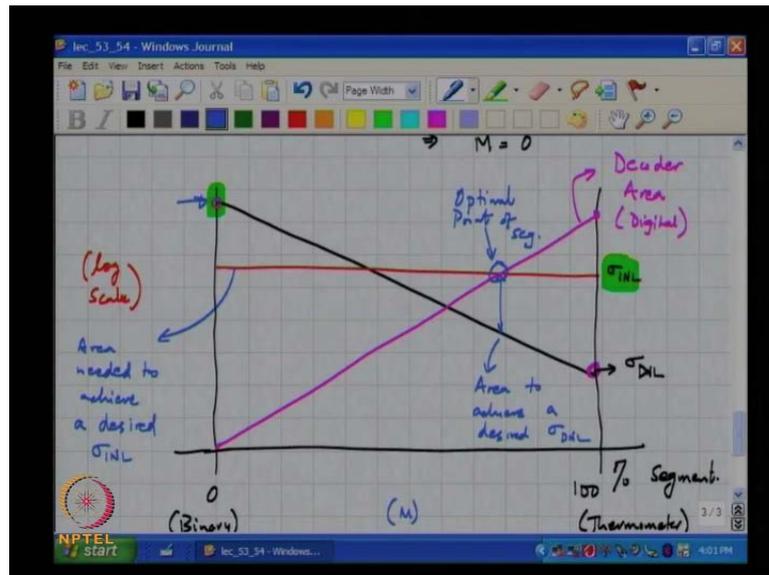
2 to the M plus 1 minus 1 which approximately 2 to the M plus 1 M equal to n when you want a fully binary DAC. So, you can expect the I am going to now erase off all these

lines only think you need to bear in mind is that this is a log scale correct, since the y is a log scale right and the x is.

Student: Linear

I mean linear in m

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It follows that this line will be a

Student: Straight line

Straight line does it make sense, so this is the area required for a given sigma DNL all right you understand. Now, the INL area will therefore, will be something like this right, so let me write some legends here alright, what can you say about the digital area required, the digital area is exponentially dependent on.

The number of thermometer bit thermometer bits, which means that this is also exponentially proportional to M, which means that how will that look like it will be a straight line going up. Now, you need some area minimum area for a binary decoded DAC and let us say this is the digital area required which is also exponentially proportional to whatever n minus M, M is a number of bits decoded binarily. So, n minus m is the number of bits decoded in a thermometer fashion the size of the digital logic is proportional to the number of bits decoded in a thermometer fashion.

As you mean that the binary portion is nothing right that part does not take any area the total area therefore, will be the some of the digital area and the analog area. So, if this was is sigma INL speck all right if we did a completely binary coded design we see that the amount of area required will be huge because the analog area occupied by all the shells will be very, very large right.

The digital stuff contributes nothing and we see that we are now way over design from the view point of INL why for desired INL sigma INL this is all the area you need to achieve the desired sigma INL. However, we have that area for the unit shell and the reason why we needed to have that much of an area for the unit shell was because we needed to hit the.

Student: sigma.

[FL] sigma DNL is this clear all right, then you say I am going to start segmenting and as I keep moving from here to the right we see that the area needed to achieve the sigma DNL keeps reducing right. At some point it will intersect the area needed to achieve the given sigma INL all right. And if I attempt to segment it further what happens the sigma D N L reduces but the I mean you will if I chose this area for instance I am as far as sigma DNL is concerned however sigma INL becomes a problem, so what should I do, I mean I should not fall below that red line. So, what I would do would be to keep increasing the segmentation until I hit.

Student: Sigma.

The sigma INL line and beyond that the total area is basically this plus the digital area which is going up exponentially; please realize that this is a I mean this is log scale right. So, there is gentle maximum I mean if you did look at the total area it is probably something like that all right and this line the position of this line depends on details of the technology and such all right because if within codes the logic is you know let us assume that is very, very small.

Then this line will move parallely down which means that if basically if the logic is very, very small it means that the decoding is free in which case you would do. If the decoding logic was magical it was possible to make it 0 area then what kind of segmentation would you choose, then you would a 100 percent thermometer right. So, the relative

position of this line is a function of a process and so on and feature size and this kind of stuff, but you can see that for a given technology you will be able find a sweet spot.

Around here there is hardly any difference between and whatever degree of segmentation you choose, because this is a is exponentially falling down correct. So, even though it is true that the area here is slightly greater than the area here that difference will be only very, very small, but the difference in performance will be I mean performance here versus performance here can you comment at A and B the INL is the same, but the degree of segmentation is higher at d than in.

So, what can you say about the performance at d the sigma DNL is clearly much smaller than the sigma DNL at A alright. So, it makes more sense to choose the more segmented solution right, so this is a optimal point of segment does it make sense is this clear alright, so we will stop.