Analog Circuits and Systems through SPICE Simulation

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Lecture – 49

Welcome back, let us resume our discussion on the digital modules for the single slope ADC. We have looked into the block level implementation of the control scheme for single slope ADC, the constituent building blocks and their functionality. Mainly the counter and some of the logic that is going to implement the phi 1 and phi 2 pulses. Next we will be looking into the transistor level implementation of the flip flops, which are constituent unit for the counter and also the gates.

So, digital design point of view of course, in digital design we expect that some of the libraries may be available to us. But when we are doing your custom mixed signal design of course, some of these digital blocks like the latches or the flip flops and logic gates need to be designed manually. And of course, there are some design considerations related to the digital units that we need to address at the transistor level.

So, let us look into those design issues and try to complete the discussion on the digital controller module.

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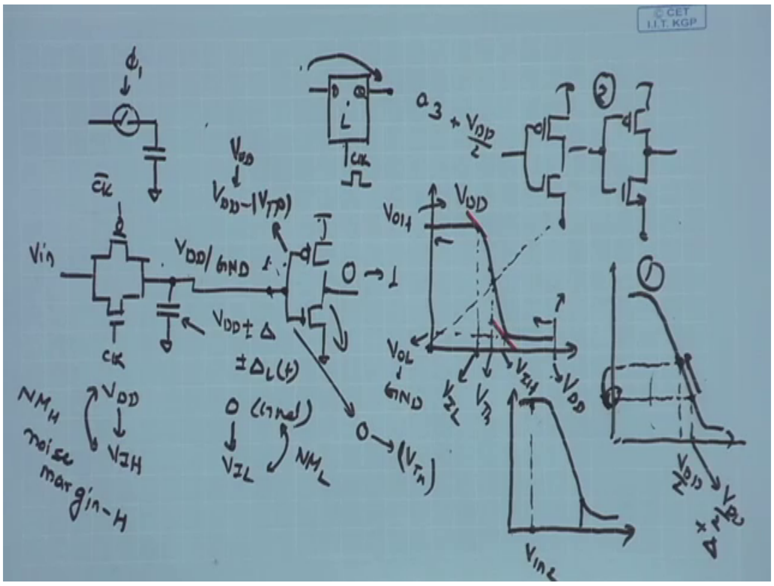

So, in the flip flop we have seen that the main operation that is going on is storage of data. So whenever there is the clock edge coming for latch; suppose this is the D latch; I am not drawing the triangle symbol over here; that means, this is a latch. Wherever the clock of the latch is high, the latch is transparent and whatever input is available it is transferred to the output. And when the latch is off or it means the clock is low the output value is retained; that means, when the latch is disconnected from the Q is disconnected from the D input, the output value over here, logic level over here is retained.

So, it is something analogous to the analog sampling that we have done. So, you have the phi 1 phase which is switching this switch on and under that condition the switch is transparent. Whatever analog value V is available, it is getting stored on the capacitor and after that when the phi 1 goes low and the phi 2 is on; this is disconnected, but this capacitor stores that charge, it retains the charge. So, it looks like this latch is doing function analogues to the sample and hold circuitry, but this is doing it in digital domain.

It is sampling the digital bit and storing it when the clock level is low and same thing the negative level sensitive latch, it does the same thing when the clock is low. So, it samples the digital data when the clock level is low and it is transparent during that phase it is tracking the data. So, if during the low phase of the clock the data changes; the output will also change. So, that is the negative level sensitive latch and when the clock goes high, again it becomes opaque and the data over here is supposed to be stored.

So, if we want to implement such a latch and hence the master slave configuration edge triggers; the flip flop; the simplest possible implementation would be something like this where you have a switch and a capacitor. Since this can store analog value, it can as well store digital value; if it is the transmission gate we can always expect that it can pass Vdd as well as ground reliably and we can have a capacitor over here and therefore, it can comfortably store the digital value as well; whether it is Vdd or ground. In fact, we are having less concerns about the non idealities of the switches like clock feed through, charge injection, leakage etcetera because here we are concerned with only two levels; you have Vdd and ground, we are not really looking for a precise analog level.

So, we can say that this is a very simple digital latch; you just have the transmission gates and you have the V in and you have the capacitor over here. And you have the clock and the clock bar, then this becomes simplest possible digital latch. This value may be relatively small, this capacitors may be relatively small because here we are not concerned with preserving 15 millivolt, 10 millivolt of accuracy. Here the voltage over here is supposed to be either Vdd or ground and we must make sure that the voltage over here does not leak in when the switch is open.

For example, when the switch is opened I would like to make sure that the Vdd or ground value stored over here; does not change significantly. What is that significant change for digital operation? Remember that is given by the trip point of the digital gates; the simplest digital gate being inverter right.

So, suppose this is connected to some digital gates; this digital logic values connected to some digital gates. So, simplest one will be an inverter; you can have many other gates or some logic which is using these value. So, yesterday we saw that in the final stage phi 1 implementation; we are using some logic to implement of phi 1. So, likewise you will have some gates or some logic circuits which are connected to the output of these latches. Suppose in this case we have an inverter and under what condition; under how much distortion or how much deviation in the stored charge or voltage over here can be tolerated by this inverter.

So, suppose the input was Vdd and as a result when the clock went high; this node was charged to Vdd. And as a result, I have the voltage the gate voltage of the inverter charged to Vdd. Now of course, you may have some leakage component, you may have clock speed through; as a result it may be, at the sampling instance itself it may be Vdd plus minus delta. And after that this is at t equal to 0 and after that you may have leakage component which is also going to be delta leakage the function of t. So, this voltage component may be time dependent, it will change this stored charge in a time dependent fashion; depending upon the leakage constituent of the different mosfets to which this voltage is connected.

So, this delta is coming at equal to 0; while sampling itself you have some error coming as we have seen because of clock feed through, charge injection etcetera. And then you have a time dependent component which can be because of leakage. So, as a result we may have overall change in the voltage over here; the function of time. How much change can be tolerated? We must make sure that the inverter over here is still reading the signal as Vdd and; that means, its output should be remaining 0, The moment this voltage suppose from Vdd drops down so much; that this inverter treats it as 0; then it will switch to 1, which is wrong value. And what can we say about how much error will be tolerated before the inverter flips its state. So, for that we have to look at the one again the trip point or the transfer characteristics of the inverter.

So, they are some important characteristics of this inverter transfer characteristics; we have the maximum level VOH of the inverter, when the logic level is high which is equal to Vdd. And we have the minimum level of the inverter, which is the VOL; output low, output H. And this is simply ground in case of a digital C mos inverter, we know where the maximum level is Vdd and the VOL minimum level is ground.

And here if we look at this slope region and try to make a tangent of minus 45 degree; the point after which the slope starts increasing becoming greater than 1; why greater than 1? Because, we have seen that in order to have a fast switching and regenerative operation of a chain of inverter, we need a slope greater than 1. If the slope is greater than 1; in that case even if you have signal over here which is not completely Vdd and ground, even if the signal is within the slope region; it can settle the value to high or low.

So, this is the discussion we had earlier that if you have a chain of inverter say to such inverters connected together in chain. And you have the signal over here which is somewhere Vdd by 2 plus say 0.5; 0.3 volt. So, slightly higher than Vdd by 2 and assume that the trip point of this inverter is close to Vdd by 2. We have seen how does the trip point depend upon device characteristics, but assume that the investor have been sized such that the trip point; that is a point at which V out equal to V in that is defined as a trip point; if you remember.

So, this is going to be the trip point of the inverter VTh or threshold of the inverter at which it flips the state. So, the trip point is inverter suppose it is Vdd by 2; the input level is only slightly higher Vdd by 2 plus 0.3 or maybe even lower 0.1, 0.2. So, that it is somewhere in this region and it is not completely Vdd. So, as long as the input is in this high slope region; we can make sure that in the next transition; if I just draw it slightly magnified fashion; I am just drawing that slope region in a magnified fashion.

So, as long as I have the input in this high slope region Vdd by 2; say the input is lying over here Vdd by 2 plus delta; that means, the resulting output will be here. As long as this is in the high slope region, where the slope is greater than 1; I can make sure that the output of this inverter will be sufficiently lower than the midpoint. Or in other words the output level produce by the first inverter will be closer to ground because looking at the slope is this slope is greater than 1 as compared to V out equal to V in point, this will be pulled down lower; if this is in high slope region. So; that means, that for the next inverter; output, the input point is closer to ground; further removed from the ground. Therefore, if I draw the characteristic for the next inverter, but what is happening; for the second inverter, this is inverter 1 and for the inverter 2; the input received will be this one; this Vdd by 2 plus delta was the input for the first inverter.

If I look at the transfer characteristic; it gives me the output value equal to this; the input was not completely Vdd or ground somewhere in between because of some error because of some leakage coming in suppose because of some circuit defect it was somewhere here; not completely ground, not completely Vdd which is not the right digital logic level. But it is in this high slope region, so now if it is in this region then we can say that because of the gain of the slope; the output point of the first inverter will be further lower than V optical to begin point. And as a result, for the second inverter; if I draw the characteristics, the input to that is; it is going to be further lowered. And as a result, you are having the input of the inverter is further lowered and as a result; we are having the V in 2 of the inverter; I can say this is inverter 2; V in 2 the inverter further at a lower point and if this is for the lower, it will make sure that the output is further closer to the higher level Vdd by 2.

So, if the input is lying in this high slope region; it will ultimately reach the higher level or the ground level because of the high gain in this region. And as a result, this is the transition region and if the input is lying anywhere in this transition region; we can easily conclude that the output will end up towards one of these two extremes; Vdd or ground depending upon at what point the input is lying; whether it is higher than this V optical to V in point or lower than this V optical to V in point. And likewise this trip point as we selected dependent upon the revise parameters, it is not very well defined. Of course, you can set it by sizing the kn, kp ratio; as we have seen the trip point depends upon the kn kp ratio and W by L sizing etcetera.

So, you can size that trip point and try to adjust it in device sizing, but always there is some uncertainty. And therefore, if the input signal is in this range you can have uncertainty that the final output can end up being wrong, it can go into the opposite direction as expected. So, for right or robust competition; if I take these two boundary points; the points on the characteristics where the slope is reaching 1 and after that you have a slope greater than 1; of course, this is minus 1, but in terms of magnitude the slope in this region is suppose greater than 1 and these points that is just 1.

And I can say that the input side; if the value of the input was supposed to be 0, but because of some error it increase and finally, reached this high gain region; then it can lead to flipping, it can lead to wrong evaluation at the output; right ideal value of low level was here, but because of some error in the previous stage, the output reached this particular point. And as a result, the next stage can end up interpreting this as high level rather than low and the inverter results can be different; it can be opposite of what is expected.

So, this can be treated as the upper limit for the logical low level. If the logic low level increases beyond this; we can say that it is violating the right logic operation and the next inverter can end up giving wrong result. So, I can call this as V I L; the maximum input level for logic low. If the logic over here was supposed to be 0 and the voltage initially the discharged to 0, but because of some error leakage etcetera the logic level increased all the way to VIL; beyond that the next thing water can end up treating this as high rather than low and then the inverter can trip, the result will be opposite as compared to what we expect.

So, this is the VIL point V input low likewise if the logic high level is supposed to be Vdd; this here on the X axis; this is the input of the inverter, the highest logic level Vdd is over here; this is Vdd. So, initially the logic stored over here is expected to be 1; that means this node is charged to Vdd. And then once again because of some leakage this voltage is dropping, it is dropping and approaching this particular point at which once again you are entering in the high gain region. So, we can say that this is the minimum voltage level which can be safely treated as the high level; below that once again you are entering the high gain region and as a result the output can flip. Therefore, I can call this as VIH; the minimum logic level for input high.

So, if the input level goes below that; the next inverter can treated as low level rather than high level. So, this is the definition of VIL, VIH, VOH and VOL for the digital inverter. Therefore, if we say that how much degradation the voltage level over here can tolerate so that the next inverter does not misinterpreted as the opposite level, so if this is Vdd how much leakage can be tolerated? What is the minimum value to which it can be allowed to go, because of leakage etcetera so that the next inverter keeps treating this as Vdd and it its output is staying at 0; so, that will be the VIH.

So, the output it can go from Vdd all the way to VIH till that point, the second inverter will still be treating this level as 1. So, we can say this is the noise margin; so, the starting point was Vdd, but even because of some disturbance, some leakage or noise; the voltage drops to VIH; till that point the second inverter will be treating this level as high level.

So, we can say you have this much noise margin for the digital high value. I can call this noise margin on the higher side NMH; noise margin, this is another very important quantity when we are looking at the transistor level design of digital logic gates; noise margin on the higher side NMH. Likewise, if you are looking at the opposite side; your input is supposed to be 0 or ground and you want to see, what is the maximum disturbance in this level; what is the maximum increase in this 0 level; that I have stored here, that can be tolerated by this inverter so that this inverter still treats it as logic 0 and does not flip to 0.

So, if this voltage increase too much as compared to the 0 because of some disturbance, leakage etcetera; then this inverter may end up flipping and it can end up treating this as high level rather than the originally sampled low level. So, what is that value once again you can see initial sampled value was 0, but if the 0 value increases to VIL and we enter into this high slope region; that means, the input value is higher than this VIL; that means, beyond this point once again we are not certain that the second inverter will treat this as 0; it can end up flipping because now the input has increased beyond VIL; now you are in the high gain region and once again you can end up flipping the inverter.

Therefore I can say the maximum value that I can tolerate is VIL and this can be once again treated as the noise margin NML; noise margin for the logic low level. So, although ideally; it should be 0, but because of say leakage, because of disturbances because of say noise from certain sources, you are ending up increasing this level up to VIL; even till VIL, the second inverter will be treating this level as logic low and therefore, we can say this is the noise margin for this inverter on the lower side.

Starting from an ideal value 0, but even because of some disturbance it goes all the way to VIL; this can still be regarded as logic low. Likewise, starting from Vdd, but it goes all the way to VIH; reduces all the way to VIH because of some reasons, still the subsequent logic gate will be treating this as logic high.

And in general; if you do the transistor sizing properly, this region can be made sharp in an inverter. It depends upon several factors; the sizes of the transistors as well as the load capacitance etcetera, but in general this slope region can be pretty sharp. And these two will be located close to Vdd and as a result, the noise margin best case noise margin can be at seen as Vdd by 2; if I size the transistor such that this VIH is Vdd by 2; the trip point of the inverter is Vdd by 2; if I can size the inverter such that this is achieved and VIL and VIH are also both close to Vdd by 2; this region is narrow.

In that case from the 0 level; the data can or the level can go all the way to Vdd by 2 while retaining the low level likewise from the higher level Vdd, it can go all the way to close to Vdd by 2 by still retaining the higher level. Of course, for more conservative analysis, you may keep some margin and you have of course, some finite slope and the worst case of slope can be great. Because of some reasons, if your P mos, N mos ratios are not properly matched or the load capacitance of the inverter is too much, you can end up having a different characteristics because of the mismatch or you know deviation in the transistor parameter like the V T or the W by N of n mos because as we have seen if you change the W by L of N mos, P mos; the characteristics can shift depending upon the drive capability of P mos or N mos.

So, in general those characteristics VT, W by L of these mosfets will affect this slope or affect this transition region and hence this slope can vary with the device parameters. And therefore, in order to keep sufficient margin of course, we will have some limit. So, maybe at least we can assume at least a couple of 100 millivolt on the upper side, couple of 100 millivolt on the lower side. So, definitely till couple of 100 millivolts; there is a sufficient tolerance till couple of 100 millivolts on both sides. For example, if I am looking at the high level over here; when this voltage is high; of course, we assume that this P mos is going to be off and this N mos is going to be completely on as a good switch.

But if the voltage over here starts dropping and we approach say Vdd minus mod VTP; then this P mos will be getting on; will start to get on and if it goes further high, then it will be also turning on more strongly and the N mos will be sorry; if it goes further low the P mos will be turning on more strongly; N mos will be turning off relatively strongly. As a result, you can end up inverting the state; so, crudely we can say also is from other perspective that the minimum degradation that you can obtain over here is going to be Vdd minus mod VTP.

So, initially if this was Vdd; I can go all the way to Vdd minus mod VTP before I can turn on the P mos. Because after that if you increase further this P mos will be turning on more strongly and N mos will be getting down; getting off. Likewise, on the other side if this level was initialized to ground and the N mos was off and the P mos was on and then I increase this all the way to VTN sorry; VTN as a result the N mos will start getting on; if I go beyond VTN p mos will become weaker and weaker and beyond this point once again the inverter can flip.

So, roughly we can also say that the VIL will be close to VTN of the N mos and VIH can be close to Vdd minus mod VTP of the P mos. Of course, they can be further lower means of course, this is not the exact transition point; it can be further lower, but roughly at least we can say that these are the VIH and VIL points. And if I look at the numbers that we have; Vdd equal to around 2 volt or 1.8 volt in our technology and VTP, VTN both around 0.4 volt. So, on the upper side I have the noise margin; I can go all the way to at least VTN on the lower side is 0.4 volt and right like just like that on the upper size VIH can go all the way to Vdd minus 0.4 volt.

So, if I take this definition for VIH and VIL; I have at least around VTN on this side and more VTP on margin on this side. So, I can tolerate few 100 millivolts of change in the logic level or the voltage level over here; while preserving the logic level. So, what we are trying to say is even though the voltage changes as compared to the original sample value by few hundreds of millivolt; that is your VTN or VTP, still the logic level is preserved. So, still the next logic gate is treating this as high. So, you can see this is the reason why digital circuits are much more robust as compared to analog circuits. Analog we have seen micro volt of noise can be problem, when you are processing the data at the front end; and we are very much concerned about the 1 upon f corner, white noise and so on.

But in digital circuit this noise margin phenomena; which is dictated by the transition of this inverter; that gives us a much wider room, it can tolerate much bigger noise even if the signal level is changing by few hundred millivolt; it is still safe the logic level is still preserved. This is an important point, important distinction between the analog operation and the digital operation. Because in digital operation, we are concerned only with logic high level or logic low level; the logic level are preserved even for such large deviations in the stored voltage. And that is the basic underlying point behind the robustness of C mos logic, robustness of digital logic.

So, in general for the digital logic; you can have Vdd which can be very noisy you can tolerate few tens of millivolts, even hundred millivolts of noise in the Vdd and ground. Whereas, in the analog circuit we cannot even tolerate millivolt; we have to make sure that the Vdd noise is lower than millivolt is very clean the microvolts of noise or disturbance. Whereas, in digital logic; you can have much bad supply, you can have much fluctuating voltages over here and here several hundred; few 10’s to 100 millivolt of noise is also ok.

So, this is also going to give us answer about the design of the digital sampling; how it is different from the analog sampling. So, when you are talking about analog sampling; this has to be very precise, we cannot even tolerate millivolt or drop as we have seen. But in digital case, we are much more relaxed; we are not even worried even have a 100 millivolt of drop and therefore, of course, we can see that we may not even need this sampling capacitor. We can just use the capacitance or the parasitic capacitance of the next gate for sampling the digital value because the voltage is so large and we are concerned with only Vdd or graph. So, we can take a short break and then resume our discussion on the transistor level implementation on the flip flop.