Analog Circuits and Systems through SPICE Simulation
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Lecture – 48
Control Scheme

Welcome back. Let us resume our discussion on the overall digital Control scheme that we have discussed.

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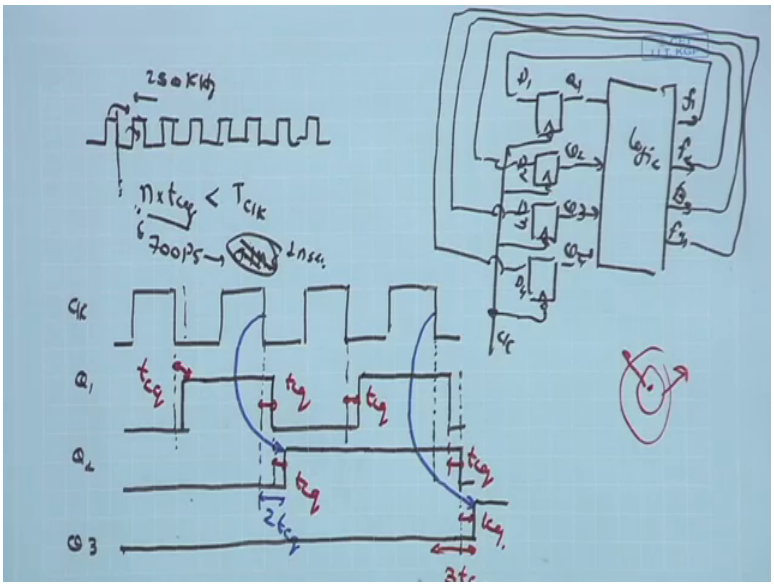

So far we have discussed the major component or the constituent of the control scheme which is our ripple counter. And based on that we need to realize our overall control phases or the pulses which is going into different modules like the comparator, the ramping circuitry, sampling circuitry, offset cancellation circuitry and so on. So, based on the operation of the ripple counter which is triggered by the main clock we need to generate the control phases.

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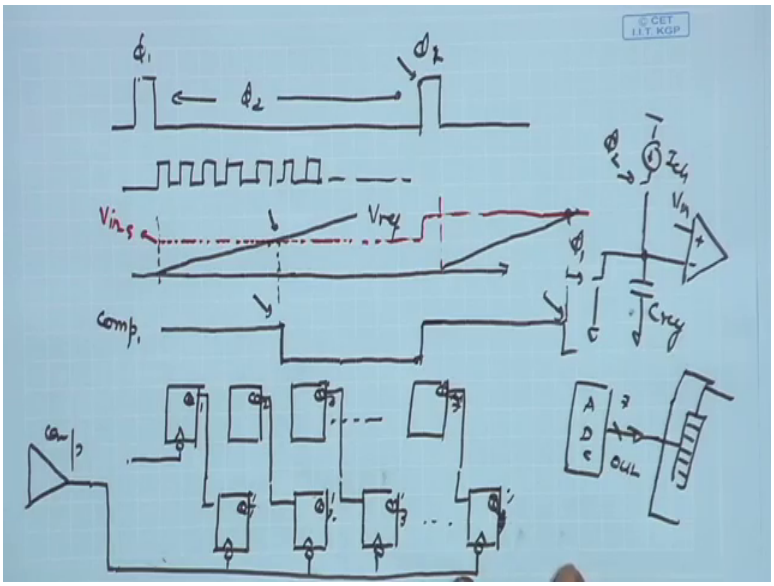

So, if I look at the waveform that we are going to require, once again reverting to our 2 phases phi 1 phi 2. And we are supposed to start the counting operation say at the negative phase of phi 1. So, you may have the counter getting started over here. And we expect that the ramping voltage is also going to start at the negative edge of the phi 1. So, you will have the V ref which is basically the voltage stored in the capacitor also ramping up at the at the phi 1 sorry if at the phi 1 phase. And finally, the point at which the V ref becomes equal to the sampled input which is your V sample or V in sample this is the red level do note is a level of the input data a very sample, and the instance where the V ref becomes equal to the V sampled I would like to have my transition.

So, at this point whether the comparator output will be changing. So, we expect that the compared output will be starting from high in the moment this transition occurs the compared output will be going long low.

Student: [FL].

And this is the point. Who is there? Who has been brought the food? Twice it has been announced in the class. Who is there? You notice is not visible? In the class it has been announced twice. Now let us continue the discussion, do not worry this will be you know, off the record. So, but you know this is not, if you are not taking seriously with these are your other classes are there, other people will be coming and if you are leaving these things behind, last several classes the same thing is happening, we have told you

before also, but again you are leaving the packets and all the food item on the chair. So, they do not, they are not supposed to do the cleaning for you, right? They are the staffs who are helping you in coordinating this lecture. It is not their form to clean for you. So, you are unnecessarily creating you know issues here ok.

So, let us resume our discussion. So, what I want is the comparator output will be going low at this point. And accordingly you will have the data or the counter output to be trans or the recorded registered at this point. So, whenever the comparator output is going down I would like the counter output to be registered as my final data for this particular conversion duration. And finally, at this instance once again I have to create the phi 1 pulse. So, these are the operation that I need to do I need to detect this transition time and at this point only whatever counter output is coming I need to latch it to circuitry or a latch which is storing my digital output for this conversion cycle. And then at the end once again I have to make sure that the phi 1 phase is going up. So, based on the counter scheme that we have how do we implement these operations.

So, let us see the first operation where we need to identify the transition point and make sure that the data is made available whatever counter output is available till this point it is transferred to a set of registers. And that is made available as the output digital word for this particular conversion cycle. So, this is one particular conversion cycle, after the phi 1 comes again next cycle begins. So, in this cycle the conversion is happening on the particular sample data that is available over here.

In the next cycle once again the sample data may change right. So, you have in the fight to phase a sample if I may change to a new value when you have some other V in and therefore, the conversion cycle will again become when the phi 1 goes low. And once again you will have the same slope for V rep time being at some point will meet. And once again you need to register the data. This is the overall operation. And for that I can use another set of flip flops, which are supposed to store the data or the counter output when this transition happens. And the control signal for that particular set of flip flop can come from the comparator. As you see the comparator output transitions over here from high to low and once again during the phi 1 phase when the data is getting sampled and the reference signal has been discharged to 0 it will be once again transitioning to low to high.

So, remember the comparator output it is remaining is going to remain 0 till the reference voltage is once again brought down, how does the reference voltage is brought down? We remember that we have a discharge switch also which is shorting the sampling or the c ref which is basically storing the sampling sorry the reference voltage. So, we have the reference c ref and of course, you have the I charge that we have implemented using current source. And you have the switch over here which is operated in phi 2 phase with charger this capacitor. And also whenever the phi 1 phase comes you have the other switch which is supposed to discharge this.

So, whenever phi 1 is coming over here the V ref is again discharged to 0, and as a result the comparator output will once again be turning high. Because this is 0 and V in rain of course, is going to be slightly higher than 0 minimum value will be V overdrive. So, we in will be slightly higher than 0, in this field as a result I can assume that the comparator will be making low to high transition back at this point. It will have some delay of course, the moment in the fight to face the moment this is discharged to 0 it will have some delay, but roughly in this period return comparator transitions again. And once again it will remain high for the entire duration, and once again in the next cycle whenever the capacitor voltage is crossing the sample voltage once again the competitor will be making a transition.

So, whenever the high to low transition in the comparator happens I would like to register or record the counter output. Therefore, I can have a set of flip flops which are taking the counter output as input data, and their clock can be said to the comparator output whenever comparator is transitioning from high to low. That negative edge should trigger the registering of the data or registering of the counter output into the other set of flip flops. That is the scheme I can implement. So, effectively if I try to see this you have the original counters flip flops. You have the original counter flip flops. I am not doing all the connections you have say Q 1 Q 2 Q 3 Q 4. And these outputs are available to you. In this case we have a ripple counter and therefore, the clock the main clock is coming only to the first one and we know that you have the connectivity from the Q 1 to the clock of the other ones and so on. And we have the comparator output. I can have another set of flip flops which are taking this flip flop outputs. And their clock once again negative edge triggered and their clock is coming from the comparator. And finally, I have a Q 1 dash Q 2 dash Q 3 dash Q and Q 7 dash 8 dash basically sorry 7. So, this is

the scheme that we are going to have and these are my final outputs Q 1 dash Q 2 dash Q 3 dash and Q 7 dash which is available as the digital word for that particular cycle.

So, in one conversion cycle these Q 1 dash to Q 7 dash will be changing their state only when the comparator is having high to low transition. And then it will be registering the data for that cycle. Next it will change only in the next conversion phase, in the next conversion cycle. And therefore, at the rising edge at the rising edge of the phi 1 I can use this data for my digital processing. Because just before the rising edge of the phi 1 I am entering into the just after that phi 1 phase I am entering into the next conversion cycles before that I can take this data stored in this register these 7 bits into my digital domain you will have another set of registers or you have you have some logic blocks in the digital domain which are going to use this data and process it further.

So, those digital blocks can be triggered with the positive edge of clock over here, and they will be taking the new output or the new digital word corresponding to the last conversion cycle, say at the positive edge of 500. So, the overall adc output available as the 7 bit word this is your output data and this denotes bits. So, then we have this cross denotes n number of bits if I denote this number; that means, 7 bit data, and that is going to the digital block where you can have the very first stage as another set of flip flops which are having 7 flip flops and all of them are triggered by the same clock, which is having a rising edge over here. Then onward it endures in the digital domain and rest of the processing happens in the digital domain you have a bunch of computation going on arithmetic computation and going on and all that processing going on over here. So, so this is regarding the registering of that data right. So, at what instance we are registering the return transferring into the digital domain.

Now, of course, the other thing we also need to look into is the generation of these phi 1 pulses from this original clock. So, in general as I said in the system you will have a single global clock and based on that clock you will be generating this phi 1 and phi 2 phases. So, how to use this single global clock generate this phi 1 and phi 2 phases. And also what do we need to do to this counter which is taking this main clock as the input. So, what happens to the Q 1 Q 2 could up to Q 7 when the final value say 1 1 1 is being reached, and then subsequent that how do we generate these 2 control pulses phi 1 and phi 2.

So, if we just go back to our original truth tables that we have.

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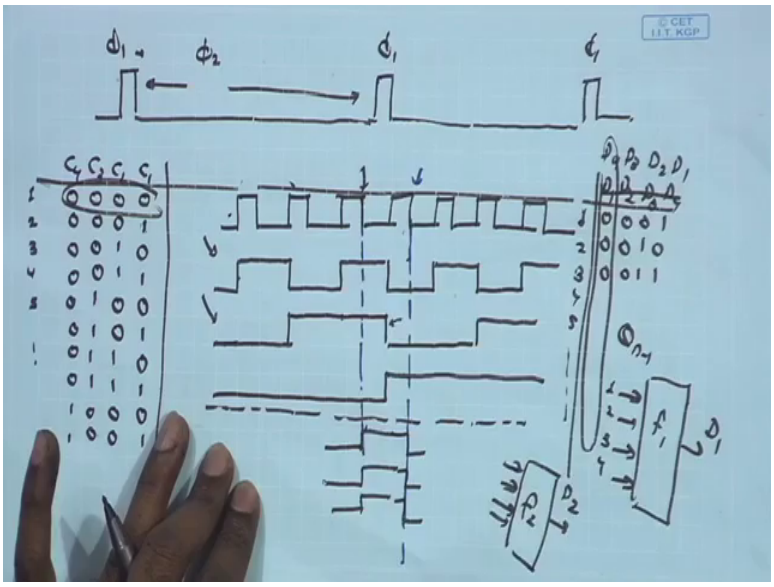

And if you look at Negative edge any instance where all the flip flops have been turned 1, suppose I am drawing an instance a particular negative edge closed after which all the outputs have been transitioned to 1. So, I mean just consider this as a separate case different from that is drawn in the above waveform is all the outputs have gone high at this positive edge, what happens at the sorry at this negative edge what happens? So, the outputs at the next negative edge, because we are following a sequence right. So, starting from 0 0 0 you have 1 0 then you have 0 1 then you have 1 1 and so on coming in. So, if I look at this waveform this is the sequence going to follow till the ms b 0 0 0 1 0 0 0 1 0. So, likewise 2 3 and one is going to increase and finally, all the bits will be becoming one there will be a clock cycle for which at the negative transition all the (Refer Time: 14:35) will be turning 1.

So, after that of course, what is the scenario all of them are going to toggle at the next positive edge simultaneously from 1 to 0, because at take before that edge all of them there 1 and at the next positive edge sorry at the next take it away all of them are supposed to toggle from 1 to 0. And therefore, at this instance all of them will be automatically transitioning to 0. And again the cycle will start all of them again getting reset to 0 after reaching 1 1 1 1 1 and again starting afresh from 0 0 0 0. That is automatically happening we do not need to apply any additional control to do that.

So, if you allow it to reach the maximum value 1 1 1 1 1 after that the next phase of course, all of them where one just before the negative edge over here immediately after that all of them will be transitioning to 0. So, this is the operation we expect. And therefore, if we simply allow the counter to run as if you simply allow these flip flops to keep running and keep counting till the maximum value 1 1 1 1 after that anyway all of them will be transferring to 0. And that is going to give me the control signal for phi 1. So, when should I set the phi 1 high. So, that should happen when once again all of these are making 1 to 0 transition and all of them have reached one and then they are making 0, once again I should activate phi 1 and start afresh. So, how can I do that?

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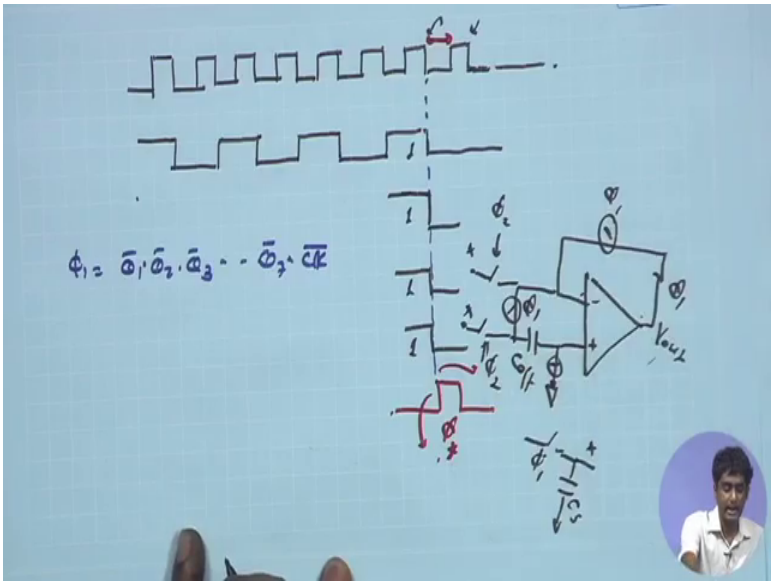

So, if I look at the waveform once again and this is the main clock, which is the high frequency clock, and these are the output of the flip flops individual flip flops. And the likewise you may be having any certain output. So, that at a certain instance you are having all of them turning to 0. So, you will have a certain instance where all of them are turning to 0 and so on. And this is the deviation at which the conversion cycle stops or end. So, here at this negative edge all of them after reaching 1 1 1 they are transitioning to 0 at the particular negative edge over here.

So, how do I generate the phi 2 pulse? So, here after the next negative edge over here once again I would like to start counting. So, we can have the phi 2 pulse for example, generated during the systems. And here what we can do is in order to generate the phi 2

pulse we cle see a clear logic what is the logic we need to implement. So, here the clock the main clock is low and all others are also low and therefore, simply using the and operation of all these Q 1 bar Q 2 bar Q 3 bar qn bar and the main clock bar I can generate phi 1 pulse.

So, whenever all of them have turned low and at the same time the clock is low I can use that as the phi 1 pulse. And so, therefore, if I use this logic this is nothing is, but phi 1 is equal to Q 1 bar dot Q 2 bar dot Q 3 bar Q 7 bar dot clk bar. So, whenever this logic is going high I can transition to the phi 1 phase. And during this phi 1 phase I should make sure that the sampling is happening properly the sampling speed is good enough switching the switches that your using in the sampling is able to charge a sampling capacitor at the same time you are having the discharge switch also phi 1. So, during that phi 1 phase we have to make sure that this switch is able to discharge the c ref during the sampling phase, we also have to make sure that the input data is getting sample appropriately on the sampling capacitor. And also we have the other circuitry where you have the offset cancellation going or a sampling of the offset going on the offset capacitor or c offset that we discussed yesterday. So, these 3 operations need to be finished within this phi 1 phase.

So, the c ref needs to be discharged the input data needs to be sampled and the offset of the amplifier also needs to be sampled on the c offset and all these 3 should be fast enough, So that they can be completed within this duration that is something we have to make sure and you might have noticed in the simulations also. So, the choice of the c ref over here and the corresponding switch dimensions over here become critical when we are trying to do the discharge operation.

So, this one is relatively simple this constraint of charge discharging this capacitor to ground is a relatively simple only thing you need to do is make this switch large enough, So that within the phi 1 duration it is comfortably able to discharge. If you make it minimum size and this capacitor is large say you know we have taken very large capacitor just to allow lower current if you remember sufficient current if you remember this capacitor reverse chosen has 20 pico farad around and therefore, if you use this minimum size switch the rc time constant may be too large. And it may not allow it to discharge completely to ground during the phi 1 phase.

So, all you need to do is make this switch large enough. Here of course, when we make the switch large we know that we have going to have leakage flowing through the switch and the leakage component can once again disturb the stored charge, but this is not a floating node you are having the current coming over here. And here we are not really even if you make this sufficiently large and during the off phase you are having some leakage component over here that leakage component also will vary as this voltage is changing, but that leakage component can be of the order of a few tens of nano ampere if I keep this leakage component sufficiently small as compared to the charging current say at least hundred nano ampere then still the slope not changed significantly.

So, there comes a trade off you have to be careful while designing this charging circuitry that we need to make the slope constant right and you do make a slope constant we are using this constant current source and we try to we try to we I am sorry. So, we looked at the constant current source and we try to keep this sufficiently large. So, that we are able to have a current of around point one micro ampere if we go for smaller capacitor in the current required will be further lower and it will be little less reliable. That was the reason by which you chose such a large capacitor of 20 pico farad. And if we choose a large capacitor we also need to choose a sufficiently large switch over here which is able to discharge that capacitor during that narrow phi 1 phase. And then we also going to have more leakage over here.

So, when phi 1 gets off that leakages again going to cause deviation from the required value and this leakage current is not constant as the voltage increases over here leakage will increase. As a result it can lead to non-linearity and as a result you can have some inaccuracies. So, you to make sure that if you are choosing a large capacitor corresponding to the large switch over here and then during the charge phase you are trying to charge with a small current the leakage is sufficiently small. So, it does not really make the slope deviate from the or constant value we want that is the concern you should take care of, but the here the simple thing is make the switch large enough. So, that the discharges pass during the narrow phi 1 phase make sure that during the off phase of this phi 1 or in phi 2 phase the leakage current through the switch is not too large. So, that it starts the voltage over here the slope of the voltage here starts deviating from the constant slope we want that is the caustic we should have for this case.

Of course for the other 2 circuitry the sampling circuitry we have to look at the sizing of the switches as we saw in the sampling circuitry the sampling switch size. So, determine the rc time constant and we calculated that the minimum size transistor was also expected reaching meeching meeting our rc time constant quite comfortably. So, there the switch sizing was not very critical provided we are using few pico farad of sampling capacitor.

And if you remember our circuitry for the offset cancellation there also we had the c offset which is supposed to be charged with the offset using the closed loop unity gain feedback. And during that duration once again the for the unity gain amplifier circuit the c offset acts like a load capacitor, and during that duration the unity gain amplifier should be able to charge that load capacitor. And another what is the transient response of the unity gain feedback should be fast enough, So that during that phi 1 phase it is able to charge the load capacitor or the c offset with the required offset voltage. And it is able to settle during the duration, that will require that the bandwidth of the bandwidth of the closed loop unity gain amplifier constructed with the same comparator is higher than the bandwidth given by this period. So, that is another constraint that we have. So, these are the issues we need to take care of while using this phi 2 phase.

So, basically we can just simply send this phi 2 phase to the phi 1 phase to the 3 switches that we have the discharge switch over here. The sampling switch and offset cancellation switch and of course, the phi 1 the phi 2 phase goes to the current charging switch over here current charging switch over here. And the input sampling switch for the comparator that we discussed here a phi 1 we can of course, adjust if you want the phi 1 to be longer we can make it longer then the logic required over here will be different here the logic implemented is you know simpler you are just you know ending all this Q 1 bar Q 2 bar 2 clock bar. If you want the phi 1 to be longer, then you need to make sure that the counter is disabled for longer duration.

It is not counting for longer duration. And also you need to have another scheme which is going to count how many pulses of phi 1 you want further or how many phases of the clock you want for the if phi 1 duration. For example, when the phi 1 goes high, after that logically, but should I do in order to extend the phi 1 for the I should count how many clock pulses of the original waveform you need for phi 1 to be high. So, if I want to extend phi 1 right. So, one of the question was that you want to keep phi 1 high and

you want to have the sampling duration slightly longer. So, that the rc time constant is relaxed and also on the other hand your comparators close loop operation can be relatively slower. So, there I can extend the phi 1 remember phi 1 is putting constrain on the closed loop operation of the offset cancellation circuitry, if you remember the offset cancellation circuitry that can be having a severe constraint as we discussed yesterday.

So, your having the sampling capacitor coming over here and in the unity gain configuration this is the effective circuitry. We are having you are connecting this to vcm. So, effectively ac ground and this is the c offset and this is your V out. So, effectively for V out the offset appearing as a load capacitance and we are doing it in the phi 1 phase. So, we are operating these 3 switches in the phi 1 phase. And therefore, we should make sure that this doing this small duration the phi 1 phase it is able to charge this c offset to the required V offset their for settling time should be fast enough. And we have seen earlier also settling time depends upon the pole of the amplifier the 3 db kind of frequency of this closed loop operation. And we therefore, should make sure that the closed loop bandwidth of this unity gain configuration is fast enough as compared to the frequency given by this phi 1 duration.

So, if you keep phi 1 equal to this load duration of the clock low phase of the clock, the corresponding period that we see of course, is going to be almost twice the clock frequency that the bandwidth of this comparator should be several times higher than twice the original clock frequency. So, that the settling is fast. So, that will be the constraint. So, if the frequency over here is 250 kilo hertz I would like the closed loop bandwidth to be several times higher than that at least say omega hertz will be a comfortable number. So, so that was a constraint.

If I allow this phi 1 to stretch longer. So, therefore, longer duration phi 1 is staying high. Then of course, I will be able to allow more time for the phi 1 phase and therefore, I will be able to allow more time for this closed loop unit again configuration to charge the c offset. Likewise I will be able to allow more time for the sampling capacitor, where the input is getting sampled on the sampling capacitor. We have seen; however, that is not a very severe constraint even if you are using this low duration for example, you know having 250 kilo hertz of clock, and you are using this 4 microsecond duration for sampling the data onto the sampling capacitor. Using the switches even minimum size which would be able to meet that constraint. You can slightly increase the 3 dimension of

course, to meet that that is not there is a relatively less severe constraint, but here the constraint can be more critical because here you need to make sure that the open loop bandwidth of the amplifier is close to one megahertz and despite the large load capacitance and the compensation capacitor coming into picture. So, that was more serious constrain that we discussed in the last class.

So, this constraint may mandate that let us rather than trying to push this closed loop bandwidth to higher value I can extend this phi 1 duration little longer, So that I can relax the bandwidth requirement for the closed loop operation. What we discussed yesterday that open loop bandwidth you do not have the composition capacitor you do not have a stability constraints. So, that is not major constraint, you are easily able to achieve the open loop bandwidth, but for the closed loop bandwidth we have effectively this large c of coming that loads the capacitor loads the comparator in the closed loop as a result you have to use the compensation capacitor and other result the bandwidth goes down.

And in order to make sure that the bandwidth is remaining sufficiently high I would like to take this. So, this question is clear like we first looked at the simpler scheme when we are assuming that just one duration is good enough for achieving the phi 1 pulse and during this phi 1 operation all these 3 operations of off state sampling input sampling you know, you know have the input this is your phi 2 phase and at this point you have the input getting sample. So, if I mark this as a star you have the input getting sampled as well. So, this is the star point this which is off during phi 1 on during phi 2, others are phi 1 phi 1 phi 1. So, this was this is also happening during phi 1 phase of the sampling capacitor c s.

So, this sampling of the input the offset sampling on c offset and the discharge of the c ref. All these 3 should complete within phi 1. And what we identified this is the more critical one can be this closed loop operation, other 2 are easier to solve probably here you just need to take care of the leakage in the off state. Otherwise you can just increase the size just have a cross check that the leakage in the offset is not disturbing the c ref or making it non-linear that is one constraint. And the other one this is also relatively easier to handle if you just for instance increase the size of the switch little bit or corresponding to that just to preserve the same voltage level and signal integrity you increase the cs. So, that linkage is not causing the droop. So, this is also relatively straightforward, but the constraint comes here.

So, for that we can discuss another extension where you can try to make this phi 1 programmable or you can have a longer duration for phi 1, any question? So, this distinction is clear between the present scheme where we are using only one negative phase of the clock which indeed is phi 1 simply by taking the and the and of all these output. And second one where we would like to extend this phi 1 for a longer duration.

Student: (Refer Time: 32:21) short term.

Short term will not be feasible because here the transitions the max fastest transition will be allowed by the fastest clock that you have in the system. You can make it shorter you can some logic you can insert some logic (Refer Time: 32:32) rather than clock if you want to rely on some logic you can do that, but why will we do that there is that is not required at all there is not going to give us any benefit in terms of functionality or speeding of the operation there is no point. So, we can take a 2 minutes break and then resume our discussion we can discuss the alternate scheme and then go into the transistor level implementation of all these blocks the flip flops the logic that we are trying to implement and everything, and look at the issues related to transistor level implementation of these circuits.