Analog Circuits and Systems through SPICE Simulation
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Lecture - 39
Comparator for ADC

Welcome back. We have just had a description on the designing sizing of the switches.

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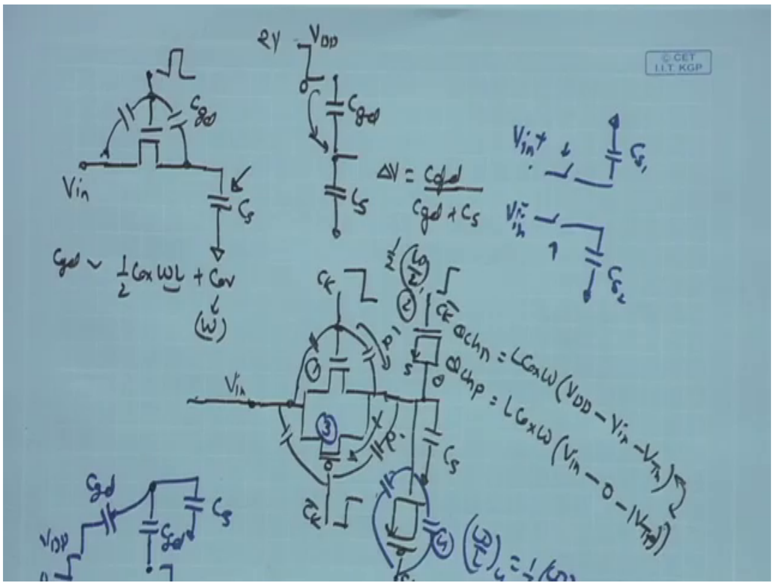

For the sample and hold circuitry and we looked into the non ideality associated with the switches. Namely: the charge injection clock feed through there are some other issues also related to the noise of the switch, but here since we are talking about the ADC and the signal is pretty amplified we may not really consider the noise produced by the channel current over here.

So, we are ignoring the noise part so that 2 particular component that we have discussed is a clock feed through and channel injection current charge injection along with that we also seen the sizes of the concentration based on the leakage current and the on resistance. So, these 4 concentrations combine together the leakage current on resistance the charge injection and clock feed through can give us indications about the sizing.

So, based on the based on the off resistance we determine the value of CS which is required to store the data with a good accuracy. Next we looked at the on resistance and confirmed that the sizing ratio for the new size ratio for the transistor is good enough to meet the minimum possible T on. We said that the T on could have been reduced relatively further as compared to the on duration or the sampling duration, but we chose a value of say few microsecond which is a much smaller fraction of the total time duration total sampling duration that we have.

And then we also try to look into other moralities like the parasitic capacitance resulting in clock feed through and the channel charge injection which can lead to inaccuracies. And there also be confirmed that the large ratio of CS versus the parasitic capacitances of this MOSFET can be helpful in mitigating these non idealities.

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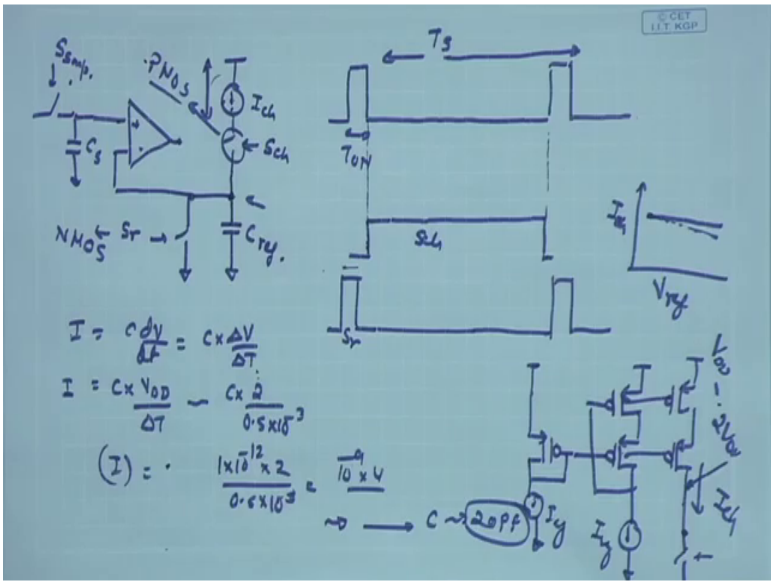

So, now once we have considered this sample and hold unit we can go further and look into other fundamental built in blocks of our single slope ADC the other one that we need to check is the reference voltage ramp that we just discussed. And there we can see that one of the easiest would be to produce the reference voltage and time would be to charge a constant capacitor with a current source.

And therefore, if you just have a current source along with a switch which can charge a constant capacitor C ref it can produce a ramp with a constant slope provide in this current remain constant. So, this is your I charge and again call this switch as say S charge whenever this S charge is going on this voltage will be increasing linearly with time also to begin with I need to discharge this I need to set this switch to ground and I can call this S reset.

So, when the S reset is getting on this will be discharged to ground and then this can be applied as a reference to our comparator that we discussed this is our CS the sampling capacitor. And we have the switch over here which is our S sample. And here we need to look at the time waveform for the S switch and S r when are we going to meet them. So, as we discussed earlier we are going to use a narrow pulse for the sampling as compared to the overall sampling duration. And this is your T sample and this is your T on, and as soon as the data is sampled at the falling edge of the T on.

Remember, when the T on is getting off the data becomes stationary or stable at the CS and I would like to start my conversion or the ADC operation at that point. And therefore, it is the right point to put the S C h on. So, I would like to put my S C h on at this duration and keep it on throughout the entire T S minus T on just before the T on gets activated again I would like to bring it down and this is your S charge. And likewise I have the S reset the S reset can coincide with the T on. So, when the T on is on you can have the S reset turn to 0s that the reference voltage is anyway set to 0.

So, that set can be just be confident with the S reset. So, this is the tiny waveform that we expect that we will see how to produce in the digital logic. So, later when we go to go to the component digital components the counters and the control logic we can see the mechanisms through which we can generate this using a single global clock. So, in general the entire system you will have just one clock and using that you may have to generate the appropriate control signals for everything else. So, we will look into that little later right now I am just single that the waveform available to in the simulations you will be just required to construct these waveforms using ideal switches sorry the ideal voltage sources pulse sources with certain T on T off ratio, and certain frequencies suitable to get these waveforms.

Now here, once again we have discussed 2 components 2 critical component that is the current source and the capacitor over here whose choice is going to determine my overall charging behavior. And once again we expect this minimum and maximum voltage over C ref to be close to 0 and be ready respectively, because our input voltage is also having corresponding range. And therefore, the I C h over here can we can say I equal to C db by dt where you have the delta V, because this is going to be V almost a constant slope.

And therefore, I can just replace this D V by D y delta V by delta T and this delta V is going to be VDD almost in our case 2 volts and the delta T corresponds to the entire charging duration if I assume that this is almost same as T S because I can ignore this T on I can take the T S as I guess 0.5 millisecond that we use in the beginning. So, I can take this as 0.5 millisecond.

As a result I guess C times 2 upon 0.5 millisecond coming over here. And once again I like my C value over here to be sufficiently larger than the parasitic components parasitic capacitances of this switches and the amplifier because of the removal parasitic capacitances can change with the voltage. So, the voltage is changing over here the parasitic values especially C G D, C G S and they can change as the voltage changes and as a result the rise will become non-linear with time I do not want that.

So, I would like the C ref to be sufficiently large as compared to all the parasitic capacitances is coming at this mode and once again if I look at the comparator from the switches even if there is a minimum size transistors at least you will have say a few femtofarad or few tens of femtofarad of capacitances coming over here, because of the input devices and therefore, it will for safe to meet I can choose this C ref to be say at least 1 picofarad.

So, let us check whether if I where choose this C ref to be 1 picofarad which is sufficiently higher than all the parasitic capacitances of these inverter I will be getting I value which is pretty small if I look at this 10 to the power of minus 9. And as a result the required I value can see its going to be you know pretty small as per the required conditions over here and if I look at say.

So, in terms of order of magnitude having just 10 to power of minus 8 coming over here which is just 0.01 micro ampere. Now producing such small values of I definitely this feasible on chip if I try to see it is definitely feasible to produce such low values of i. However, the precision in order to maintain the precision for such that low value I you can you will have to do a lot of you may have a C ref of these topologies for the current generation source and current mirror for that for such low values a few tens of nano amperes the current precision is maintained and if you want to have better precision and more robustness we may like to go for literally larger charge current over here.

So, few tens of nano ampere or 10 nano ampere may not be a good number, because that is going to have a lot of variation over process and temperature. So, remember for this kind of current the transistors implementing the channel the I c h will be operating in sub threshold regime and with process and temperature there is a lot of variations. And it will require a lot of calibration for that this is within the within the given accuracy. So, generally when we use this kind of very sub-threshold current sources there can be some mechanism through which we can calibrate them and even after the fabrication

We can set them close to the desired value, but the control becomes more and more challenging if they are operating in deep sub threshold regime. Therefore, that may mandate a larger value of C over here. So if at least if you want to have a 100 nano ampere so, that you have a 0.1 micro ampere of current we can see that you require at least say 10-20 picofarad out of capacitance over here. So, if I choose say 2.5 ;25 picofarad out of capacitance that will lead to 0.5 0.1 micro ampere of current which is relatively safer up to 100 nano ampere of current it is relatively safer once you go below 100 nano ampere of 0.1 micro ampere it become more challenging to maintain these currents to a good precision.

So, I select C say 20 picofarad which can be of course, quite area hungry it will take a lot of area if I have 20 picofarad I remember in the fronted amplifier once again we had limited our capacitances to 10 picofarad and lower, but again once again here in the ADC the robustness requirement the requirement to keep these current sufficiently robust over process and temperature we are forced to have a C value which is larger.

Of course, another constrain is also coming from the delta T or the sampling frequency. If you are trying to have something which is faster that is and also or if you are going to have the sampling frequency which is smaller that is also going to require a smaller delta T, because the charging rate is correspondingly smaller ultimately you have to have transition from 0 to VDD.

So, if you are trying to save power once again you can see that the area is going to increase. So, there are always tradeoffs power and area power and precision and so on. So if I assume, if I try to save power by curtailing my signals to further lower frequency rather than one kilohertz if I try to curtail it too few 100s of hertz by using a low pass filter.

So, in that case probably I will be able to use the a smaller I will be able to use a larger I will be able to use a larger T over here I am sorry as if I am trying to use a larger signal frequency or if I am use and trying to use a smaller delta T over here. And of course, for a given VDD I required also you know goes up further. And therefore, the once again the power consumption in this particular branch is going to go up.

But, but in general the power consumption in this branch may not be. So, critical because we have seen that the power consumption in the fronted amplifiers etcetera are sufficiently larger at least few tens of microampere whereas, here you have we are limiting this current or limiting this current to a few 100s of nano ampere or one microampere.

Therefore, that that is not an important constraint; however, area definitely is a more serious constraint over here, because a capacitor values of larger than 1 picofarad the area becomes pretty large for a 40 nano 180 nanometers PMOs technology the area density of this capacitor may be just up to; so, a few tens of around 10 femtofarad per micrometer square. So, 1 picofarad; that means you are having 100 micro meter square 10 micro cross 10 micro. And if you are having say as such a large value of 20 picofarad you can assume correspondingly large area.

So, the C values take a huge amount of area as compared to all the transistors etcetera the area becomes an important constraint. So, this is regarding the choice of the I c h and the C ref this is just one point that we have addressed. Now we also need to look at the choice of the bias current I R or rather the ramp current c h. And also the switches over here now here of course, switches are going to be much less critical, because they are just supposed to discharge the current to ground and here it is supposed to just pass the current provided by c h to the capacitor.

And therefore, I can afford to have this switches to a minimum size um and also we need not worry about the voltage drop across the switches if even if there are minimum size and the r on of the switches is suppose say 10 kilo ohm as we just discussed. This is here we are looking at the current which is maybe a fraction of micro ampere 10 to power of minus 7 or something and as a result the voltage drop across this switches will be very small is even there in triode region and fully on the way I have intended power of 4 times of the power of minus 7. So, less than mill volt drop across the switches when they are fully on.

So, we do not expect significant drop across the switches as a result we can use minimum size transistors without worry about the voltage headroom over here likewise here of course, it is just supposed to discharge this current. So, here headroom is not at all important. But here of course we are trying to connect this current source with the help of the switch to this point. And we know that the current sources we need certain minimum voltage headroom however. And therefore, the switch should not eat up that headroom.

But remember the digital switches we are just acting like switches and turning on and off they can operate in deep triode region when they are on and they are voltage drop is very insignificant as compared to the voltage headroom of the current source therefore, we do not worry about the headroom of the switches another point regarding the price of transistors. So, here we are trying to discharge the capacitor voltage to ground and we know that NMOS is a good candidate for that. So, I can just use an NMOS I do not need get TV over here likewise this current is supposed to charge this voltage to the maximum possible value VDD from 0. And therefore, we know that PMOs is a good candidate for this one because PMOs can easily charge the capacitance node to VDD.

So, I can use the PMOs comfortably over here without worrying about putting at cg. So, we do not need a cg for either of these 2 transistors now let us talk about the I c h that we are trying to implement and remember the constraint for I c h is that we try to keep it as constant as possible even if this voltage is changing. So, in fluently we should not allow I c h to change significantly.

We should keep the ic h versus this V ref almost flat in order to ensure good accuracy and for that once again we would like to use cascode current mirror and if you use cascode current mirror remember for a cascode current mirror as we have seen earlier in our discussions the minimum headroom required is to the overdrive provided you use the reduced headroom cascode or wide swing cascode that we have discussed in the class. So, we can use a reduced headroom cascode that we have discussed in one of our earlier session to implement this I c h and there also we can make sure that the headroom consumed by that transistor is sufficiently small by using appropriate w by l of the transistor.

So, if you remember the discussion we can have our reduced swing transistor this is reduced the headroom transistor where you are having I ref injected into the PMOs and the you are having the same I ref injected over here and with the help of this you can bias the cascode current source this becomes my current source there I am providing the I c h. So, you have the of course, a switch conducted over here.

So, this is your switch and this is prominent form in the output branch and here we know that the maximum voltage this can handle is almost going to be 2 V overdrive where V overdrive V S G minus mod vt of these 2 transistors. And if you sizes the transistor large enough the overdrive can be made sufficiently small maybe few tens of milivolt. And we can also make sure that the output the maximum output over here which is supposed to match the maximum output of l from the amplifier which is again VDD minus V overdrive of the previous stage we can make sure that this limit VDD minus 2 V overdrive over here.

VDD of 2 overdrive over here matching with the maximum voltage that are expecting at the input by appropriately sizing these 2 transistors by having sufficient w by l. So, that the V overdrive is minimized there to constrain I need the minimum l. So, that the ro is sufficient. So, that the slope remains sufficiently flat if you use very small channel length despite having cascode you may not get a very flat curve. Therefore, you need a minimum channel length. So, that the curve is sufficiently flat and also you would like to need the like to have the w sufficiently large.

So, that the over drive voltage is small. So, that I can we can have maximum possible voltages over here without pushing this transistor into triode and hence without deviating this current from the required I c h. So, the l determined by the flatness of the I D V D S curves and w is the remain by the overdrive voltage the first choose the l to get a very flat curve for the id V D S or in this case I would say I out I c h versus the V ref.

So, this should remain as flat as possible if V ref is reducing V ref is increasing we know that V S D will reduce. So, you know because the channel of modulation you can get some slope; however, you have to keep the channel in sufficiently large. So, that this slope is minimum and then at the same time you have to keep the w sufficiently large. So, that the over voltage is reduced.

So, now if now we have discussed the second critical module for the over design which is our ramp circuit for charging the capacitor we looked into the design or choice of the c f and the I charge we look at the tradeoff that despite a numerical value giving us a very small I we should not go for that and rather choose sufficiently large I c h. So, that it is robust enough it is more tolerant towards processing temperature variations and also we looked into the concentrations for the I c h in order to make it sufficiently constant and it.

Ensure the slope is remaining relatively flat up now the remaining expression is on the most critical block which is indicate comparator where we are going to look into the comparator design for the overall operation. We are going to look into the design issues associated with single operation also going to look at the non-idealities associate with the comparator which can hamper your overall operation or at least reduce the accuracy of your digitization. And trying to propose solutions to that along with that we look at architecture level how to resolve some of the issues or limitations faced by a single comparator by combining multiple of those and meeting the overall specs in terms of input range.

Because one of the most important design consideration for this for this ADC is the input range we need to make full swing at the input we need to meet the entire range swing at the input and for that again we you have another constraint coming into picture so that we will see that that gives rise to another difficulty and in order to meet the input swing. If you are trying to make some architectural modification trying to add other modules to make the input range large; we will see that other compared to non idealities like offset and mismatch can create for the difficulties. And we mean it to address those issues by having appropriate mechanisms to cancel out the non idealities.

So, let us look into the comparative design trying to look into the transistor level implementation the issue associated with the choice of the topology the number of stages the sizing and along with that. So, the non idealities like offset before we look into the comparator design it will also be useful to check out the check out the specification of the compare that we would like to use. So, that we can have some idea about the design parameters of the comparator and look at the practical number that you can have for the target comparator.

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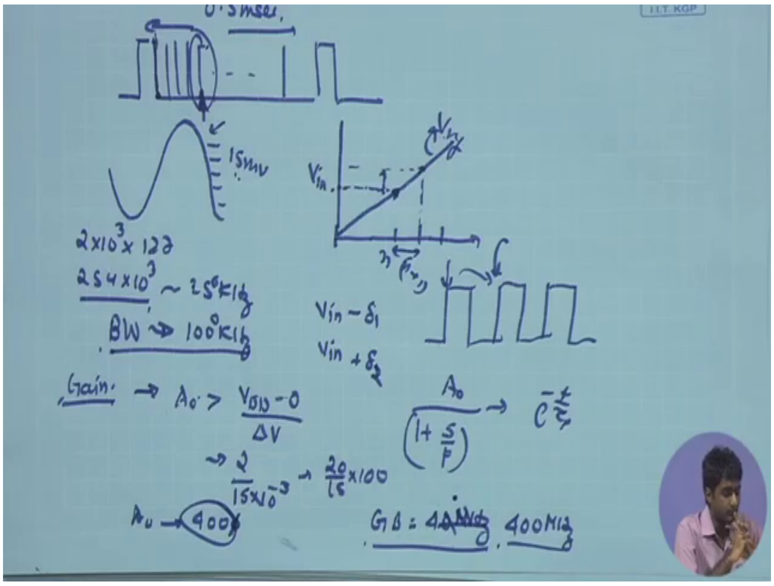

So, if I look at the operation once again I am supposed to have T S the time sampling relation that I have chosen is around 0.5 millisecond in this example. And as I said the comparator is supposed to compare the ramping we ref with the sampled input signal and the 2 important specs for the compare that you need is the gain and the bandwidth of the comparator.

So, for a comparator we can use the same 2 stage amplifier that we have been using for the front end application as well as for the filter design and so on. However, we need to look into the overall specifications in terms of gain bandwidth. So, let us let us first talk about the required gain of the comparator that we are going to use. Once again, if I talk about this entire duration where we are first of all defining the entire signal level into 15 millivolt segments and then, we are trying to map it into this duration of 0.5 millisecond. Remember that the on duration of the comparator that is as long as the comparator is high. That means, you are having the capacitor the reference capacitor of being charged and the on duration or the high duration of the comparator determines the magnitude of the signal.

So, is that come in the V ref which the input signal quicker; that means, of course, input signal is smaller and vice versa. And of course, that also implies that if you are having a a smaller input signal that with that there would in that that would imply that the reference signal is reaching the input quicker and you are having the compare output going down faster or earlier. Now if I look at this is the first metric that is the gain of the comparator for that we can arrive at the gain.

Several different ways if I look at the analogy for the analogy for the ramping circuit that we are looking at there the suck there the voltage is going to increase at different time steps continuously now how many time steps do we want in this interval. So, that we can have the number of quantization levels over here equal to the number of conversation we want in the ADC. So, we know that the ADC quantization we have chosen is say seven bit and therefore, we are looking for you know 127 different levels. And therefore, we are having the overall voltage signal divided into 127 different segments. Therefore, of course, if you have to measure the entire signal in terms of time duration in this entire 0.5 milliseconds.

I would like to divide this into correspondingly 127 segments and as a result if I look at the counter which is supposed to supposed to give me the current of or supposed to give me the magnitude of this duration and hence the magnitude of the input signal that is supposed to be driven by certain clock frequency corresponding to this time division. So, here I would like to have my overall signal or overall sampling frequency which is 10 kilo 2 kilo hertz chosen corresponding with that I would like to have the frequency of the clock given by 127 times 2 kilohertz.

So, close to 250 kilo hertz. So, this is going to be my clock frequency which is required to give me so many different levels in the time domain correspond to the required number of levels in the amplitude domain. So, I approximately I can take it as 25 kilohertz a comfortable number. And, now if I look at the comparator bandwidth under gain required to satisfy this 25 kilo hertz bandwidth for the clock.

So, one important factor would be the speed of the comparator how fast the comparator should operate and for that we need to look at the behavior of the comparator between the clock pulses at which it is having the transition. So, suppose the comparator is having a transition at this particular positive phase of the clock and therefore, we would imp this would imply that just before this positive edge the reference signal was equal to V in minus maybe a small value delta. And just after this particular instance the reference signal has gone up to V in plus delta 1 and provide this delta 1 or we have delta 2 provides delta 1 delta 2 are sufficiently large that would imply that just at distance the comparator should start to change its output from VDD to ground and before the next clock pulse arrive the comparator should be able to make the entire transition.

That means if I zoom out this region if I say that there is this is the clock which is driving the counter. So, before the next clock pulse come; that means, because the count gets incremented by one the comparator should be able to change its state. So, from this particular rising edge to the next time rising edge the comparator should be able to change its outputs state and settle to the low value. And therefore, I would like to make sure that the settling time of the comparator is definitely lower than the period of the clock over here.

So, here I would like to make sure the settling time which is given by the 3 db cutoff frequency of the comparator or the amplifier which is being used to do these are the comparator I would like the 3 T V cutoff frequency to be sufficiently higher than the clock frequency appear using over here. Remember if you are having an open loop amplifier which you are using as a comparator with the tungsten in auto 1 plus S upon p its overall time domain response will be given by the exponential factor 10 to the power minus T upon tau p will tau p is 1 upon T and in order to make that time constant sufficiently smaller than this time period.

So, that the competitor can respond fast within this one period I would like to make sure that the pole frequency of the amplifier that we are using is sufficiently higher than this 25 kilo hertz good margin will be 4 x. So, we can keep the amplifier bandwidth or target amplifier bandwidth to be at least you know 4 times 25 kilohertz. So, let us keep it 100 kilohertz we can be more aggressive and try even larger value, but for the time being we can stick to say 100 kilohertz.

Now this is the one only that is known other quantity that also needs to be figured out is the gain of the comparator and for that once again we can look at it in from different angles one of the possibility is to look at the ramping behavior of the V ref and at if I look at the different clock pulses. So, suppose the clock is going on and this is the n-th period of the clock and this is the n th plus n th period of the clock. So, of course, at this point the counts is going to increment from n to n plus 1 and suppose the V ref is the V is approaching the V ref. So, this is your V ref which is ramping up and this is the V in which is sampled.

So, the point where V ref equal to V in is the place they have to stop the counter down. So, if the V ref approach is being just act the nth come just before the n-th come the counter may miss this falling edge of the comparator because at this point ideally the comparator will go down, but of course the comparator has some finite delay and the control loop which is supposed to set the counter of it will also having some finite delay it may end up missing this transition, but definitely before the next transition I would like to make sure if the counter is able to the competitor is able to switch completely to ground.

And therefore, the by the time the signal is reaching or being incremented by this delta V which is given by the step voltage change between this time intervals we would like to make sure that the comparator is completely able to switch from say VDD to ground. And if I assume that this delta V is of course corresponding to the interval or segment that we just figured out remember you have the total number of segments over here which is n which is equal to that total number of segments in the amplitude domain.

So, if I assume that this delta V is the same as whatever delta V is use as a segment over here which is 15 millivolt we would say that within this single clock period the overall increment over here would also be close to delta V, because here starting from 0 going all the way to VDD and for this delta V duration you should make sure that the comparator is transiting from VDD to ground. So, to an approximation we can say that if this is the limit this is the minimum signal for which the comparator is having or having a transition from the minimum voltage level that is 0 going all the way to VDD or vice versa. So, this is output spring corresponding delta V.

So, to some approximation we can see that the open loop gain of the comparator a naught should be greater than this full swing which is 0 to VDD divided by delta V and in this case if I have VDD which will say 2 hold and delta V same 15 millivolt, we can have we can see the required gain as say 20 upon 15. So, basically 4 by 3 times 100 and once again if I look at the margin, we would like to have the gain say sufficiently large with that because of precision temperature variations if the open loop gain is going down we can have enough margin. So, I would like to make the actual open loop gain in the design at least sufficiently large in this number.

So, that because of worst case process and temperature variations if this number goes down as compared to the expected design value I have enough margin. So, rather than 100 I can keep some margin at least to say a few 100s or at least say we can pick a number say 400 we have these 4 points larger than this. So, let us choose a gain which is say 400 which is sufficiently larger if you want to be more aggressive we can go for even larger gain at least same 10 power of 3. So, that we have a very good margin and even in the worst case temperature in process variation we are having enough room over here remember that gm outer product of the amplifier they are very much temperature process dependent. So, we not like this again to drop below the required values.

So, let us keep the value 400 and therefore, we would have a gain method product which is going to be 4 mega. So, you are having 400 times 10 to power of 5 over here.So, we can see the gain bandwidth product is going to be 40 mega hertz for this particular case. So, remember this given every product is sufficiently higher as compared to what we use for a front end amplifier which is just around 1 gigahertz

So, here of course, that required gain open loop gain is lower you know just talking about 400 which is much lower than 10 to the power 4 let me target it for the fronted amplifier, but the bandwidth required is also relatively higher. So, just that it can operate with this high frequency clock always we can respond faster as compared to this clock that is giving us the upper up the lower constrain of the frequency. So, we have the requirement for the gain and bandwidth for this and comparator now what we have the specs we can go ahead and try to look at the transistor level implementation and associated issues or the comparators any question.

So, let us look at the comparator design which can meet the specs; the gain that we have over here as we have mentioned it is not very significant in the earlier designs you might have seen that a few 100s of gain can be obtained from a single stage. So, we may think that we are single stage comparator may be able to do it, but let us look at the issues and try to understand why still we may have to stage preferable it just in order to keep the design robust enough.

Student: Sir, this (Refer Time: 35:37) is 2 kilo volts then the value to the comparator should be 1 mega hertz or 250 kilo hertz.

So, sorry, 50 kilo hertz, sorry for the error; so here will be bandwidth is going to be 4 times to 1 megahertz and that just push this up. So, I am sorry for that I have a 4000 gain that is because I have chosen the initial frequency to be slightly higher if you look at the discussions earlier we had, we restricted our signal frequency to 100 hours. So, it here I have intentionally taking it higher at one kilo hertz just to make sure that the design is the more more aggressive neural potentials can have significant content up to kilo hertz.

So, that is a little bit upper limit, but still I have you know taking that in order to have the more aggressive limit for the enough that will just push my inner part; so, now, the things yes if I stick to the larger bandwidth requirements say at least 1 kilo hertz for the signal then of course, it seems like.

Student: Sir our gain is increased.

I guess you had the bandwidth 10 power of 3 and you are having the overall this is 1 mega, you have the gain which was you know 400 and that was also because we are having the overall factor that I said is around 100, but I just took you know the overall voltage the peak to peak voltage that you have to we have seen that the delta will appear expecting of around 15 millivolt. So, as a result we are having something like 100 times some integer.

So, we are trying to gain the gain which is sufficiently large if I sorry, if I look at the gain have taken it as 400. So, being bandwidth product if I say this is rather than 40 it is 400, so, I have the gain bandwidth products given by 400 megahertz which can be definitely challenging enough. So, you are having overall gain bandwidth product which is 400. So, if isolates. So, I was basically sticking to the earlier bandwidth. So, here intentionally I have increased the bandwidth from say 100s to kilo hertz. So, in our earlier discussion the bandwidth of the signal was maintained within 100, but just to ensure that the highest signal container not lost I have intentionally increase the signal content or the target bandwidth of the system to be at least 1 kilo hertz and that would mandate larger bandwidth now if I had taken more relaxed concerned about in terms of signal bandwidth so; that means, let the LPSs or low pass filter reject the contains beyond 100 hertz.

So, that my DSP can do the required computation within 100 hertz of signals and give us a required information that would relax that would have much relaxed content over here. So, in that case the bandwidth would be you know just 100 kilo hertz and the gain well product would be 40 megahertz still you know relatively relaxed, but now if I am targeting higher frequency contained in the signal also of course, it translates to trade off over here we are.

Student: (Refer Time: 38:55).

Having a much higher bandwidth requirement and also the open loop gain requirement, so, we can see that if you are trying to extract more information from the data and trying to have a larger frequency contained in the data you are paying the cost in the analog domain you are having to put more gain for the comparators and also the digital part which is the clock and the control unit we are going to have become more power hungry.

So, just like in the analog domain if you are having higher frequency contained or allowing till one kilohertz remember there also you may have to use relatively higher chopping frequency for instance because you need to shift the frequency further higher as compared to the corner frequency corner frequency may be 100 hertz, but now you mean to shift the signal frequency sufficiently high or at least few kilo hertz. So, that would also of course, need to increasing power in the fronted stages, but along with that if I look at say even the filter stages where you are having the anti chopped data which has been down converted to the original frequency and we are targeting say at least say up to kilo hertz.

So, all the stages including the VGA and the filter they will have to process that frequency contains. So, analog power of course, goes up here if I talk about the ADC there we are seeing that if you are allowing larger frequency contain the signal the overall gain requirement and the bandwidth requirement also goes up and hence we are having more stringent contain of the gain bandwidth. Now here if I take up say in order of 400 they are also still we have the same argument holding true we have almost say single stage which can achieve this gain, but along with that you have the you know bandwidth requirement for which you may have to restrict your overall r o values and hence burned sufficiently bias current sufficiently high bias current as well to achieve this kind of bandwidth and hence the gain bandwidth product of 400 mega hertz.

So, a CMOs technology if I look at the gain bandwidth product 180 nano meter can achieve gain bandwidth products close to few gigahertz easily and therefore, this is also within limit, but definitely it is on the higher side and it may mandate larger bias current in the comparator and hence increase your power dissipation of the comparator, so the design of the comparator. Therefore, would become a lot more challenging and we need to make sure that within a given power budget we are able to ensure the comparator operation and we will also see that if we look into other non idealities of the comparator like mismatch and offset it may further aggravate the requirement of the bandwidth that that I will come to at very soon.

So, let us try to look into the comparative design and try to resolve this issue of single stage whether has 2 stage and see what are the pros and cons of using just single stage to obtain this 400. Along with that of course, you have a bandwidth requirement which is also sufficiently large you are talking at talking about at least a bandwidth which is you know pretty large which is close to say 1 gigahertz and which is also very much achievable, but it is going to burn good amount of power in the comparator.

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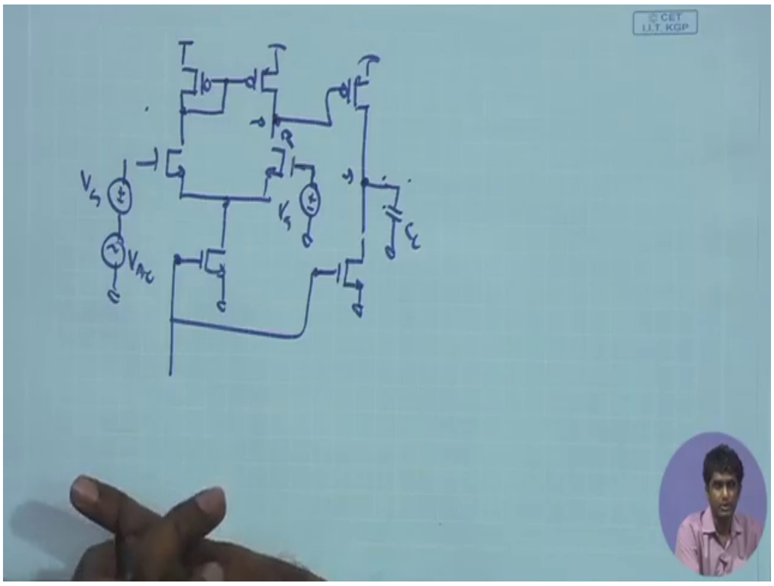

So, the time delay at you looking at for the comparator in this case will be pretty large sorry pretty small. So, let us get back to our comparator circuit where we are going to use our open loop amplifier and remember for the comparator operation ideally we did not worry about the biasing point of the output voltage over here and we are for the 2 stage op amp time of course, we have certain constraint if I use this as an op amp we need to make sure that this is at a proper bias point and that impact makes the in a feedback configuration of course, the negative feedback of the amplifier make sure that this is a framing desired bias point.

But for open loop conditions once again we do not have much control over the single ended output the differential amplifier or fully differential amplifier we have taken help of the common mode feedback to strength output to that point here that is also not feasible because it is single ended output. And we cannot really take a common mode feedback to stabilize this if we do take at the single ended approach and try to figure out something like the single ended version of the common mode feedback circuit it would require a very large r c time constant for just providing a low pass filter. And extracting only the DC component from here in the differential half you have the common mode extractor which is automatically extracting only the common mode DC value or low value common mode value.

But here if I try to extract the DC value your first establishing a bias point it will require a very large r c r c value or filter value used to implement such a common mode feedback or a DC feedback I should not call it a common mode feedback but a DC feedback to stabilize this 2 requirement. So, therefore, for signal inversion generally it is not very feasible to obtain a well defined DC point in the open loop amplifier if you are looking at integrated circuit, because those kind of very large r c values will not be feasible to extract the DC potential and then put a feedback to the amplifier.

Therefore, for in dependent circuit we do not have well defined DC point over here, but for comparator operation we do not worry about the DC point, because it can go all the way to VDD and ground in normal operation remember; however, in order to obtain the frequency response when you are trying to judge your amplifier for meeting the required again bandwidth constraint you need to use the appropriate DC bias point so that you can take the frequency response.

Frequency response remember it is an linear analysis where the simulator uses linear model the small signal model of the amplifier and the small signal model need that the amplifier the transistors are in saturation therefore, in order to use the frequency response you must make sure that you are applying a proper DC bias over here maybe VDD, VDD by 2 and make sure that this is also having an appropriate DC bias if you are using ideal values is a not having a very drastically different lambda and lambda p this will not necessarily being triode region when you are applying VDD by 2 over here it will be somewhere close somewhere between 0 and ground is VDD and ground, but only thing you do need to make sure is that it is not going too low or too high when you are applying a common potential over here for the AC.

So, once AC will positive you will connect a DC potential over here or maybe another DC potential here along with an AC potential over here and sweep and do the AC analysis for the output node but while doing this you should just make sure that the DC point over here is not too low or too high. So, that these transistors are entering to triode one of these are entering to triode for that even quick the bias voltage over here a little bit. So, that this potential is not going to down to up.

So, of course, we know that these are obtained using current sources and we can in general bias both these using a single current source , but just to take care of the DC bias when you are checking the frequency response if you use same bias over here and the output of the PMOs is also being just dictated by the DC point over here it is not listening that you will have this, that this close to VDD by 2 it may be low and high and pushing one of these 2 transistor in triode V in also.

So, you just to make sure that it is not happening you may be able to disconnect this and put a different DC force here at the gate of this NMOS. So, that by tuning that you can tune the DC potential and then you can take the frequency response, because we expecting that the gm and gm and r o values not change drastically if the currents are similar make sure that you are not drastically changing the currents, but by little bit tuning of the gate voltage you can just make sure that this is not going too low or too high that is one approaches for analysis sake when you are trying to do the frequency response and try to check the open loop divider of this circuit.

Now, once we have the frequency response here of course, as we said if you look at the V the required gain and bandwidth you have a overall beam requirement which we just estimate at few 100. So, around 400 and if we look at the overall bandwidth which is coming around at least say few 100s of kilo hertz to 1 gigahertz. So, the gain bandwidth product is pretty large and from there we can look at the overall sizing of these transistors and also the trice of the stages where you are going for single stage of 2 stage now if the gain by the product is too large we know that ultimately bandwidths will be determined by the small signal resistances and capacitances at the output nodes.

This is I frequency node which is going to give you a critical pole another one over here which is going to give you a critical pole this is a relatively low impedance node that does not give you a significant the pole over here is at much higher frequency. So, these are the critical poles. Now if I look at the output node and assume of course, that you have a load capacitance over here which is sufficiently larger than positive capacitances then the analysis will be simpler in that case I have the c l times the r over here determining the overall bandwidth.

However, if the parasitic capacitance over here is too small in that case if the load capacitance over here is too small in that case this node may end up dominantly. So, we can consider both cases for life time being we can you know start with a c l of a nominal value and assume this to be the dominant pole and try to look at the calculation of the W by L values.

So, we can take 2 minutes break after that we will resume the discussion.