Analog Circuits and Systems through SPICE Simulation
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Lecture - 38
Ramping Circuit

Welcome back, and let us resume our discussion on sampling, so last model we discussed the leakage issue with the switch and we looked into the R off and C S combination which is ultimately going to determine the size of the C S, what is the minimum value of the C S required to successfully store the sample data over the entire duration.

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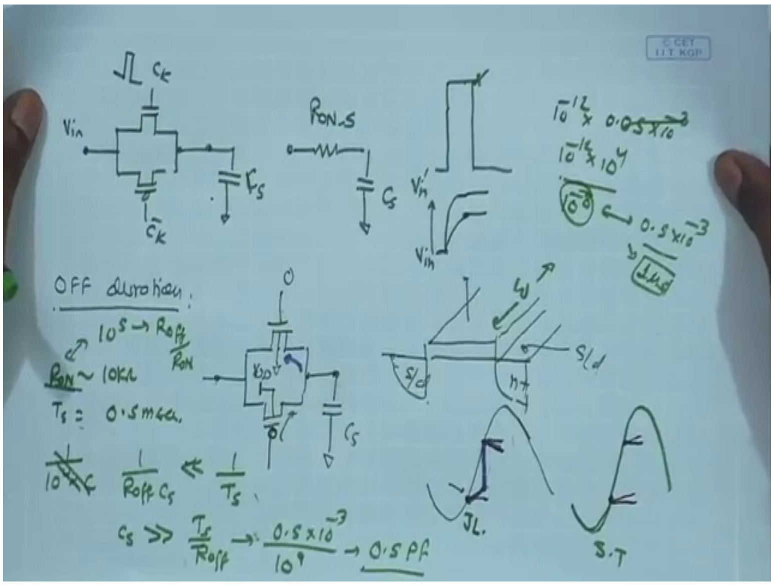

Likewise you also would like to make sure that the R on and C S factor is also matching our criteria of being less than the T on duration over here. And that will ultimately determine what should be my T on how aggressively my T on can be scaled down so that I can use very narrow pulses for sampling my analog data for that once again I can just check the numbers if I use minimum phase transistor and assume the R on to be 10 k and the C is say close to 1 picofarad then once again the value that I get over here is going 10 to the power of minus 6.

So, you having say capacitor or 10 to power of minus 12 and you are having T S which is say duty cycle of the T S you are trying to reduce by say 1 upon 10. So, in that case you are going to have 0.05 millisecond, now whether we can go for 1 upon 10 or lower that of course, depend upon this particular value and if you look at the sorry, if you look at the rc combination you are having the overall R on given by the 10 to power of 4 and this is going to determine my T on duration, here I am getting overall factor 10 to power of minus 8 which looks like much smaller than the T on duration that we are targeting our sampling duration is 0.5 millisecond and as compared to the R on C combination that we are getting that T on duration looks like pretty large as a result we do have a lot of room for scaling down T on in this case. And in general for CMOS technology even if you are using a minimum size of transistor the sampling duration can be relatively small for the given capacitor size that is we have chosen.

As a result we can aggressively scale down this T on and duty cycle ratio of maybe just 10 or even lower can be good enough for sampling the data. So, we do have enough room for sampling or reducing the duty factor and sampling the data with very narrow pulses only thing that you have to make sure is that the data is stable enough for that we have already determined the C S. So, what we concluded of this is that for a minimum size transistor we have enough had room for reducing this T on and we can go down at least by an order of magnitude and you say a few micro second of pulse widths to do the sampling.

So, even if I use 1 microsecond rather than 1 millisecond will still be within limit very comfortably within the limit. So, let us go for you know 1 microsecond why we are not going for lower than 1 microsecond that has something to do with the generation of this 1 microsecond pulse. So, we will see that when you go for the digital control and all how these control signals for sampling switching etcetera will be generated. So, early switching we can go down further may be sub micro second regime, but for the time being let us choose this 1 microsecond because it is significantly small as compared to our overall all sampling duration of 0.5 millisecond. So, if this is close to 1 microsecond it is hardly significant as compared to the entire sampling period. So, let us stop here.

Just few points regarding the R on if you are trying to increase the switch widths just to speed up the transistors there can be other issues that can also come into picture which relate to the which are related to the non ideal effects of these switches and their effects can still be seen even the switch is minimum size their effects can still be seen at the output and if I using minimum size transistor to the effects will be smaller, if we go on increasing the size of the transistor then they become a lot more prominent, that is another reason oh for choosing a sufficiently large C S.

Let us see those 2 reasons those 2 contributors very briefly and how they can have an impact on the sample data how they can corrupt the sample data. Remember the resolution that we are seeking is around 15 millivolts. So, we do not want this signal to be corrupted by more than maybe few millivolts if we want to preserve the signal integrity over here. Therefore, any non ideality is coming from the switches if it is trying to corrupt this data beyond few millivolts definitely it needs to be considered. Even if it is minimum size transistor we must make sure that it is the non idealities associated with this switch is not significantly distorting the data over here.

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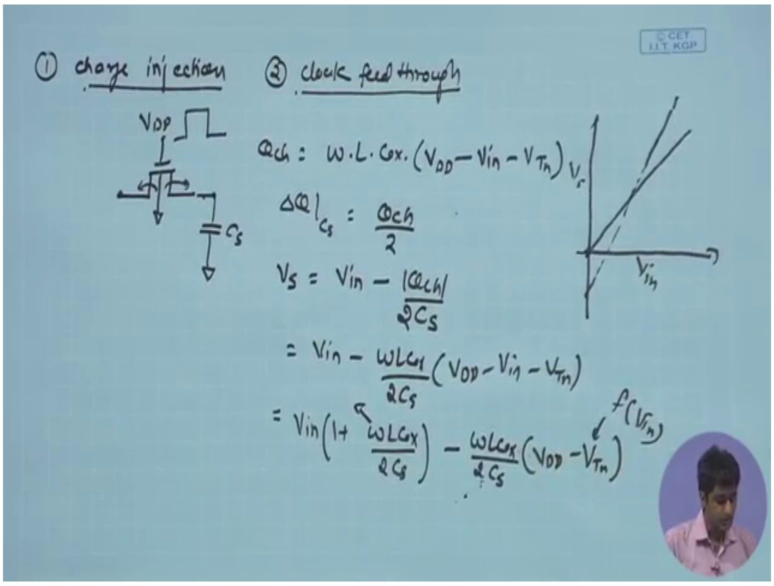

So, let us look into the 2 main factors which are which can distort the data which is first one is the charge injection and we will look at the second one which is clock feed through. So, these concepts are in general very crucial than we are looking for switched capacitor circuits wherever we are having amplifiers combined with lot of switches and capacitors to implement interesting functionalities like integrators or closed loop amplifiers filters and so on here we are just talking about the sampling operation where also these 2 effects play a very important role and can limit the accuracy that we can achieve by the sampling process. Inherently we will see that the transmission gate topology that you are using is going to give us advantage in terms of both of these. But it is important to be aware of both these non idealities.

The charge injection arises because of turning off of the transistor whether it is NMOS or PMOS and if I look at this behavior you have a sampling switch suppose I am considering only NMOS and the switch is turning on and then going off. We know that the channel charge in the NMOS if it is in triode region it will be almost uniformly distributed in the channel source drain are all almost equivalent for the triode region when the input is almost equal to the output and under that condition I can write down the total channel charge in this MOSFET Qch as W times L times Cox times the overdrive voltage which is going to be V GS minus V t.

So, if I say V G which is the gate voltage when the switch is on which is V DD minus V S. So, source can be taken as either this one or this one better than the triode region both the terminals are almost equivalent when the switch is on and therefore, I can just take it as V in minus the threshold voltage which is V Tn. So, this is the overall channel charge that I can write.

And when the switch is turning off this channel charge is supposed to be injected out of the MOSFET. So, when the switch turns off this channel charge gets injected and if I assume that half of it gets injected in the opposite directions I have Qch by to jumping on to this capacitor which is C S therefore, the delta Q that I get on the C S that is going to be Q channel by 2 assuming that the charge is injected equally on both sides after the MOSFET gets off.

Because, remember then you turn off the MOSFET the mobile electrons forming the channel charge have to be injected out, so that the MOSFET is turned off and that injection involves injection of negative charges on both side, because remember NMOS is going to have electrons as channels the mobile charges are negatively charged electrons and therefore, it amounts to a negative charge injection on both this point.

So, this is basically going to be a negative Qch minus sign injected onto the C S. And therefore, what we can expect is that as compared to the V in the V sample would be V in minus this mod Qch upon 2. Now this is the delta Q that is injected on the C S therefore, what should we expect for the delta V, we know that Q equal to C V. So, according to that we should have a delta V the change in voltage over here this delta Qch or Qch divided by C S. So, this is going to be my the voltage ideally it should have been just equal to V in, but because of the Qch it is having this particular magnitude and if I plug this in I have this as the positive quantity.

So, W L Cox upon 2 C S times V DD minus V in minus V Tn and if I take this common I am left with 1 plus W L Cox upon 2 C S and then I have some negative quantity which can be given as W L Cox upon 2 C S V DD minus V Tn this is what we are left with. So, ideally I would expect V S equal to V in, but I am getting this whole term where I have first of all some nonzero gain factor. V in times this gain factor which is greater than unity and then I have some offset term which looks like independent of the signal to the first order. And definitely that that would mean that I am having some corruption in the signal as compared to the sample signal my data is slightly different and if I plot these, so ideal would have been V S equal to V in, but because of because of the gain which is greater than unity I am going sub I am going to get a slope which is greater than forty five degree and also we are going to have a negative offset. So, when V in equal to 0 I should have some negative offset.

So, as a result I am going to have the actual curve looking like this ideally this is what we expect therefore, I have deviation in the sample signal as compared to the input signal. And of course, we can see that if the area of the switch is increased that is W and L is increased and the C S is reduced then the effect of this channel injection the charge injection will be much more prominent. So, if you are trying to increase your sampling speed then of course, the corresponding charge injection if it can be more prominent it is going to corrupt your data more strongly. So, there is always a tradeoff between the sampling speed that we are trying to achieve and the charge injected.

Remember that this is, this charge injection phenomena is more or less going to be independent of the T on duration because T on duration or the duty cycle even if you aggressively scale it down it does not affect the overall quantity of charge injected whenever it is getting off it will inject the same amount of charge.

So, it is independent of the T on of the duty cycle the duty cycle is not going to affected; however, the size of the MOSFET and the capacitor they are going to affect it. So, if I am trying to make my T on if I am trying to make the MOSFET larger or C S smaller in order to facilitate faster sampling it is going to have more corruption because of this charge injection effect . And we can see that the overall non-linearity that is the overall gain error that is coming is dependent upon the W L Cox upon 2 C S and if we talk about this quantity W L Cox for a overall if you if you are looking at a nominal device of 1 micrometer with this parameter W L Cox for 180 nanometer technology L being minimum say 180 nanometer W being say close to 1 micrometer this factor can lead to few femtofarads. A few 10s of at the max you know few femtofarads and the C S if I want this to be this error to be sufficiently small C S must be sufficiently larger than this.

For example, if I am talking about say high precision say 1 percent or better precision then of course, I would like this to be at least several 100s of femtofarad the other term over here also can be problematic if I look at this V DD minus V Tn this V Tn is also quantity which is not independent of the signal. So, V Tn in general will depend upon the body effect and if I look at the NMOS where the body terminal is say grounded and you are having the source terminal which is equal to V in.

So, ultimately this becomes a function of V in which is having an highly non-linear characteristic. So, therefore, it is also going to introduce non-linearity when very high precision application it can be more critical for our application where the precision is relatively limited it still less you know not so much critical. However, we must make sure that in the overall design when you are designing a samplings switches these effects are minimal and they are not violating our precision requirement. For example, in our case we would like to make sure that the overall the factor resulting over here is not leading to more than say a few millivolts of error in the sampled data.

If I talk about the other issue which also comes in because of the clock action is called clock feed through and that has to do with the parasitic the action of parasitic capacitances associated with the clock.

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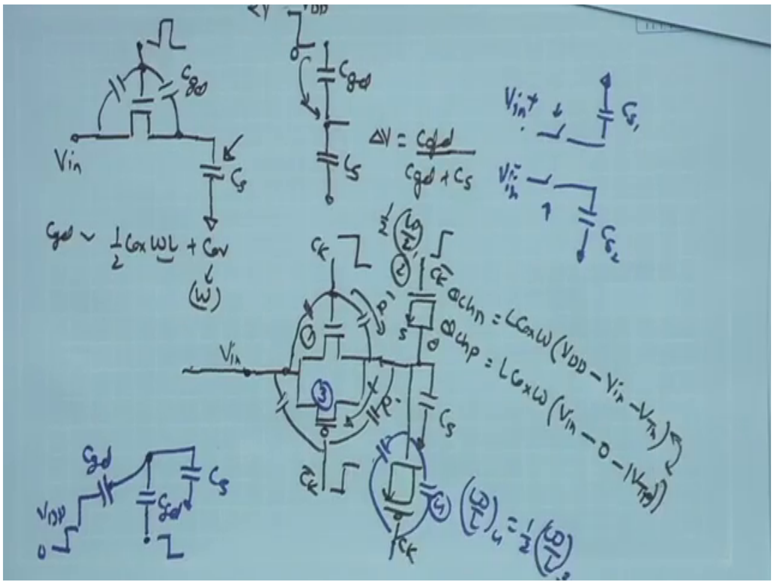

So, if you have a NMOS over here and if I assume that you have the parasitic capacitances from the gate to the source and gate to the drain entire region remember both of these are almost similar. And you are trying to switch this the switch on and off by applying that pulse and you are having the V in over here ideally if it these 2 are absent and for the time being if I ignore the channel or the charge injection effect the switch is faithfully going to replicate the V in over here. But now if I also look at the condition when this switch is almost turning off and the that condition I have an effective voltage divider form between this C I can call it C gd of this MOSFET and the C S.

So, at the verge of turning off the switches we can we can assume this is an almost an open circuit and then we have the input voltage over here transiting from V DD to ground. Therefore, we effectively have a capacitive divider where the input signal is transiting from V DD to 0 to turn off the switch and we have the C S over here and as a result if I want to see what is the effect of this voltage transition on this point this is something like an AC divider where because of the capacitive coupling this step voltage over here is going to have some effect over here.

So, if I look at this it is just going to be proportional to delta V is resulting from this clock action is going to be proportional to C gd upon C gd plus C S. And therefore, once again we can see that if the MOSFET dimension is larger for example, if you are having a larger W of this MOSFET once again the cg d will be proportional to the W of the

MOSFET also you have in saturation region you have the overall C gd given by a combination of the oxide capacitance and the over loop capacitance, so for it is also proportional to the length of the MOSFET.

So, in the triode region remember both C gs and C gd become almost similar and they are proportional to the C gd is proportional to the 1 upon 2 Cox W L plus the C overlap this term depends upon the W of the MOSFET and here of course, you have W L, so both dimensions. So, basically if you are having a larger size MOSFET once again to cater to faster speed you can expect more corrupt ion and especially here you are having a V DD which is you know 2 volt and you would not like this potential to fluctuate more than few millivolts because of this clock action and therefore, it becomes critical that this C gd is sufficiently smaller than C S thousand times smaller than C S.

So, once again this is going to impart from limit on the some lower limit on the value of C S if you want to have sufficient accuracy for the data sampling I would like the C gd to be orders of magnitude 1000 times smaller than C S and that would again imply that if I talk about the minimum size transistor also even if I am using minimum size transistor with W L minimum and it is having few femtofarads of parasitic capacitances. That would imply that the C S must be at least 2 picofarad to ensure that the signal is not significantly corrupted because of this delta V coming in.

So, once again we can see that these constraints related to the non relatives of the switch are going to play a significant role in determining the sizing. So, even if you are looking at low frequency application where the size of the MOSFET can be afford to be small we should be careful about these effects and that is going to put that is going to increase the lower limit for C S. So, first limit came remember from the leakage we had looking at the leakage and that should not call sufficient droop in the output sampled voltage as compared to the ideal value. And there are other 2 components also coming in because of this clock action term which is called which is termed as clock feed through and other 1 charge injection. Why it is called clock feed through because the clock which is transiting at this gate of this MOSFET, but because of the parasitic capacitance you are having feed through of that voltage because of this capacitive coupling.

So, if you connect 2 capacitance series and you are having a large jump at this point of course, you will see some fluctuation at this point because of this capacitive voltage division because remember this transition point is going to have high frequency component it is not so and because of that high frequency component definitely you are going to have the corresponding signal propagating at this point because of this voltage division. So, we have to be definitely careful about these 2.

And another one important factor is that if you are using in transmission gate base MOSFET there to some extent this both charge injection and clock feed through can be minimized because remember the PMOS and NMOS actions are just opposite. When the NMOS is getting on PMOS both NMOS and PMOS are getting on the gate voltage of one of them is going to V DD another one is going to ground therefore, the polarity of the gate voltages or the clock waveforms are just opposite and to some extent they can cancel the effect of clock feed through as well as charge injection. It depends very much upon the MOSFET parameters and it is very difficult to exactly match them and cancel them out, but to some extent of course, transmission gate can help in minimizing both these effect that is the clock feed through and charge injection because of the opposite polarity of the clocks applied to the gates of this MOSFETs.

So, you can again look at the combined structure where you have the PMOS and the NMOS and you are having, you are having the charge injection effect as well as the clock feed through over here and other sampling capacitor C S and you have the V in coming in from here. And remember if I talk about the clock action for turning off this MOSFET the clock will be going in the negative direction whereas, turning of the PMOS it will be going opposite direction. So, the affect of clocks feed through if I assume this equation is just opposite on 1 terminal you are having the signal going from 0 to V DD another 1 V DD to ground therefore, to some extent it can get cancelled if these capacitances are almost similar. And in order to make this similar it will be important to make them almost same dimension. However you know, you may not be able to exactly cancel that out it is not always possible to have exact matching between these 2, but to some extreme it can definitely reduced.

Likewise if I talk about the charge injection charge injection for the NMOS as we said it is going to inject negative charges right. So, whenever it is turning off the electrons which are forming the channel of the NMOS will be injected on the opposite side PMOS is having holes in the channel right. So, effectively it means vacancy of electrons, so when the PMOS turns off the holes get injected physically of course, electrons get injected into the PMOS channel to kill the channel. As a result the NMOS is going to dump electrons whereas, PMOS is going to sync electrons when the channel gets off. Therefore, it will also try to cancel out this effect to some extent and therefore, once again you can have some cancellation some degree you can have some cancellation.

Of course, if you look at the charge throat the equation of the charge throat if you can see for the NMOS it is going to be V GS. So, if I assume that this particular potential is V in for the NMOS we have seen the Q channel of the NMOS is going to be Cox W times L times V GS minus V t. So, V G is V DD minus V S is V in minus V Tn and the Q channel for PMOS you look at this again L times Cox time W for that it has to be V SG. So, if I say V SG so V S becomes V in and gate becomes 0 because when the PMOS was on V G was 0, and V S was V in and then you have minus mod V TP. So, this is the magnitude of the PMOS charge because for PMOS when the channel was on it was the V SG, S is the input voltage or the sample voltage over here both are anything similar. And the G is 0 for the 1 condition therefore, V SG becomes V in minus 0 minus mod V TP.

And therefore, if you see the magnitude point of view it may not cancel exactly because you have 2 different terms over here only for certain value of V in it will cancel. But at least to some extent roughly it can minimize the charge injection effect to some extent . There are other schemes people do apply like rather than depending on this NMOS and PMOS pair if you also add additional dummy transistors over here for example, for the NMOS if you end up adding a dummy transistor these are source and drain which are short it together and then you are having the W and then assume that this W is half of the NMOS over here. So, this is if this is W 1 is this done M 2.

So, what I am doing is I am shorting the source and drain and this is the gate I am applying just a clock bar over here. So, when this turns on this turns this turns off this turns on. So, basically when if I assume that W by L 2 is W by L 2 is half W by L 1 this is this is dimension just half the dimension of this one; that means, if I assume that half the channel charges injected over here that can be used in forming channel of this NMOS also this is very well matched with this particular NMOS. Likewise if I put a PMOS dummy device that is having W which is just half the W of this PMOS when it turns off I will turn that one on. So, I can have another PMOS device dummy I can short the source and drain. So, the source and drain is shorted and if I am feeding clock here I will feed clock bar here if I am feeding clock bar here I will feed clock here. So, that when this

NMOS is turning off this dummy NMOS is turning on and it will just sync that charge because it if this is injecting the charges channel is getting killed its channel is getting formed. So, it will just sync that charge.

Likewise the PMOS over here when this is getting on when this is getting off because of the 0 to V DD transition it is injecting the holes whereas, this is getting on because I am driving it by clock another result it will be injecting those holes to form S channel. So, when S channel is getting killed it is forming a channel likewise then S channel is getting killed this one is forming the channel and if their dimensions are matches W by L of this being half of W by L of this one. Likewise W by L of this being half the W by L of this 1 it can help in mitigating the charge injection to some extent provided we have almost half charge injected on both side which is not always true. Also we can see this configuration can also help us in mitigating clock feed through because if I look at the capacitance for one of these devices. So, the C gd of these devices will be the combination of C gs and C gd the total capacitance and the W of this 1 is half the W of the PMOS over here this capacitance and the total capacitance provided by the parasitics over here will be similar.

From assuming that if this is 3 and this is 4 W by L of 4 is half W by L of 3; under that condition once again these 2 capacitances combined together will be equal to the capacitance over here and as a result if I look at the condition I have clock transiting from 0 to high over here, but here you have just opposite transition you are applying the reverse clock over here. Another result if I look at the total signal over here at this node I can model it as the first capacitance having a transition from 0 to V DD and the second capacitance total capacitance is provided by the MOSFET over here which is having transition from V DD to ground and then again having the total capacitance over here C S. So, these 2 will be almost similar because the W by L of this 1 is half of this one. So, the C gd and C gs combine or for this MOSFET is going to be same as. C gd of this MOSFET assuming that is a triode region both are almost similar.

So, in that case I can see that the overall effect of 0 to V DD transition and V DD to 0 transition will be almost canceled out because of the equivalent C gd appearing over here and then the overall effect can be cancelled out likewise on the NMOS side. And because this NMOS these transistors are the source and drain are anyway 0 say in terms of static currents they are do not having a static current they are just going to sync the current little bit of a fraction of current when the channel gets on and again eject the current which channel gets off and their action is opposite to these two. So, they are not of course, having any static current. So, they will be having only transient current just to form the channel and the kill the channel.

So, this methods can be used to mitigate the effect of clock feed through and charge injection to some extent especially when you go for high speed circuits where the switch dimensions becomes critical and the C S has to be smaller this becomes very handy. We can see later that if you look at using fully differential circuits the effect of these 2 phenomena can be mitigated further. So, here we are having single unit circuit if you are using fully differential circuit the effect can be mitigated to a larger extent. For example, if you have a fully differential implementation you are having 2 C S, C S 1 and C S 2 and the input signal is also fully differential V in plus and V in minus then these offset terms that come over here with other charge injection and clock feed through can be cancelled out to some extent.

Of course there is non-linear dependency on V in just we saw that. So, it will not be ideally cancelling out fully, but to some extent a fully differential implementation even for the comparator can help in killing this non idealities. So, that is one of the reasons why people prefer fully differential even fully differential comparators and fully differential ADCs. So, that the moralities of these switches can be mitigated to some extent and especially we will go for high precision circuit where the precision becomes a lot more critical or you need to do some very sophisticated DSP digital domain for which you need very precise analog data for that I would like to cancel out these effects of these moralities.

But in that case I would like to make even my ADCs of the comparator fully differential, right now whatever comparator we are going to discuss probably is going to be first version is going to be single ended differential input, but single ended output. But later they can see how to extend it into a fully differential comparator which will be applicable for the processing of a fully differential signal as well. All right, we will take a short break and then start our discussion again.