Analog Circuits and Systems through SPICE Simulation
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Lecture - 33
Transistor Level Design Of Fronted Amplifier (Contd.)

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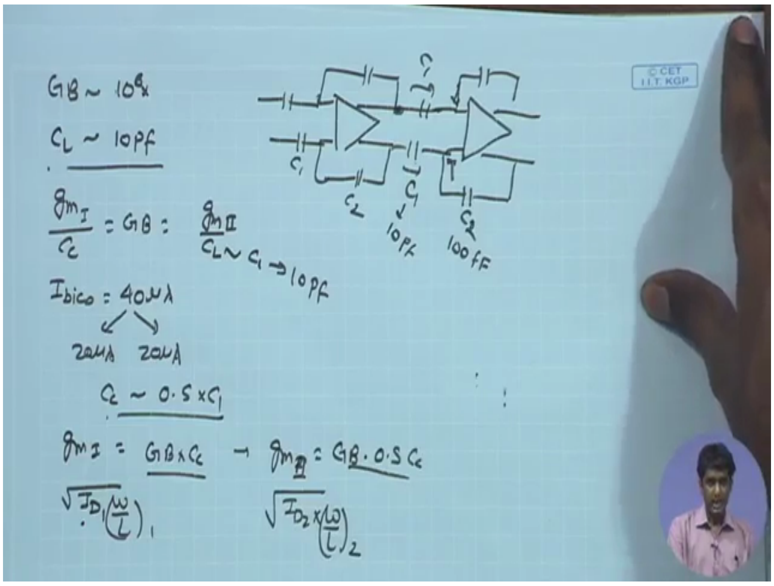

Welcome back. So, let us resume our discussion. Now once we have this W by L ratios available and the gm 1 available we need to look at the gain what is the gain requirement. So, if I look at the say next requirement of gain, let me keep this sequence over here as it is and let me go to the next requirement which is the overall open loop gain that we are looking at and also the corresponding bandwidth.

So, we have the open loop gain requirement which is the 1 10 to the power of 4 and once again we can divide this in an uneven fashion, we can take a smaller fraction of the gain for the first stage and larger when for the second stage or vice versa and that also depends upon design considerations if you are going for say larger gain for the first stage once again it basically contradicts with the wise requirements. So, for the time being let us bifurcate the gain requirement also equally it is not a bad price you can you can do that especially for low power applications where the current budget is the fading factor.

So, let us go for the equal partition on the gain between the 2 stages and then say that A 1, A 2 the gain of the first in the second stage each is going to be given by around 100.

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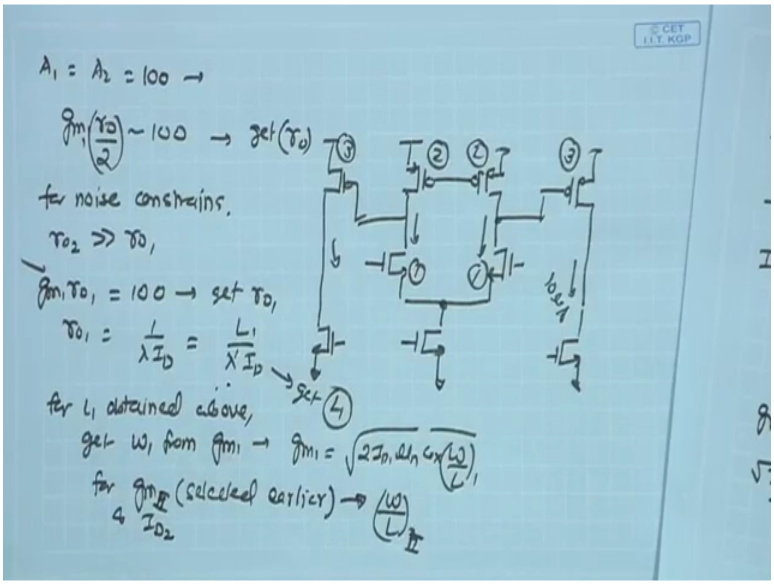

So, that the overall open loop gain of the amplifier is 10 to power of 4 as we needed and that would mean that gm 1 times ro by 2 of the first stage should be 100, the gm 1 has already been determined in the previous stage based on the gain balance requirement and the C c L requirement and therefore, the ro can be obtained from here. So, I can obtain ro of the input device.

Now, ro of the input device does not mean that you have both the ros coming into picture the ro which is smaller that will be coming into picture while determining the gain of the first stage.

once again just for the sake of simple convenience and drawing the entire circuit and the ro in the first stage is going to be the ro of the smaller ro of these two. The first stage ro is going to be determined by ro P parallel ro M for the differential operation and assuming that the bias current in both of them are similar, the ro is going to be dictated by the channel length. And if we call our discussion on noise we know that the low input referred noise requirement asks us to keep the channel length of this PMOS sufficiently large because that appears in the denominator are L square when we are looking at the input referred noise V in square.

So, the channel length of the PMOS must be significantly larger, as a result the ro of this PMOS can be pretty large as compared to the ro of the M. So, for noise requirement for noise constraint I would generally have if I call this input pair M 1 and the PMOS M 2 I will generally have the ro 2 much much greater than ro 1 it can be at least 10 times greater than ro 1 and as a result the gain in the first stages they going to be determined by gm 1 ro really ro 1. So, I should it will be more accurate I would say the gain is gm 1 ro 1 and that would give me the value of ro 1 estimated.

So, this gives me gm 1 ro 1 equal to 100 and with the known value of gm I can get the value of ro 1 and we know that ro 1 is equal to 1 upon lambda I D which also depends upon the channel length if you remember we discuss in the very beginning while discussing the device concept that the lambda is can be expressed as lambda dash upon L times I D. So, if your channel length is larger effective channel length or effective small signal resistance increases therefore, the L over here can be estimated based on the value of I D and the ro that we have.

So, I D we have already got from the power budget this came from the power budget and ro 1 came from the gain requirement and hence I can get the L 1 the input device channel length from this constraint. And once we get L 1 from here once we get L 1 from here we can get the W of the input device also because from the gm constraint. So, once we have for L 1 obtained above we can get W 1 from gm 1 because again the gm 1 is nothing else, but root under 2 I D 1 U n co x W by L 1. So, since L 1 is known I D is known I can find out the W 1 required. So, I have the input devices for the first stage.

Now likewise if I have the value of gm 1 and also the gm 2 known from the previous step if you recall the gm 1 gm 2 ratio also was known depending upon the C 1 C c and C L ratio that we set. So, C c, C L ratio was determined based on area constraints and based on that I determine the ratio of gm 1 gm 2, gm 1 is known gm 2 is now also known and therefore, I have the current budget, I also have the current budget given to me. So, I bias of the I bias of the second stage is also known to me I have bifurcate the current into 2 half. So, here also I have the total current bias given by 10 microampere here, 10 microampere and both the branches 10 microampere leading to total to 40 microampere. So, each branch is having 10 microampere of current as our initial assumption and therefore, I have the W by L requirement of the second stage as well.

So, from this I can get for gm 2 assumed earlier I can obtain the value of W by L 2 gm 2 and I D 2. So, gm 2 and I D 2 that we obtained earlier from there we can estimate what is the value of W by L 2 required. Let me rather call this three let me call this pair as 3. So, this is 3 3, this is 2 2 this is 1 1 or I can stick to the roman letters just to be you know consistent with my notations let me stick to the roman letters because I am using the roman letter to determine the stages.

So, the roman letter 1 determines it means the first stage, roman letter 2 means the second stage let me stick to the roman letter and say that the gm 2 also I can denote it by the roman letter, gm 2 will be obtained by the gm 1 gm ratio that we had over here and from there I have the I D 2 also determine and I can look have the value of W by L 2 known.

Now once we have the W by L 2 known there once again we can look at the overall sizing constrain or the L values for the PMOS and NMOS devices as we have seen the 1 upon epsilon thermal noise of the second stage does not interfere so much does not reflect so much as the input referred noise because it is getting divided by the gain of 2 stages gm ro square. And therefore, the channel length sizing constraint does not come here or so strictly and therefore, these channels lengths can also be similar I do not really need to have very skewed channel lengths as in the case of the first stage.

In the first stage; however, as we have seen the channel length of this device needs to be determined based on the 1 upon f corner frequency. So, if you increase the channel length of this device and also the W of this device you can shift the corner frequency towards lower value. So, if you remember the 1 upon f corner frequency derivation it will be determined by the channel length of this and the W and L, W L product of this. So, if the area of this input device is large we know that the flicker noise is proportional to 1 upon W L and this flickered noise of this input device directly comes at the input. So, for that I do not even need to do any derivation I know that the flicker noise is proportional to or inversely proportional to 1 upon W times L.

So, I would like to increase the W L product. So, that I can minimize the input referred flicker noise of my first device or in other words minimize the corner frequency shift it towards lower values. So, shifting corner frequency why it is important because it will allow us to have a lower chopper frequency and hence lower bandwidth. So, for as if now we have targeted that let us keep the chopping frequency 100 hertz and if it can be met comfortably within this 10 microampere budget we are happy with that if you are still having more budget available you can further try to shift it back towards lower frequencies by increasing the channel length further and W by L further. But for the time being the target the initial target is just to check whether with the W 1 and L 1 that I have arrived at and by increasing the L of this device towards higher values how low I am able to shift the corner frequency.

So, I have the W and L of this input device already determined by the gain requirement and the ro requirement. And the next is the W and L of this, so as we said the L of this device can be increased we can try to push the L towards higher value and that will help me in reducing the 1 upon f corner frequency towards lower value what is the possible disadvantage of that at the first stage. So, if I consider a noise issue for let me you know just keep this circuit as it is.

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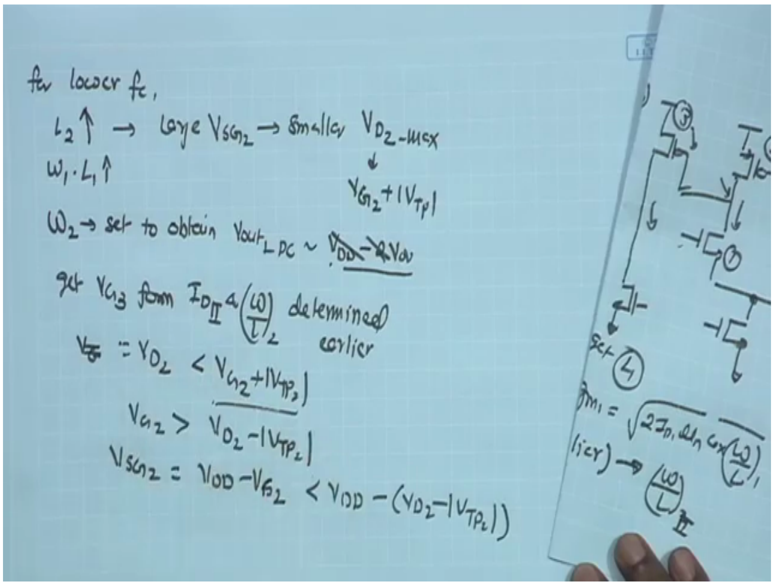

If I look at the noise issue for lower fc I would like the L of 2 to be large and also W 1 times L 1 to be large both these factors and if I increase the L of 2 we know that the overdrive voltage of M 2 will be increasing if I am increasing the L of 2. That means, the W by L of 2 of reduced the required V SG to support the same is given bias current will be increasing and as a result you will require you will require a large V SG drop and that would mandate that your overall signal swing at this node gets limited right.

So, if you are having larger L means W by L of M 2 getting reduced sorry. So, W by L 2 getting aggressively reduced because you are pushing the L 2 larger and larger to get the 1 upon f right reduced. And that is require going to require a larger V SG drop, a larger V

SG drop; that means, the gate voltage the gate bias voltage over here is going to be lower gate voltage over here lower means the maximum potential that you can have over here that is also going to be lowered right because we know that the maximum potential available at the drain of these 2 outputs is going to be V GP plus mod V t.

So, a larger L of these devices and smaller W by L of these devices larger L means larger V SG 2 and that would mean smaller V d 2 max because V D 2 max is equal to V G 2 plus mod V TP right because if you are requiring larger V SG; that means, smaller V D 2 max because the you know V D 2 max is V G 2 plus mod V TP larger V SG means smaller V G 2 and hence smaller V D 2 max. But is that a serious constraint for the first stage if you especially if you are looking at the input stage and the signal swing is relatively small 100 micro volt and the overall closed loop gain is say 100. So, at the max we will be getting a signal of 10 millivolt at the final output and for that 10 millivolt 10 millivolt we are having even further smaller signal swing over here.

So, final closed loop gain if I look at a closed loop gain of 100 the amplifier at the output will producing 100 micro times 100 and the for that 10 millivolt the input swing over here will be further 10 divided by 100s of 0.1 millivolt. Therefore, the swing over here may not be a serious constraint therefore, having a larger channel length for these 2 devices and having a small having a smaller V G and hence the larger V overdrive is not a significant disadvantage. So, that is also you should keep in mind. So, for the input stage noise minimization is going to be crucial having a smaller swing is definitely not a constraint. Even for the output stage you are having just 10 millivolt peak to peak swing at the max and therefore, the signal swing at the output is not a major constraint.

So, even if I have to choose largest channel length for these 2 devices in order to increase the gain higher and higher is not it is definitely going to reduce the swing for given bias current if you increase the channel length the required V G of this gate also goes up likewise the required the gate voltage of this NMOS goes down. So, if you are trying to increase the channel length of these devices also for example, to get larger gain for a given current.

So, for a given current if you increase the channel length the ro will go up and as a result the gain can be expected to be higher, but once again it is going to reduce the available signal swing, but that is not a significant constraint for the first stage and therefore, we can sacrifice the signal swing we can ignore the requirement of the signal swing while focusing on noise minimization while focusing on lowering of the 1 upon f corner frequency.

So, let us just assume that this W and L 1 is sufficient for giving us sufficiently low corner frequency and then I try to maximize the channel length of the M 2 so that our desired 1 upon f corner frequency is achieved. So, you have, remember if you have the W by W times L 1 coming in the first bracket and then you have the second one which is having L 2 square in the denominator. So, I would like to for a given W 1 L 1 I would like to maximize L 2 to basically check that a desired 1 upon f corner frequency is met. After that once you have L 2 determined once you increase the L 2 for that the 1 upon f corner frequency shifted further down then the question is for determining the W of these 2 transistors and once again it is not going to be a serious constraint. So, W 2 can be set to obtain say the V out over here V out 1 DC say close to at the max say V DD minus 2 V overdrive or V DD this can be a strain sufficient number. So, if the V over drive is the overdrive voltage for this a PMOS I can set the W by L over here, so that the desired dc potential over here can go down.

So, if I am looking for the maximum allowed potential over here and I would like to set it to say close to even V DD minus 2 V overdrive where V over drive is the required V over drive for these transistors. In that case I can accordingly set what is the W by L required over here. For example, for the second stage if I look at it I already have the W by L required from the previous equations and I also have the I D required.

So, that is going to give me the required V SG for these 2 devices and that V SG is the basically the drain potential of this one and I would like to make sure that that drain potential is sufficiently low for the PMOS over here. So, one possibility of sizing the W by L of M 2 is get the V G 3 from the I D 2 and W by L 2 determine from the previous stage and once you have that then basically we have the V D 3, V D 2 required. So, we have this V G 3 equal to the V D 2 and corresponding to that I would like to make sure that this V D 2 is not too high for the M 2. So, I would like to make sure that V D 2 over here is lower than V G 2 plus mod V TP 2.

And that means, I can obtain the value of V G 2 required V G 2 should be greater than V D 2 minus mod V TP 2 and that is going to give me the V SG requirements, the V G is greater than this then I know that V SG 2 which is V DD minus V G 2 must be smaller than V DD minus V D 2 minus mod V TP 2. So, this is another there is one way in which you can arrive at the V SG 2 requirement and that is going to give me the W by L requirement of the 2 transistors.

So, I already have the L determined from 1 upon f noise and then I can set the W of the 2 transistors following this equation. So, I have the V SG requirement coming from the gate expected gate DC potential and from there I can set the V SG 2 and that is going to give me the W by 2 because you know the W by 2 is going to determine by the V SG of the M 2. So, I already have L 2 known from the 1 upon f analysis corner analysis and then I have W by L 2 known. So, that basically gives me the W and L of the PMOS transistor over here. And I also have determined the W and L of these devices assuming that they are meeting by 1 upon f noise criteria and finally, the L of these devices W by L is known for this input device I need to check the L so that the gain of 100 is met in this stage.

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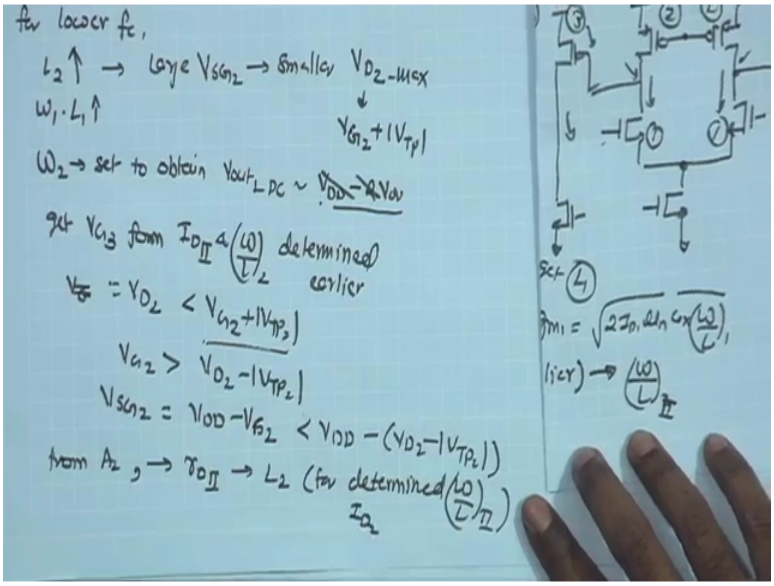

So, from A 2 I can determined the gain I can determine the ro of the output device which is going to be given by gm ro by 2. So, get the ro 2 and hence get the L 2 for determined W by L 2 of the second stage. So, W by L 2 has already been determined previously I have the A 2 known for the second stage around 100 and therefore, ro 2 known and that is going to give me the L 2 for a given W by L 2 and I D 2. So, that basically gives me the W by L 2 of this device and also the W and L individually. So, I have the W and L of the M 3 M 2 M 1 known; now the next is the question of these NMOS devices.

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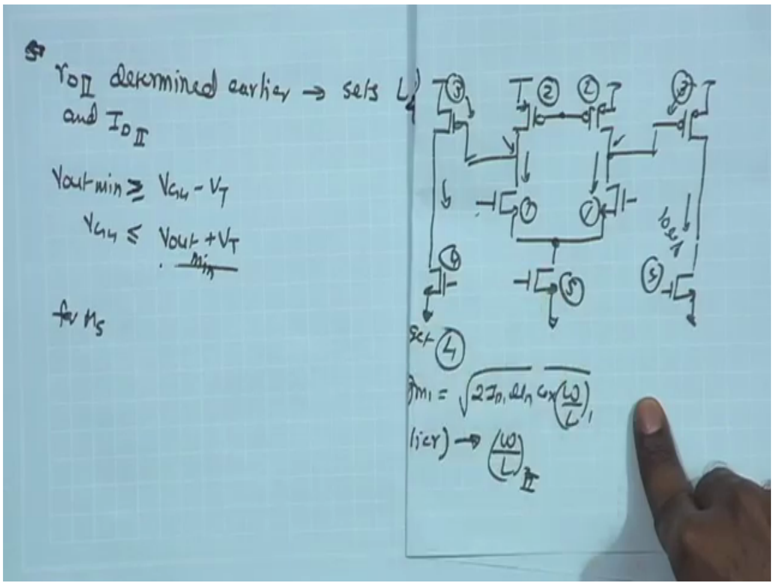

So, for NMOS devices once again the channel lengths should be similar for the second stage for this, if I look at the second stage if I look at if I call this say 1 2 3 4 M 4 pair; that means, I am calling this 2 at M 4. So, once again that ro is determined, I is determined for a gain requirement therefore, the ro 2 determined earlier sets the L 2 or you know L 4. So, L 4 is already known ro 2 and I 2, I D 2 determined earlier sets the L 4 because I D 2 budget is known and also the L 2 has L 4 has been determined based on the gain requirement. So, that gives me the L 4 also, so these 2 must have same L 4. So, that the ro is equal to the required value, so that gm ro is equal to 100.

And next I have the W of this MOSFET to determine and again W will be determined by the output signal swing required I must make sure that the output minimum level required over here is higher than V G 4 minus V t and that gives me the V G 4 constraint. So, V out min is V G 4 minus V t and therefore, V G 4 V out min should be greater than equal to this quantity. So, that this M 4 does not introduce a triode and therefore, V G 4 should be less than equal to V out min plus V t. And once again the V out min if I call this V out min V out min is not going to be very small because output DC point can be V DD by 2 and V out min can be you know hardly V DD by 2 minus 10 millivolt and therefore, this is also not a very important constraint and therefore, the W by L requirement of M 4 is not very significant in this case. I can have a poor W by L of M 2 also or W can be pretty small is not very important.

However, the tail current source once again for if I call this M 5, for M 5 what is the W by L constraint of the determine if the W by L of M 5 if we keep it small then the required V G value will be large for a given bias current and that means, the minimum input level that you can have is going to be small.

So, the gate level or gate potential of M 5 determines the input common mode range what is the minimum input signal level whatever the minimum input DC level that you can have. In our application, if you remember the gate DC potential is been determined by the output dc potential which is equal to V DD by 2 using the resistive feedback and hence the input DC point over here is fixed we are not telling DC coupled system the input is coupled through the main amplify using capacitive feedback. And this is the DC potential over here is determined by the output DC potential which is V DD by 2 and input signal is pretty small it is just a few 10s of microvolt 200 microvolt and this is going to be not having any significant signal swing.

Student: (Refer Time: 25:00).