Analog Circuits and Systems through SPICE Simulation
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Lecture - 29
Dual Loop CMFB Design

Welcome back in today's session and we are going to start our discussion by reviewing some of the concepts related to our previous discussions on common mode feedback, we will try to address some of the good questions that were raised and that can help you in doing the simulation assignments at the part of this course.

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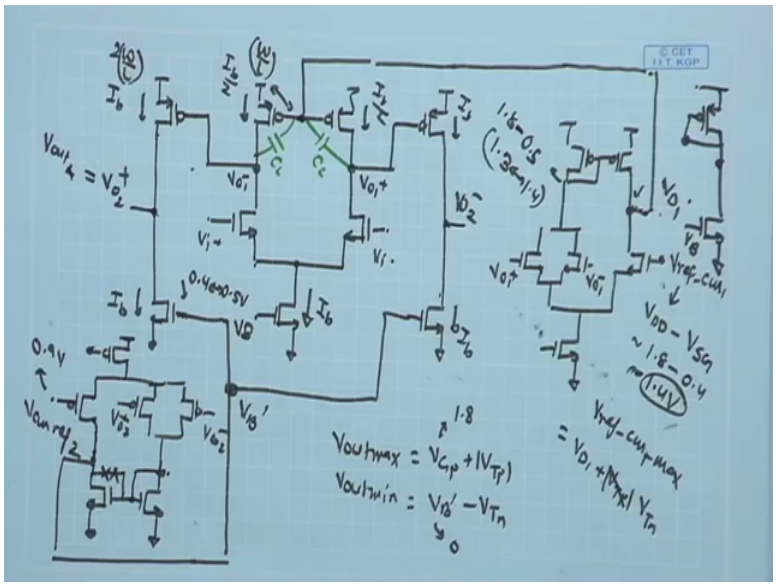

So, I will discuss the circuit implementation for the dual loop common mode feedback where you are having two separate common mode loops for the first and the second stage of the op amp and we look into the you will try to contrast this method with the single loop compensation that we discussed. And we will try to understand the pros and cons of both the methods and some of the details that we skipped earlier transistor level implementation of the dual loop common mode feedback we will go a little bit deeper into that and finalize the implementation which will be useful for your simulation exercise.

So, let us start with our op amp circuit that we had the two stage fully differential op amp with the input V i plus and V i minus and let us go for the common mode feedback for

the 2 stages separately. So, we are going to employ error amplifier for the first stage and another second error amplifier for the second stage over here.

Now, for the first stage we can build the error amplifier that we discussed in our earlier sessions, the split input pair extracting the common mode voltage over here and the output having an overall current mirror load which gives us a sufficiently high gain from the error amplifier. You are having the V ref cm 1 which is basically the common mode reference level for the first stage coming over here and if I call this V o 1 plus and V o 1 minus I can put it over here V o 1 plus and V o 1 minus coming over here and the output of the error amplifier goes to our PMOS load of the first stage.

And this is what we have done in the beginning while we looked into the common mode feedback of a single stage differential amplifier in isolation. So, we have already analyzed this particular configuration where you have the single stage diff am compensated by an error amplifier. And we looked into the composition scheme, and we suggested including coupling capacitors between the gate of the PMOS transistors and the output of the first stage which is effectively going to give us overall miller multiplication at this point.

And therefore, if we remember in the common mode half circuit we are going to have this C C coming between the input and the output of the common source stage provided by this differential pair. And likewise we can also look for the common mode feedback for the output stage, before we do that we have to look for what is the output expected from the error amplifier which is compensating the second stage or which is go going to provide the common mode feedback for the second stage.

It is supposed to drive the gate of NMOS transistor and therefore, if we use a similar structure over here to drive the gate of the NMOS transistor it would require a vg close to say V t of this NMOS. So, if you talk about 180 nanometer technology the V gs required may be close to 0.4 0.5 volt if your V DD is 1.8 volt and V t is around 0.4 volt. So, I am assuming that the V gs will be close to 0.4 0.5 volt and under that condition the output potential expected over here will be close to 0.4 volt and that can push the input device into triode region because if you look at the DC operating point if you look at the you know DC operating point of this error amplifier this is going to be behaving like a simple

differential amplifier with current mirror load. If I look at the common mode responses of this suppose these 2 DC potentials as well as the bcm ref are close together.

The output DC point over here is going to be close not the same, but at least close to this gate voltage of this PMOS load which is basically V DD minus V gp and again this V SG drop will be close to the V t of the PMOS mod V t of the PMOS which is again 0.4 volt. So, nominally this potential will be close to say 0.4 V DD minus 0.4 or 0.5 volt, so V DD 1.8 minus 0.4 or 0.5 volt.

So, it is something like point 1.3 1.4 volt and we are expecting that the DC potential that is required to drive this is of course, much lower it is close to 0.3 point is going to be close to V t of the NMOS. So, 0.4 2 0.5 volt this is what we expect over here. So, if I look at the DC condition for this amplifier nominally this potential will be in this range 1.8 minus 0.5 so around you know 1.3 it can go to 1.4 in this range. So, this is a minus sign and this is you know the range just let me distinguish this.

This is also I am talking about the range 0.4 to 0.5 volt around and accordingly we also need to see what is the V cm ref that we are putting for the first stage in order to see whether this amplifier is going to work properly if I am using it only for the first stage.

Now, if I look at the DC conditions for the current biasing I am using some I buyers with the help of this current mirror and I also may be using the same I bias in these 2 branches. If I assume that you are having the same almost same I bias in these 2 branches which are being fed with the help of a current mirror with a reference branch the 2 PMOS over here are also having I bias. Whereas, under DC condition what we expect is that these 2 PMOS transistor they are going to have I bias by 2, I bias by 2 and these sources are identical. So, this current sources that we are putting we are expecting that these are going to have identical dimension there before they are also going to sink I bias each and as a result I am expecting I bias over here as well in both the PMOS load of the or PMOS input device of the common source stage.

And now in this case I would like to ensure that the W by L of these 2 PMOS device they are having certain ratio with the W by L of the PMOS device of the load. If I look at these devices the tail currents of devices if I assume that their ratios are same. So, for the same gate voltage applied by reference branch they are going to sync the same current and if these are supposed to sync the same current as well I would like to make them

double the size of this transistor, so that the gate potential that is applicable for these devices are also close to the gate potential coming over here.

So, if you have a single ended op amp where the first stage is the diode connected there you directly have an insurer that the output DC potential over here will be rated by the gate potential of the PMOS and that also becomes the input disappoint of the PMOS of the common source stage. But in this case the output DC point is not defined gate potential over here is expected to be such that it supports the same I b by 2, I b 2 by 2 flowing in these transistors.

Therefore the V SG or the gate potential over here provided by the error amplifier should be such that it is supporting the I b by 2 current in these 2 whereas, if I am expecting I b current in these 2 the for the same gate potential I need to have W by L ratio over here which is double. So, if this is W by L this should be 2 times W by L and also the gate potential of these PMOS should be close to the gate potential of this one. So, that it supports the same I b suppose the double the I b for twice W by L ratios.

Therefore this drain potential or output DC potential and stable operation should be close to the required it should be you know the output common mode that you get over here should be close to the V gp of this load transistor. And that V gp is once again going to be close to the V DD minus mod V tp value therefore, I would expect this V cm ref to be close to V DD minus V SG of the MOSFET, of the PMOS which is once again going to be 1.8 minus 0.4 0.5 volt, so once again around 1.4.

So, the V cm ref value that I am getting over here is going to be around 1.4 volt and therefore, under steady state when you have a common mode stable the effective common mode input coming at these 2 input is also going to be around 1.4 volt is that safe enough for this device whether it is going to operate properly with such a large input common mode value that also needs to be verified. So, if I look at this amplifier in isolation the maximum common mode level that you can have for this amplifier that is the maximum common DC level that you can have for the input device over here and here that is the (Refer Time: 10:41) determine by the V d plus mod V t. So, the V ref cm max if I want to find out what is the maximum allowed value of V scm that you can have V ref cm 1 max that is going to be given by the I would call it V d let me call this V d V d 1, V d 1 plus mod V tp because if assume that under DC condition you are having

certain V d 1 over here the maximum common mode level that you can have at the input is going to be equal to that V d plus mod V t p.

So, the DC bias under the nominal DC bias this load is going to have DC potential close to this 1 which is say 1.3 volt and therefore, the maximum input level that you can have maximum input common mode that you can have over here it is going to be the drain voltage plus the V t of the NMOS sorry, this should be plus V tn of the NMOS. Because here we are talking about a particular drain voltage which has been set with the help of this diode connected MOSFET and if you are assuming that these 2 voltages are close together under nominal operations these 2 voltages are supposed to be close together another result the drain voltage over here is set with the help of the diode connected MOSFET that is V DD minus V SG. So, that is same over here.

So, (Refer Time: 12:10) assuming the under nominal condition under sterile steady state operation the V d 1 is having a value close to 1.3 1.4 and under that condition the maximum input level the maximum common mode level for this amplifier that you can have or in other words the maximum reference common mode level that you can have for this is going to be the V d 1 plus V tm which is once again 1.3 1.4 plus the V t.

So, it can go very close to V DD the input allowed level or the maximum V ref cm level can go all the way to V dd. So, that is not a problem. So, having a higher required V cm is not a problem for the input device over here. So, even if it is 1.4 it is not going to bring this transistor into trouble or the PMOS also into trouble because the from the maximum side this gate, this drain potential is being clamped with the help of the diode connected MOSFET and for of that particular drain potential I am just seeing what is the maximum allowed V cm ref that you can put. If you go on increasing the gate potential further and further what is the maximum gate potential that you have while keeping this transistor into saturation that is going to be the drain potential plus V t.

Beyond that the transistor over here will be entering into triode region. So, that is why we are first of all finding out the V d 1 which is going to be close to the DC potential over here as long as these 2 potentials are close and then for that V d 1 what is the maximum V cm ref that you can have that is going to be equal to V d 1 plus V t. So, that is going to be pretty large it can go very close to V DD. So, 1.4 is not an issue as a V cm ref. So, this is one conclusion.

And the second thing is the V out. So, as I said V out is anyway close to the DC potential of the gate of this PMOS which is also going to be the DC potential provided for the gate of these 2 PMOS over here therefore, it is going to be consistent. So, it is very much suitable for biasing the PMOS transistors over here.

Now, one question can be how to obtain the V cm ref because this V cm ref is supposed to be equal to the DC bias points over here and what we are saying is that these DC points over here should also be close to the gate potential provided at this PMOS. So, for that I can create a reference gate potential of such a PMOS transistor and feed it over here.

So, for that I can use a diode connected PMOS and apply the same reference V b whatever V b is coming to this tail current source I can apply the same reference voltage V b over here and this is going to produce V DD minus V SG potential over here which is going to be close to the DC potential over here.

So, in order to be if you are keeping these 2 devices same then in order to get the same vg as this device I also need to keep the size of this device twice these of the individual device because these individual devices they are crediting I b by 2, I b by 2 and if I keeping this 2 same then the diode connected MOSFET over here should be double the size of these individual devices because this together will be carrying I b. Other option is you make this half this size you can make it half of the tail current source over here in that case you can keep this device dimension same as this device dimension under that condition whatever V G is produced over here will be suitable for biasing the V G over here and this can provide the reference voltage I can keep this as a reference cm over here for biasing my PMOS drain voltages.

So, what it will do it will enforce that the DC common mode level at the output of the first stage is close to the DC gate voltage expected to support I b and if that is happening I know that the same gate voltage is going to the PMOS over here and therefore, looking at these ratios it will also ensure that it is supporting I b current in these 2 MOSFETs.

Student: (Refer Time: 16:40) keeping the V SG upon the MOSFETs equal to V t (Refer Time: 16:42).

I am not keeping V sg equal to V t it will come close to V t because the current value that we are using in our example is pretty small, few tens of micro 200 micro and as a result the overdrive (Refer Time: 16:57) will be small V gs minus V t will be small as a results the V gs will be close to V t. So, that is what I am assuming in all these examples and any doubt in whatever I just did regarding the DC biasing, regarding choosing the V ref. And why this particular you know amplifier or error amplifier with NMOS as input and PMOS as load is to table for biasing this PMOS gate.

Student: Sir, can it effect in swing.

Which swing?

Student: Sir, when we applied in differential amplifier if the bias point output bias point (Refer Time: 17:31) because that (Refer Time: 17:32).

Output bias point we have, we have so far we have just fixed this bias point and what we are ensuring is that the gate potential provided to this 2 PMOS is suitable for establishing the I b current in these 2 and we are also trying to you know or expecting that these 2 tail current source are also having I b current. We are just trying to match or just trying to establish appropriate bias points where the two PMOS are driven by a gate voltage which will try to establish the current I b and at the bottom side also we are having these 2 NMOS where you know we are expecting the same bias current I b we have kept the dimensions over here same and therefore, right now we have not biased these 2 gates that will be biased using a separate common mode feedback loop. But we are expecting that this voltage will be remaining close to be b as a result this will also tend to pull or you know pull down the same bias current I b.

So, the purpose of this is to get an appropriate DC point over here which allows the bias current I b in these steep to PMOS transistors and at the bottom side we have these 2 NMOS transistors where the gate voltage is expected to be close to this bias point their dimensions are also close as a result we are trying to establish or trying to enforce I b in this NMOS also. So, we are just trying to ensure that both this PMOS as well as NMOS are biased with the help of this gate voltages to establish I b current and then it will be more convenient to have the output voltage close to V DD by 2.

Of course let us to be taken care by the common mode feedback loop for the second stage so that it can adjust this gate voltage little bit across that V b so that the output voltage is very close to the desired value. Swing here is more important, swing here is not so important if you talk about swing you know that if you are going for 10 to power of 4 or larger gain the gain of each of these stages is more than 100, this is more than 100 as we have discussed earlier also the swing at this point is not too critical as compared to this is the swing here is much larger.

Especially if you are talking about the first stage few tens of microvolt of signal here you may get a few millivolts of signal and therefore, it is not going to. So, be so critical with respect to swing. So, even 100 millivolt of swing available over here is good enough 50 millivolt is good enough much more than required. So, I do not worry so much about swing here, but yes swing will be more of a concern here especially if you are having a second stage of front an amplifier with programmable gain.

Student: Sir, why we need to (Refer Time: 20:11) may made a feedback for biasing tail current (Refer Time: 20:16) of NMOS.

Because right now we have not fix this one, so we have discussed earlier an example where there was a common feedback or common mode feedback loop for the 2 stages where a single error amplifier was taking the output from the 2 you know differential outputs and it was providing the feedback here that was a single common mode feedback loop for the entire 2 stage.

That is what we have discussed earlier and here we are discussing you know 2 separate common mode feedback loop and looking at some of the details related to biasing. So, just like we are concluding that this error amplifier with NMOS as input and PMOS as load is able to handle the required reference voltage which is you know 1.4 volt close to 1.4 volt and it is also able to provide an output voltage which is suitable for biasing this PMOS. Likewise we also need to argue that different flip topology with NMOS as input device sorry PMOS as input device and NMOS as load device will be required if we are constructing another common mode feedback loop for biasing these two.

So, far we have biased we have bias the output DC point over here the common mode DC point over here with the help of first loop we also need to do the same for the second loop. However, we see that the output DC point has to be close to the V g of this NMOS

and therefore, it would be more prudent to look for NMOS load where the output DC point of an NMOS load differential amplifier will automatically be close to the V g of the NMOS and let the input pair be PMOS. So, this is the reference 1 and sorry this has to go on the other side do that and you have the PMOS current source. So, here I can put my V cm ref 2 which is the output common mode reference point.

Now, what should be the output common mode reference point this is anyway a DC bias. So, I can in the AC point of view I can put it at AC ground. So, this is again my differential amplifier the same error amplifier topology I have just flipped it. So, the load device is now NMOS input devices PMOS the source current is also PMOS accordingly and here I am going to get the V o 2 plus and this is your V o 2 minus I am going to get those over here V o 2 plus and V o 2 minus, and I have to check the polarity the way I have drawn is not proper. So, I have to would look that look at the polarity that how it is able to satisfy a negative feedback across the loop and stabilize my common mode output this level.

So, we can again trace the loop assuming that because of some reason the output common mode level over here go up if this goes up I need to increase the gate voltage over here so that it is able to pull it down. So, if because of any reason output voltage over here goes up how will you bring it down if I increase the gate voltage of these two devices little bit they will try to pull it down because the gate voltage of this PMOS is fixed and because of some reason this voltage is going up you want to bring it down.

So, only one of the option is that you increase this gate voltage so that the V gs term in the equation that becomes larger as a result it will be able to support the same current with a smaller drain to source drop. So, it will try to bring the disappoint over here lower. So, in order to do that if this is going up I need this particular output to control the gate voltages. So, the way I have drawn I just need to flip this diode connection I need to draw this way. So, this will be my output node the high gain output node. So, diode connection will be made on the other side and then I can bring it over here and connect it with both the gates.

So, this is basically this is going to complete the common mode feedback for the second stage and we also need to see what is the reference common mode over here that is required for the reference common mode this is output node and we need to worry about

swing and for getting the best possible swing I need to make sure that the output DC level over here the common mode level over here is biased midway between the 2 extremes the V out max and V out min. And we know that V out max is going to be equal to V gp plus mod V tp right. So, V out max V out I should call it V o 2 max because I have defined it as V o 2. So, just assume that the final V out I am assuming as V o 2.

So, V out max is going to be V gp plus mod V tp. Now anyway the gate voltages of these four MOSFETs are similar close. So, I can just write V gp plus mod V tp and V out min is going to be this V b the I could, I should not call this V b dash because this is the V b which is DC bias coming from some fixed reference and this is the V b dash provided by the common mode feedback. So, this is going to be V b dash minus V t and. So, for a given V b dash which is coming from the common mode feedback amplifier the minimum output level that you can have over here while keeping this NMOS in saturation will be equal to this V b dash minus V tn.

And if I just put the numbers once again if I look at the numbers V gp as I said is going to be close to say 1.3 1.4 plus mod V tp. So, this number is close to V DD close to you know V DD, close to 1.8, and V b minus V t and also again it is close to 0 because for low current value the V b which is basically the V gs of this MOSFET will be close to V t because V gs minus V t is small and you are trying to have lower bias current in this circuit. Therefore this is also going to be close to 0.

As a result the output can have almost full swing from close to V DD to close to 0 and as a result I would like to bias my output DC point or the common mode equal to V DD by 2, this plus this by 2, so 0.9 volt and therefore, this point I can keep it as 0.9 volt. And once again here we can see that why we have chosen this NMOS load, because the gate the output DC potential if I just look at this as a differential amplifier with current mirror load if I look at the steady state condition in which the effective DC potential or effective potential at the gate of this PMOS and the reference PMOS is same we are going to have same current will be branches. Approximately another result the gate voltage being same the drain voltage of this NMOS devices are also going to be same which is going to be equal to V gs of NMOS.

Therefore the drain potential of these 2 NMOS is going to be close to V gs of NMOS which is fed to these 2 NMOS also. So, that is for the output disappointed naturally close

to the gate potential of an NMOS therefore, I would like to use the error amplifier with PMOS as input device NMOS as load to bias the current sources over here.

So, this biasing scheme will also ensure that the biasing current in the second stage is close to the biasing current that you are having in the first stage I b because here what we have done is we have made the output DC point of this stage such that the V sg of this PMOS is suitable for supporting I b in these 2 branches. And likewise we have created a DC bias point at the gate through the help of this with the help of this common mode feedback once again to support the same current.

So, this will ensure that the current in these 2 stages are similar or close to the desired value. In case of diode connection MOSFET we already have output reference point if you have a single ended op amp where you have diode connected branch in the first stage there automatically we have an output DC point over here equal to V gp of this MOSFET and that basically sets the vg over second stage, so that ensure that you have a current over here which is going to be close to the current in the differential stage.

But in this case with the help of this overall common mode feedback in the first stage and the second stage by choosing the references properly in the first stage and the second stage and the amplifier topologies properly in the first stage and the second stage we are able to ensure appropriate current bias this is clear.

So, few more points regarding stability and its comparison with the single loop common mode feedback will be looking into that. And some alternatives that came up in our discussions earlier will be looking into those. So, any discussion required before we (Refer Time: 29:30) will be, I will resume our discussion after that.