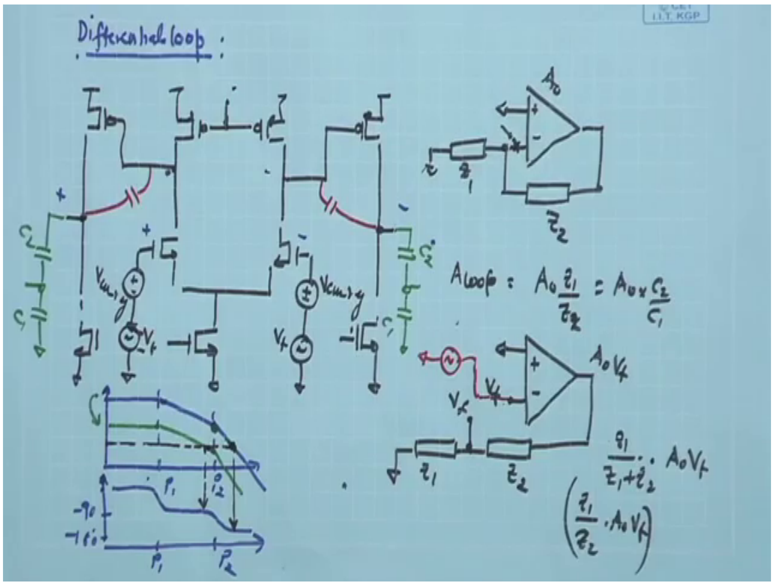
Analog Circuits and Systems through Spice Simulation

Prof. Mrigank Sharad
Department of Electronics and Electrical Communication Engineering
Indian Institute of Technology, Kharagpur

Lecture - 28
DC Biasing For Open Loop Analysis (Contd.)

Welcome back and let us resume our discussion on the simulation for the stability analysis for the common mode and differential loops. So, we have just looked into the common mode loop.

(Refer Slide Time: 00:40)



Now, let us look at the differential mode operation and also the simulation steps required to analyze the high impedance resistor that we constructed using the transistors. So, let us look at the differential loop operation.

For the differential loop if I look at the overall scheme. So, for the differential loop if we assume that you have a same common mode loop for both of them and you have stabilized the common mode, so that this point is at the DC potential required to maintain an output common mode voltage equal to the required value. And therefore, for the differential loop once again we have claimed that the same capacitor over here is going to compensate the differential loop as well and to do that we can check the overall differential operation and see how to calculate the loop gain for the differential operation.

And remember in order to look at the closed loop simulation let us go to the block level and see the overall feedback scheme that we are implementing.

So, assume that you have the feedback elements over here Z 1 Z 2 and your overall impedance or the ratio of the Z 2 and Z 1 gives you the gain and you are having the DC potential over here set to AC ground. So, this is the scheme and you are having the input signal applied over here this is a single ended version of course, for the fully differential version you can draw the other path also you have the plus minus output coming in and you have the Z 2 Z 1 feedback from the other side also and using our discussions we also arrived at the loop gain for this case. So, we said that the loop gain for the negative configuration it was given by A naught that is the gain of the amplifier times Z 1 upon Z 2 or in our case and you are using capacitor it was A naught times C 2 upon C 1 if I call this C 2 if and C 1 and we know that C 2 one C 1 you are choosing it to be small because we want a large gain maybe at least few tens.

So, it can be from 30 to 50 or even 100. So, we are choosing the C 2 upon C 1 ratio fraction a small fraction and as a result the loop gain is definitely significantly smaller much smaller than the a open loop amplifier gain A naught that we are having. And in order to apply in order to analyze the differential loop stability one of the ways is to open the loop at this point. So, when we are talking about oscillations we can set the input signal to 0 and look at the loops behavior what is the phase across the loop and in that case we can loop we can break the loop at a desired point in this case let us assume that the loop is broken at this point this is a relatively both convenient way of checking the stability and almost a similar scheme can be applied to the invert non inverting configuration as well.

So, here where you are having the input signal I am setting that signal to 0; that means, this is now applied to the DC potential and we are opening the loop over here and; that means, that we will be applying the signal at this particular point and we can test what is the feedback voltage coming at this point. So, overall you know after tracing the loop what is the signal coming over here. So, we can open the loop and see that first of all you have to confirm that yes the loop gain is same as what we expected using the shunt shunt topology that we arrived at.

So, we had discussed the overall feedback topology that we are having and we arrived at the loop gain. So, if you are opening the loop at this particular point at the negative input terminal of the op amp and then looking at the final voltage signal coming over here we need to be sure that yes your feedback signal over here the overall transfer function between the V t and the signal over here is also similar to what we ah achieved earlier. So, here we can see that the other terminal is at AC ground therefore, the output signal over here is going to be eight times V t and here you are having the V f if you look at the signal coming over here after this divider that is going to be V f which is Z 1 upon Z 1 plus Z 2 times A naught times V t and also we know that in order to get large gain we are having the Z 2 which is much larger than Z 1.

So, I can ignore the Z 1 in the denominator and then I have Z 1 upon Z 2 times A naught times V t. And remember we did a similar we took the similar approximation when we did the shunt, shunt feedback configuration and analyze that particular feedback configuration we opened the loop by grounding the Z 2 from the input point to the ground and then we converted the input signal into equivalent current source and then Z 1 one also coming in parallel with Z 2. And then since you had the in the parallel combination Z 1 dominating we took Z 1 has the input point. So, there also we ignored this parallel combination of Z 1 Z 2.

So, here also we can ignoring the Z 1 in terms of Z 2 in presence of Z 2 because this is a much larger number and therefore, we can see that the loop gain is same as what we expect, but we arrived at using the exact analysis as well. So, now, in order to do the stability analysis for this particular amplifier we need to apply a test signal at the negative terminal as we are seeing over here. So, our test signal will be applied here and we need to look at the signal coming at this potential divider V f to get the overall phase margin and what we can see is definitely apart from A naught you have this down scaling factor given by Z 1 upon Z 2 which is going to reduce my loop gain for the differential operation significantly as compared to the common mode case and therefore, a reduced loop gain may automatically imply and improve stability for the differential operation.

So, assume that for the common mode amplifier, common mode error amplifier that was having diode connected load and as a result the gain of that stage was relatively small close to one and also the that connected load do not provide significant impedance and hence the poles provided by the diode connected load error amplifier would have been at high frequency. So, I do not really count the poles provided by the error amplifier they are relatively at higher frequency and also the gain of the error amplifier was significantly small. As a result for the common mode feedback case also the magnitude of the loop gain was similar not exactly same, but similar now why not exactly saying that you can recall that you know for calculating the common mode loop gain you have to see the gain from this point to the output over here the common mode output over here and they are rather than ro by 2 you get ro because the impedance looking down into the drain of the MOSFET was pretty large. So, otherwise the order is similar.

So, you have the gain from this point to this point given by gm ro and finally, from this point to this point another gm ro by 2 and the common mode error amplifier it is having close to unity gain provided the error amplifier is having diode connected load when I refer to diode connected load; that means, both the sides having you know diode connection. So, in that case the overall loop gain for the common mode is close to A naught or in all with of the order of A naught very close to that whereas, for the differential loop we are seeing that you have another factor the Z 1 upon Z 2 coming which is anyway suppressing the loop response or the loop gain and if I look at the board plot for example, for the magnitude and the phase response.

So, what we are seeing is that the poles of these 2 case poles in these 2 case are almost remaining similar right. So, if I look at these 2 cases for the common mode feedback loop what you are saying is the critical poles are at this point and this point and therefore, only thing is the impedance over here if you are looking at the common mode analysis rather than ro by 2 becoming ro that is what we have discussed earlier and we will go into that little bit more detail we will look into the derivation of the impedances that the cascode node when we look enter the cascade, coded cascode amplifiers. So, if you are not clear about that you can wait for a while and the final output stage is also having almost the same small signal resistance and the capacitance therefore, the overall poles at these 2 points will remain almost close.

So, if I look at the phase response the phase response should be more or less similar. So, overall phase response if I look at the first point it will be you know showing 90 degree in the second point approaching one (Refer Time: 10:40) degree something like that. And the magnitude response for the original case for the common mode case if I say for the after the first pole minus 20 db per day k and after the second pole minus 40 db per day k that is what we expect if these are the p 1 and p 2 which are almost similar for the 2 cases.

And now if I look at the case of the differential response for the differential loop what we are seeing is there is definitely a shift in the gain. So, poles are remaining more or less similar the gain; however, is shifted down right because you are having this C 1 upon C 2 where is Z 1 upon Z 2 factor. So, the entire plot gets shifted down. So, I have this entire plot getting shifted down, poles remains similar only thing is the magnitude of the gain has been suppressed for the differential case because you are having this additional feedback factor coming into picture in the open loop analysis and therefore, if I try to compensate the common mode loop using a cc and try to make sure that you are achieving a 0 db while your frequency reaches p 2, I would say the differential mode is over compensated right. So, for that the phase margin will be even much better because if you are assuming you are suppose you know I have drawn it such a way that the p 2 lies.

So, suppose my 0 would be point is coming over here this is my 0 db point for the common mode loop the phase margin for the common mode loop will be given by the phase at this point whereas, for the differential loop the common the 0 db point will be coming much earlier as a result the phase margin will be given by this point. As the result the differential loop will automatically have a better phase margin as compared to the common mode loop right and that would imply that if I look at the stability of the common mode loop alone and try to compensate it using the cc I will require relatively large cc to shift my frequency response toward the lower size or shift one of the poles towards the lower side. Whereas, for the differential response it will end up having even better phase margin and because the gain is lower we do not need so much compensation for the differential loop therefore, it may be better if we can you know decouple these 2 compensation and try to have more aggressive compensation for the common mode loop as compared to the differential loop.

So, this is just one point before we go into the you know other amplifier topologies through which we can compensate the common mode loop separately and differential loop separately will look into that, but this is just to you know notify you of that point.

So, what we are seeing is that for the differential loop analysis this is the way we can break the loop apply the test signal and observe the final loop response at this point and for that this is the overall loop gain in odd times Z 1 upon Z 2 and therefore, now if I want to look at the DC bias points to be taken care of while breaking this loop.

Let us draw the transistor level schematic and make sure that the DC bias points are maintained while we are opening the differential loop we can let me see whether we can be can it be done over here. So, when we open the loop over here for the differential case both the sides we are ultimately going to put the Z 1 upon Z 2 from this 2 outputs to the ground that is what we are doing. So, from both the outputs you will be putting the C 1 C 2 ratio that you have to the ground. So, for the fully differential operation you are having the C 1 C 2 both connected from the output to the ground.

So, and you are going to look at the feedback or the loop gain will be observed by checking these 2 signals while you are applying an input signal at the 2 inputs differential input applied at these 2 points and finally, looking at the output signal over here. So, if I define this as my say positive input and negative input I know that this is now going to be my positive output and this is going to be my negative output. As a result if I want to see the overall loop response if I apply a test signal over here if I apply an overall test signal V t between these 2 terminals plus minus I will look at the final output response over here, his is your plus minus so that I can get the overall loop response.

And once again while opening the loop we have to make sure that the dc, but bias point over here is same as what we had during the closed loop condition DC bias point over here is once again being provided by the common mode feedback. And if you assume that the common mode feedback is stable separately this is not going to change much, so all we need to do is use a proper DC bias point at both the terminals. So, assume that this is equal to the output DC mode common mode that we have set. So, you are going to have the V cm ref applied over here same DC point remember in our circuit also we have the used the resistive feedback to set the input common mode same as output common mode.

So, in this case output common mode point was over here if you are using the same common mode feedback loop and therefore, I am setting the input DC level equal to the bcam ref and on the top of that you will be applying a differential signal V t likewise here I can apply the same potential V cm ref and apply differential signal say minus V t. So, you put this V t and reverse of that minus V t can be applied over here.

So, in that case it becomes a differential signal applied between the 2 inputs and then finally, we are going to look at the output potentials over here. So, if the similar applied over here is anyway fully differential the test signal that you are applying at the input is fully differential the output signal over here is not going to have any significant common mode therefore, common mode signal is anyway 0 and therefore, if you are having the common mode loop you know that the output signal over here output DC potential over here is also going to the common mode error amplifier and its feedback will be coming at this point.

And since there is no signal no common mode signal ideally at this point that loop is not going to have any signal coming over here this is just a DC bias point. And also here we have seen that for the combined common mode loop if you are having single common mode loop we have also reduced the impedance with a common mode error amplifier by using a diode connected load and as a result that is not going to contribute to a significant pole and assuming that that stage whatever poles are coming that is much higher than the poles coming at the 2 outputs of our main differential amplifier.

So, if that assumption is true I can just let the common mode feedback determine the DC bias point over here and then apply the test signal plus minus V t at this point and look at the output potential signals coming at this particular point to observe my overall phase response for the open loop case. This is a capacitive divider and here I do not so much worry about that DC potential. So, here I do not need to maintain DC potential. So, I just need to look at the AC signal over here the DC potential should be maintained at this point and also over this point.

So, in this case since the common mode feedback is active it will anyway make sure that you know output DC potential is close to the required values. So, I do not really need to worry about the biasing of the output DC potential because that is already is showed by the help of the common mode feedback error amplifier which is already making this output equal to the V cm (Refer Time: 19:13) only thing is that if you are getting rid of the resistive feedback, for simplicity this RF there were considered between the input to the output side if you are getting rid of that then you will have to apply this DC potential over here. Remember if you also even if you keep the RF connected, if you keep the RF connected like what we have now you know we will draw the RF become complicated because you have the plus to minus coming.

So, this has to connect over here and this has to connect over here for the RF, now if I connect that RF and then assume that this DC potential will be you know determined by the RF what will be the problem if you apply an AC signal with 0 DC the DC potential at the gate will be 0 right. So, if you assume that you have put the RF the feedback resistor between the output and the input and positive output in the negative input like we did for biasing and then you apply a test signal if the test signal is only AC with DC potential 0 that will set the DC potential over here also 0 and then your amplifier will not work correctly. So, in that case also you any way have to put this DC potential over here equal to the V cm ref that you want if you in that case the RF (Refer Time: 20:32) is not playing any role anyway. So, you can eliminate it altogether even its present will not matter much.

So, you can confirm that even if you have RF between these 2 points that high impedance resistor that you impermanent using transistors. Even if you have that connecting between these 2 points it is not going to hart much in the overall simulation because it is very high impedance it effectively it is not contributing much to the overall frequency response apart from of course, you have the high frequency behavior that comes into picture when you loop the (Refer Time: 21:30) that the closed loop response and you have that high pass filtering mechanism provided by this RF, but for stability analysis it will not play a very significant role.

So, to be accurate you can you know always keep the RF over here, but even in that case you need to make sure that you are using a single source over here with a DC level equal to V cm ref and then on the top of that you are applying the extra signal V t for testing and then you are obtaining the output signal over here. And then phase response will be given by the gain from you know the this point to the final output at the division of this capacitor. This is how you will be looking at the phase response for the differential operation.

Student: Sir (Refer Time: 21:41) this (Refer Time: 21:42) even add down or some DC.

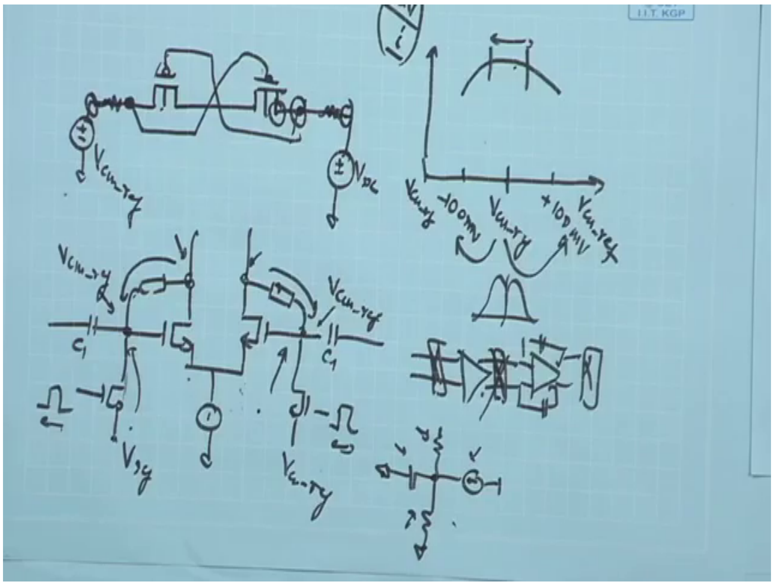
It will not matter much it will overall response is not matter much because this is anyway in the actual operation it is connected to the electrode and you do not have much control over the DC potential over here.

So, that is anyway decoupling the DC bias of the amplifier to that DC from the DC any DC level that you may have the electrode. So, it putting it is not very necessary to put an appropriate DC bias for here because this is the input point rights in your actual circuit this is the input point which is coming from the electrode and we do not have control over the DC potential provided by the electrode. So, even if we put it to AC ground does not matter much because anyway this is not passing any dc. So, it is not influencing the DC bias of the amplifier in any way.

Student: (Refer Time: 22:33) they will high pass filter.

We have discussed right. So, while determining the value required for RF we look at the high pass response because of RF and the C 2 that you have and that must be able to pass the desired signal and that only give us the value of RF, because this RF produces the high pass response that is what we had looked at if you look at the RF that the way we created it using the transistors.

(Refer Slide Time: 23:02)



You have remember the connection strengths are only at the dot wherever you are the dot this is no connection and here also you look at try is this and try to find out the impedance of this we can one easy way to do it is apply a DC potential over here which is V cm ref and then apply same you know some V DC over here and in the DC sweep analysis basically you can try to look at the overall variation of the current across these resistors. So, you can put a marker over you can put is marker over here and then look at the overall or basically marker and the source of this pmos and then over all I you can plot as a function of V DC. So, V DC needs to be swept across V cm ref. So, V cm ref plus minus say you know plus minus 100 millivolt or even few tens of millivolt because remember this could say potentials are not going to change too much. If the difference is too much this resistor will not operate as a very high impedance device because there are several other leakage mechanisms also which start building up when you have larger potential difference across this.

So, for example, if you have larger potential difference between this point and the other point, so the potential between gate and substrate also go on increasing as a result the gate to substrate leakage should also start increasing and then in that case this device does not behave like a very good resistor.

So, it will behave like a good register within some range plus minus few 100 millivolt or across the 0 potential difference. So, if I am looking at if I am this V DC is at V cm ref then of course, the potential difference across these 2 is 0 and then if you increase it that a potential difference increasing and then if you decrease to V cm ref minus 100 millivolt this is V cm ref plus 100 millivolt. So, if I am going from V cm ref to V cm ref minus 100 millivolt the potential difference across this is you know negative and if I am going towards higher one this is increasing in the positive direction and you can put the marker and straight to see what is the overall current being transmitted from this point to the output point and there from there you can obtain the delta V that is the potential difference between the 2 inputs that do DC points divided by the current flow and that is going to give you the overall impedance.

So, the impedance characteristics may look like something like this for smaller differences it gives you a high impedance, but as the potential difference increases because of increasing leakage components say the leakage component between gate and bulk and the gate and the junctions it will lead to reducing impedances that is what we expect if you plot the I divided by delta V that is the V DC minus V def. So, here I have floated up of course, the you know absolute value you can plot it across the delta V also and that is this will be the origin 0 and you will have plus minus handed millivolt on both sides and then you can look at the impedance that is changing over here.

So, this is you know the delta V upon I that you are plotting over here in terms of impedance. So, this is the whole characteristic that we expect. Remember if you do transient analysis with this kind of resistor because the resistor value is very large it will give you a very large RC time constant. So, if you are trying to set up some transient simulation where such a large value impedance is connected between the output point and the input point. So, you are having this huge resistor that you have constructed using this transistor and then you are having the input applied to the capacitor C 1 C 1 and you are having some inputs applied over here. So, if you do the transient simulation it will take time to for the DC value over here to settle to the required values in this transient simulation therefore, this value may start from some arbitrary value some arbitrary voltage and it may take some time for this resistor to charge this voltage nodes to the value is equal to the common mode output.

So, in the transient if you just calculate the RC time constant it will be you know fews you know second order of few seconds therefore, if you are trying to run transient simulation for few milliseconds in order to simulate a low frequency signal it will not settle within that duration. And in simulation if you try to run a simulation for such a long time few seconds to just allow this potential (Refer Time: 27:48) it is going to waste a lot of time. So, one of this final technique to do that or you know make it fast is to have some initial condition. So, in the simulation if you have if you are putting some initial conditions

So, that these 2 potentials are initialized to the value equal to V cm ref, in that case you will not be dependent upon this resistor values to start from that or initialize or set up this value equal to the V cm ref we are initializing this potential; that means, rather than starting with an random DC potential the simulator will start by putting this 2 potentials at the V cm ref and in that case since these 2 potentials are anywhere quickly set to the V cm ref by the help of common mode feedback which is going to operate much faster. It will ensure that in a long run also as your simulation goes on this potential is maintained at V cm ref. So, while doing the transient analysis you should just be careful of this fact that if you run the time domain analysis without initializing these 2 node potentials it will take huge amount of time just for these potentials to arrive at V cm ref DC potential. So, you have to basically initialize it to the desired value and then let that targeted stimulation it run.

So, you would be careful about running the transient simulation with this kind of large value feedback resistors.

Student: Sir how (Refer Time: 29:10) switch.

That is another way, but you have simulation options are also there we will check that in the LT spice or even in cadence you have simulation often where you can apply these (Refer Time: 29:20) conditions to some nodes even in the spice simulation. Generally when you write code for the spice simulation there also you can specify initial condition using in it statement you can you know put some initial voltages that required points. Other option is that of you if you want to use a DC source. So, that you are connecting some switches over here and you know t equal to 0 you have provided some DC potential over here which equal to the V cm ref as you suggested V cm ref and here also V cm ref you can put this for a very put this on for a very short time. And since this resistance is very small the transistor resistance is any way very small as compared to others. So, this will ensure that this is getting charged quickly and this duration is very small. So, it is getting on temporarily and setting this to the required V cm and then after that you turn it off that it does not significantly affect your overall performance that is also possible to do.

Student: (Refer Time: 30:21) one second (Refer Time: 30:24).

Because if you remember we have used this in our earlier simulation when we did not consider the chopper operation and all if you are just looking at the lobe a cutoff frequency of around 0.5 hertz to 1 hertz allows ours content for the signal to pass in that case the cutoff frequency was chosen as around the you know one hertz or lower than that close to that. So, accordingly the RC time constant will be close to that. But now once we have chopper operation and we are relying on chopper to mitigate the noise then of course, we have seen that the entire signal is shifting towards higher frequency and then you need to pass that high frequency and you do not really need to worry about the one upon f noise so much, but in case for example, in the next stage suppose you have the first stage where you have the chopper applied and after that you have subsequent stages. So, chopper generally presented by this kind of switches. So, you have the chopper applied only in the first day after that you have the anti chopper and signal is coming back to the you know lower frequency.

And then the second stage is having again that kind of capacity feedback for further gain or you are having filters with the help made with the help of these capacitors feedbacks and all. So, for the second stage amplifier once again you will need to apply that kind of feedback to settle the input potential at the same point and then on that condition once again since you have anti chop the signal a signal is that low frequency and you are not applying any chopping over here.

So, once again you may need to take care of the feedback resistor also in many cases it may happen that you do not apply chopper after the first page rather than that you apply the chopper directly after the second stage only that may also happen in that case the both the amplifiers are basically processing high frequency signals.

Student: Sir (Refer Time: 32:04) some mathematically (Refer Time: 32:08). So, why will it take both one second dot (Refer Time: 32:11).

Is not mathematical simulations if you are using time domain simulation it is basically solving mattresses at every time step.

So, just like you do a scale kvl at every time step it will be solving kcl, kvl finding out the next DC condition for each circuit points each nodes and then again finding out the you know small thing the resistance value in the capacitance values at every point and again solving the kcl kvl at the next time step. So, it is basically you know in the transient simulation it is something like a metric simulation every time you have some some spice circuit resulting from the DC conditions you have some capacitor resulting from the MOSFETs, you may have some dependent current source which some value dependent upon the MOSFET parameters. So, there are so many you know these are the MOSFET also ultimately even is a look at the large signal model ultimately it will be breaking down into equivalent resistors capacitors dependent sources.

So, it will break down the entire circuit into these elements like resistors capacitors dependent sources voltage dependent current source current dependent voltage source like that and every time step basically depending upon the DC condition different different nodes the value of these capacitors resistors will change. And as a result once again state taking the previous step values of the voltages at different different node it will try to solve the kcl for the next time step taking the current values and again find out the resulting voltage and likewise ultimately it forms a matrix of all these nodes. So, when you solve kcl for large number of nodes ultimately it is form of a matrix and it solved that matrix for every time step why updating these you know capacitance values resistance values which are bias dependent or voltage current dependent. So, every time stable to keep solving that matrix therefore, here also it will do the same thing.

So, it is something like doing the exact behavior simulation. So, it is it will simulate in a way the real current is going to flow and it will take as many time steps to settle the value at as it would require for a real circuit means in terms of you know simulation step. So, in the real circuit of course, if you are it will take say one second to settle this voltage to the required value likewise in the simulation to simulate that one second it has to simulator so many matrix equations depending upon your step size. So, it will take many many such matrix equations and finally, you will be arriving at that one second point.

Student: Sir, in this simulation current volts inverse (Refer Time: 34:46).

So, that may be because you know have having the bulk contact also. So, since you are talking about very small current and the potential differences are increasing. So, the bulk to substrate to get potentials are decreasing or changing and as a result you may have some leakage paths also which are contributing to the current. So, if the potential difference increases all those leakage paths also become stronger as a result you will not get exactly same current you have other paths also from the leakage.

Student: So, in the calculation of resistance (Refer Time: 35:18).

The best thing to do is look at the, so this is a valid mainly in the small region. So, as long as the voltage differential called these 2 is small few 10s of millivolt to 100 millivolt it is valid after that anyway this will start dropping because of other leakage currents coming into picture. So, strictly speaking this is the right region beyond that because of leakage starts dominating in other paths it will not give you a very high resistance. The better way to do is you put a small resistance over here and then you know measure the current flowing here and measure current flowing here or even from the source stage you can you know in the select the upper terminal of the source is in the simulation that will also give you the current flowing through the sources and both the sources. So, you can check how different they are that will give you that there will tell you that in the central region maybe it will be very close, but as you diverged from this 2 it will become different.

So, this scheme will be valid only for this central region where other leakage components are not very significant the especially the gate to you know bulk leakage and likewise we are having the bulk to junction leakage they are not very significant that the potential difference starts increasing then both of them will be having more leakage company other leakage component coming into picture. Here they are interested in the source to drain current source to drain current other leakage component like junction to bulk leakage or gate to bulk leakage that will know destroy the factors to that we are looking for.

So, as the potential difference across the gate and the you know source increases or you know gate and the bulk increases it increases all those leakage component exponentially because that is mainly based on tunneling effects especially if you go for a scale technology 180 nanomometer still it is if you go for more skill technology those leakage component will be even stronger and implementing this will be more difficult. In fact, you will have to go for high oxide thickness MOSFET. So, that those leakage components do not come into picture.

Even if you look at the AC analysis if you are putting an AC signal over here and trying to do AC analysis there also you have the other parasitic capacitances coming into picture. So, that will also need not give you the right r value. So, I can think about three analysis I said DC AC or you know transient. So, (Refer Time: 37:28) transient definitely that is not a good way because it is going to have you are going to have very large RC time constant and is not going to let the current flow as fast as you want the other option is you if you are doing AC analysis you put the AC frequency very low maybe you know 0.1 hertz or something like that and then the time strip in the simulation has to be reduced accordingly, sorry increase accordingly.

So, if you increase the time step in the simulation and then use a very low frequency AC maybe you know 0.1 hertz or something like that then basically AC analysis will be able to work. So, only thing is the AC frequency you are applying over here for transient that should be much lower within the RC time constant provided by this transistor then it will still work for that you need to select an AC signal with the frequency very low and use a very large time you know step. So, that for a given long duration say few seconds the signal is able to you know follow the applied or the current is able to apply the follows applied signal. So, resume our discussion in the next session.