Analog Circuits and Systems through SPICE Simulation

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Lecture - 18
Common Mode Feedback

Hello and welcome to today's session.

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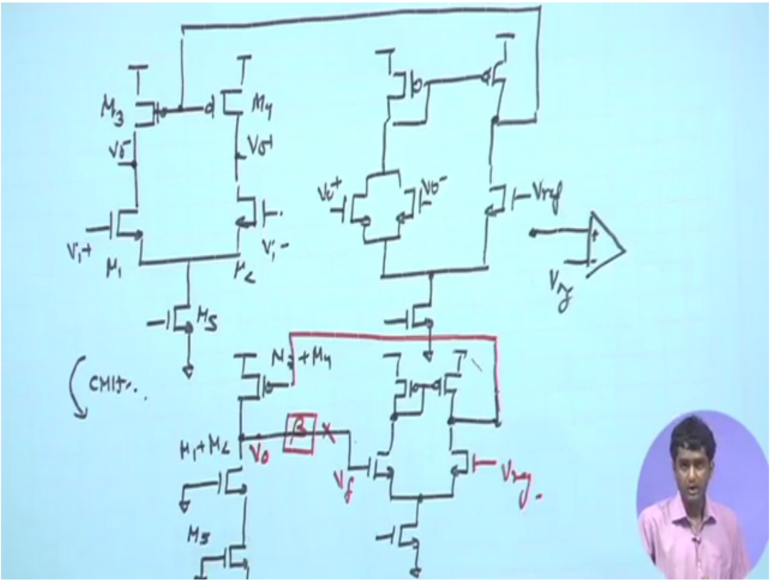

So, we will start from exactly where we left in the last module continuing with the stability analysis of the common mode feedback. So, this is our fully differential amplifier where we left last time and we are establishing the common mode dc bias for this fully differential amplifier with the help of this auxiliary amplifier or the differential amplifier with current mirror load, and we saw how these two differential pairs they are helping us in extracting the common mode level of the fully differential amplifier and providing a feedback bias voltage for the PMOS transistors. So, that an appropriate common mode voltage close to the required value V ref is established in the main amplifier.

And then we look at the common mode half circuit. So, we are looking at common mode signals or common mode dc point, we said that these two signals drain potentials are going to be close together, they are going to be exactly same if the transistors are matched and you have a common mode dc level applied over here.

So, in that case for the common mode half circuit specially if you are talking about only the dc bias point, assume that we have a common dc level applied at both the inputs as the result both the drain potentials are also at the common dc point, and any signal appearing at this point is going to appear at the gate of both these PMOS transistors another result both these drain potentials will also change in the same fashion because of any signal appearing over here. Therefore, for common mode analysis the tie them together and therefore, the two PMOS transistors and NMOS transistor were combined together to arrive at the common mode half circuit (Refer Time: 02:01) call this M 1, M 2, M 3, M 4 and M 5.

So, this I can write this as M 3 plus M 4 and M 1 plus M 2 and M 5. So, we are talking about dc potential. So, gates of M 1 and M 2 both are at dc bias points. So, I can put an ac ground over here like white the gate of M 5 which is the tail current source, that is also at the dc bias point with the help of a reference current mirror for example,. So, we can put a c ground over here as well.

Now the output of this stage as the now is going to the error amplifier. So, basically I can sit, I can put a symbol for this error amplifier; now if we look at the common mode dc point that is the both outputs over here tie together therefore, both these potentials are also going to be same. And therefore, if I look at these two transistors, they are having the same gate drain and source potential once again therefore, I can just combine these two into a single transistor, and we know that under that condition the w by l and the id of the combined transistor will be same as that of the other transistor. Remember as per our earlier discussion this was having half w by l and half id as compared to the other transistor.

So, now, for the common mode operation since these two gates are going to be combined together, we can represent it as a single device and as a result we arrive at a configuration which is something similar to our standard de femp with current mirror load, and we have our v out basically going to the output using the feedback signal. So, just to keep things separate and here we have the V ref. So, here if we look at the overall operation if we remember our analysis if we represent this error amplifier as a symbol and then look at the terminal definition we had said that the reference signal is at the negative terminal and this one is at the positive terminal right.

So, the actual Vcm that is coming from this combined transistor that is actually behaving like the positive terminal and V ref is the negative terminal. So, that if the Vcm goes up; that means, Vo plus plus Vo minus by 2 goes up this should also go up and as a result that the PMOS gate voltage should go up and should bring the common mode voltage down. So, by our definition the actual common mode signal coming from the differential amplifier is applied to the positive terminal and the reference was applied at the negative terminal.

But now for this feedback analysis, we have another stage added over here if you look at it. So, this is basically inverting stage. So, if we break the loop considering the input signal to be the V ref and see how the signal is propagated through the loop we will see that with respect to V ref this one is a negative one negative output definitely because if you increase the V ref this reduces the inverting terminal with respect to be V ref.

But after that you have another inverting stage. So, this is something like a common source stage where M 3 plus M 4 is acting like the input device and therefore, we are going to have an another inversion over here. So, with respect to V ref, we will get non inverting gain to this point from here to here one inversion and then back after tracing the loop from M 3, M 4 gate to the drain another inversion therefore, from V ref to this point we have a non inverting gain therefore, for this two stage combine together we can say that this is a overall non inverting terminals on which we are applying the input and the feedback signal as we have seen yesterday can be seen as voltage sampling. So, whatever final voltage is coming over who over here that is directly applied as the feedback voltage on the other terminal of the differential amplifier, which is effectively the negative terminal.

So, here is our sampling network which is sampling the output voltage produced by the second stage, and it is applying that sampled output voltage to the effectively inverting terminal of this overall two stage amplifier, formed with the help of the main differential amplifier and the common mode feedback amplifier. So, now if we therefore, open this loop assuming this sampling factor to be unity, we can say that you are having a input signal applied at the positive terminal you are having the voltage, the non inverting amplified voltage signal coming back which is finally, applied at the negative terminal.

So, then you increase this input signal V ref in the positive direction, the Vo also goes up, but that is applied to the negative terminal therefore, it is subtracting from the applied input. So, basically we are having series connectivity at the input the feedback voltage is effectively between subtracted from the applied input signal V ref. And at the output whatever Vo is produced we are directly sampling it choosing the unity beta factor and applying it to the negative terminal therefore, you have a shunt connection at the output therefore, we have a.

So, the shunt configuration and while opening the loop for a three shunt configuration we can see that for the beta network over here if you are looking at the output port of the beta network, the overall impedance seen looking into the output port, irrespective of the overall impedance seen looking into the input port of the feedback network, the configuration is shunt and therefore, we will be applying overall ground terminal over here.

So, let us draw the open loop consideration, looking from the output port of the feedback network the other terminal is shunt and therefore, as per our earlier discussions on feedback topologies in order to open the loop, the shunt terminal will be grounded and therefore, you just have an ac ground established at this point effectively while opening the loop and likewise if I am looking at the feedback network from the input side. Remember this is the input side of the feedback network because here you are simply the sampling the output voltage, and with the unity gain you are transferring it to the output point. So, if I am looking at the out input port of the feedback network once again at the output port we have series connection and for series connection we know that we need to open circuit that point.

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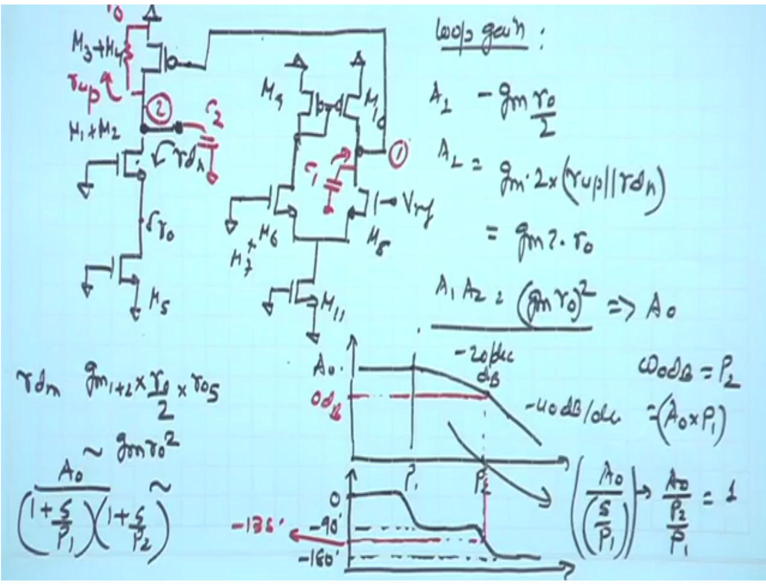

And therefore, once again looking from the input port of the feedback network, we will just open circuit this point an as a result you will have open terminal coming at the final port.

So, as a result we can draw the equivalent open circuit for this feedback amplifier. So, as I said looking into the input port of the feedback network other end is serious connection as a result we open circuit it. So, we are left with an open circuit over here and on we have the V ref which we are assuming as the input signal, and bias point all the dc connections dc bias point set to ac ground. Once again in by looking into the output port of the feedback network, the other terminal is shunt connection we are sampling the output voltage.

So, looking into the output port of feedback network, the input terminal was having shunt connection therefore, we will just put a ground over there therefore; here we just put an ac ground. This is an equivalent open loop circuit for the corresponding to the common mode feedback loop, and in order to find out the stability we need to look at the overall loop gain starting from the input point coming back to the final output over here, we are going to calculate the overall loop gain and find out the critical poles in the circuit to alive at the overall frequency response.

So, let us first look at the loop gain. So, for the first stage we have our differential amplifier constituted by the input transistors I can name them say M 6, this is the combine I would say M 6 plus M 7, M 8, M 9 and M 10 and call this M 11. So, the loop gain will include the gain of the first stage from the input to the output over here, and then finally, the second stage from the input to the output over here. So, for the first stage we know that the gain of this differential amplifier from the input to the output is minus gm ro by 2. Here the gm will belong to the input pair gm 8 for instance and ro will belong to the M 8 and M 1. So, if I assume that ro of M 8 and 10 in are almost equal then I can say ro 10 parallel ro 8 divided by sorry times gm is going to be the gain of the first stage. So, that is pretty straightforward as we have done it for the definition amplifier with current mirror load earlier.

Now the gain from input of the second stage to the output of the second stage, once again this is something like a common source amplifier. So, with respect to ac analysis these terminals are ac ground, you are having the input at the gate of the PMOS and you are taking the output at the drain of the PMOS; you are having an effective load resistance over here. So, this is something like a common source amplifier with PMOS as the input device with certain load connected what is the load impedance if we look into the drain of this device.

Student: (Refer Time: 13:22).

We know that whenever we have this kind of stacking of transistors, the stack transistors boost the overall impedance looking into the drain. So, here we have overall gm we can call it gm 1 plus 2 times the overall ro. Now what is the ro of the combining transistor if we want to be exact the total current flowing through the pair of course, is just double the ro of the individual transistor as we know, and as a result the ro of each of these is going to be ro of the combined transistor is going to be half of the ro of the individual ones. So, I can just write down ro by 2 and in fact, this gm 1 plus 2 can write it down as 2 gm and this times the ro of M 5; so ro 5.

So, this is effectively the overall small signal resistance looking into the drain. So, we get a factor of gm ro square. So, whenever we have stacked transistors looking into the drain of the NMOS we will have overall impedance given by the resistance in the source that is ro multiplied by gm ro of the stack transistor. The gm ro of this transistor multiply it by ro of the bottom transistor gives as the impedance over here. So, this is your r down if I call it r down and therefore, if I am looking at the PMOS transistor over here, it has its small signal resistance from drain to source as well ro and therefore, the overall gain of this stage will be gm 3 plus 4. So, I can call it two times gm times the overall parallel combination of r down parallel r up. So, here you have the small signal resistance looking up r up. So, the overall small signal resistance coming at this output node is the parallel combination of r up and r down.

So, I can write this down as r up parallel r down, and we know that r down in this case is much larger gm ro square, gm ro times ro where r up is just ro as the result the r up will be the dominating factor the smaller one will be the dominating factor as a result I can just write down the overall gain as 2 gm times ro. Another result the total gain combined A 1 A 2 is having gm ro square expression. So, overall loop gain A 1 A 2 gm ro square expression as we expect. So, ultimately we have to amplifier stages both of them active load. So, we expect that the final expression should have gm ro square term coming up.

Now once we have the gain in order to find out the overall frequency response for the open loop amplifier we need to calculate the critical poles and we need to identify which are the circuit nodes at which we are going to expect critical low frequency poles which are going to determine the cutoff frequency of my open loop amplifier.

So, from our previous discussion on the differential amplifier with current mirror load we know that this particular amplifier, offers a critical pole at the output node because here the overall impedance is highest that is ro by 2, at the other node the overall impedance is significantly smaller it is just given by 1 upon gm of the directed device. As a result this is the one which is going to offer critical pole for the first stage and if you look at the second stage we can see two circuit nodes first one over here and second one the output node. If I consider the lower node over here here we know that the overall small single impedance will be given by ro 5 parallel the impedance looking upward. Now the impedance looking upward into the source of this combined transistor M 1 plus M 2 with a single PMOS active load is going to be of the order of 2 upon gm.

So, it is of the order of you know one upon gm and therefore, the impedance looking upward into the source of this NMOS is significantly smaller as a result this pole the (Refer Time: 17:57) constant is going to be small as a result the pole frequency is going to be pretty high. So, which is not worried about this particular node; however, we have just seen that the overall impedance at this node is of the order of ro and therefore, similar order similar magnitude as compared to the pole over here therefore, this is the second I would say critical node at which we are going to have critical pole.

So, we have identified the two nodes one over here in the second node over here where we are going to have critical poles. As of now we cannot confidently say which one is going to be the dominant one whether one of these are going to be smaller or the other one is going to be larger, that cannot be said in a straightforward fashion with those are them can be comparable. So, if we need to find out expression for the poles at this point, we need to figure out the overall parasitic capacitances.

So, basically following the standard procedure that we have learnt earlier for single stage amplifier and differential amplifier, we can figure out the overall parasitic capacitance at this node and the second node by counting the contribution of all the transistors, wherever we need to apply miller effect we need to apply the miller effect to break down the capacitances between this node and some other terminals in the signal path and in some cases the capacitance directly appear between this particular node and the ac ground.

So, accounting for all those we can figure out the overall parasitic capacitance between particular node one and ac ground. And that will give me total C 1 likewise at the output node we can find out the total parasitic capacitance the total effective parasitic capacitance between the output node and ac ground by counting the contribution of parasitic capacitances for all the transistors and that is going to count as C 2. And we also have the r equivalent at this two point I will call this r 1 and r 2 and that is how we are going to get that two poles P 1 and P 2 at these two points and once we have these two poles and assuming that other circuit poles like the pole over here like the pole at the source of M 1 plus M 2 they are at efficiently high frequency. So, if we make that assumption and for the time being considers that these are the only two dominant poles and all other poles in the circuit direct sufficiently high frequency, I can draw the overall frequency response assuming only two critical poles in the circuit.

So, let us do that. So, the magnitude response for A 2 pole system at low frequency you have an overall gain given by A 0 which we have just found out, and we have two critical poles P 1 after of the first pole we know that the magnitude drops with minus twenty db per decade and you have the second pole P 2 after which the magnitude drops with minus

40 dB per decade. So, we have and likewise if we talk about the phase response. So, at low frequency we start with overall zero phase from input to the final output we have a zero phase, remember there is a minus one term in the loop coming because the final output signal is applied at the inverting terminal.

So, that gives automatically a minus 1 factor and hence 180 degree phase shift across the loop. So, effectively what we are having is 180 degree phase shift is already available. So, we are keeping that as a you know constant factor apart from that,if you look at the signal phase from input to output that is starting from the very low frequency ideally it should be at 0.

So, we start at 0 and we know that immediately after the first pole it reaches 90 degree, and immediately after the second pole it dropped down and approaches 180 degree priority has a third pole lying somewhere close it will approach 180 degree pretty first. So, remaining upon how close is the third pole. So, if you do not have the third pole we know that it will asymptotically reach 180 degree at very high frequency, if you have a third pole line somewhere close then it will quickly reach or touch 180 degree or go further negative as well.

So, this is the overall shape of the frequency response we expect, and now in order to get a stable response we have discussed earlier that we need to ensure a good phase margin at least around 45 degree of phase margin. So, that in the overall closed loop response we do not have any ringing and with respect to parameter variations with respect to process variations also we have enough margin. So, we need to make sure that the at the 0 degree crossing point, at the frequency at which the gain drops to 0 dB that is unity gain frequency, the phase is sufficiently lower than 180 degree lower means magnitude point of view it is lower than 180 degree or more positive than minus 180 degree.

So, if we draw the marks here you have minus 90 degree and far away from P 2 you are reaching or approaching minus 180 degree. So, we would like to make sure that the at the 0 dB causing frequency that is the frequency at which the gain drops to unity the phase is sufficiently positive, sufficiently higher than minus 180 degree and in strict sense if you want to achieve phase margin of exactly 45 degree, we need to make sure that the frequency at which the 0 dB gain occurs the phase is exactly 135 degree. So, also we know that what is the frequency at which the phase which is exactly 135 degree in a 2 pole system, that is a P 2 the first pole we have exactly phase strict 45 degree far away from P 1 90 degree exactly at P 2, we have around 135 degree provided the third pole is far away.

So, at P 2 I have an phase which is close to minus 135 degree, and as a result I would like to have my 0 dB crossing point at P 2. So, I would like to make sure that my game drops to 0 dB by the frequency P 2; this should be the 0 dB point. And in order to achieve this condition we know the criteria that we need to apply we need to make sure that omega 0 dB omega 0 dB is our second pole P 2 in the system, and also we have seen that omega 0 dB can be expressed as A 0 times the P 1 because we have after immediately after P 1 we know that for A 2 pole system the overall expression can be expressed that 1upon s upon P 1, 1 plus s upon P 2 and in this region between P 1 and P 2 this express reduces to between P 1 and P 2 this expression reduces to A 0 upon s upon P 1 because between P 1 and P 2 between P 1 and P 2 you have s or the omega which is much greater than P 1.

We are assuming that P 2 is much higher than P 1 as a result and you are at omega or a frequency which is much higher than P 1 as a results you can ignore this one with respect to s upon P 1 and hence we are left with only the s upon P 1 term from the first factor second factor, we are assuming that the omega is still much lower than P 2 So, the omega is still much lower than P 2, as a result s upon P 2 can be ignored with respect to the one over here, another result the second factor just gives me unity another result I have A 0 upon s upon P 1 left in this particular region and if I assume that this expression is valid till I approach P 2 is just an approximation.

So, we can say that at the particular frequency P 2 we are having the overall gain magnitude given by A 0, P 2 upon P 1 and that should be equal to 1. So, we need to have A 0, P 2 upon P 1 equal to one and that gives me the relationship that the overall 0 dB point that should be equal to P 2, and we have the omega 0 dB given by A 0, P 1 because in order to equate this to one we need to have omega equal to P 1 times A 0. So, omega at which the gain touches unity is going to be given by A 0 times P 1. So, this is the relationship we need to achieve in order to achieve a phase margin of 45 degree in our overall open loop amplifier.

Now, to do that we need to make sure that the pole given by P 2 is sufficiently higher than P 1, we can see that the requirement is that P 2 should be A 0 times P 1 and as a result need to make sure that the one of the critical one of the poles say P 1 is brought sufficiently lower, it is pushed down to a sufficiently low frequency by a factor of A 0 approximately so that we can have sufficiently good phase margin. And we will see the meter to do that as we have seen earlier one of the common method to achieve such letting of pole or pushing of one of the critical port was low frequency is miller effect. So, we can intentionally add a capacitance between two circuit nodes. So, that and one of the circuit nodes the overall capacitance because of the miller multiplication becomes too high, and as a result of that the pole at that particular node is pushed to very low frequency.

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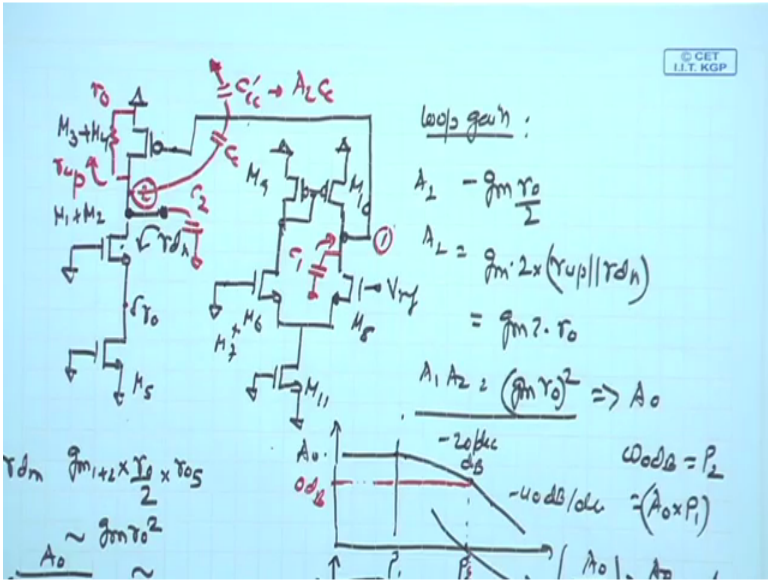

So, in this particular open loop case for example, if I want to push the node at one to low frequency, I can imagine putting a cap between this node a composition cap cc between the node one and node two as a result of which we are having a overall gain between this point one the output given by A 2 that we have just written over here. Another result what we expect is the C 1 c C 1 which is basically the equivalent capacitance coming because of this cc at the node 1 will be A 2 times c c, and other result the first node over here will be experiencing a large cap and as a result we can try to push the capacitance over here to a much lower frequency. On the other hand the capacitance over here because of the applied miller effect in the forward path the capacitance over here will be still goes to c c, because in the reverse direction it will have the factor of 1 minus 1 upon a where a is large. So, we can ignore that and as a result will just be having capacitor c c coming at this node which is much smaller than A 2 times c c.

So, here you can see that by minimal application we can try you know push the node P 1 to a much lower frequency, and the second factor that also can help us in achieving further splitting is the overall reduction in the impedance between the gate of the PMOS transistor and the output node at higher frequency. So, as we will see in one of our another example that we are going to take sufficiently large capacitor connected between the gate of the PMOS transistor and the output node, it called this produces a kind of low impedance path between the gate and the output at higher frequency may be close to P 2 as a result of which the impedance looking into the output point over here becomes smaller.

So, let us looking to that factor in the next module, we will try to see how the cc can help us in achieving poles splitting. At one side it helps us in pushing the pole 1 at towards lower frequency, at the same time it can also help us in pushing the second pole at the node to towards socket frequency and hence achieve good phase margin; and the same concept of will be similar concept will be applied in case of the compensation for definition operation as well. So, let us do that.

Student: (Refer Time: 31:14).

45 degree is a safe phase margin for which in the overall transient response you do not get enough ringing. If you have 45 phase margin lower than 45 degree within you know time domain analysis, it can be shown that it is did not lead to ringing in the closed loop response if you are putting a step input at the loop it will give you a ringing response at output.

Student: (Refer Time: 31:38).

60 degrees even better, but the design become more challenging compensation becomes more challenging. So, 45 degree is an acceptable number.

Student: Sir sir for one stage amplifier we can do this have (Refer Time: 32:03), but this multiple stages then how we analysis stage margin other thing because it can be possible that for one stage singles.

So, ultimately you have to make one of the poles dominant poles which is much lower frequency as compared to the other. So, in any case if you have three stages; so we ultimately target will be to choose one of the nodes which can be made the dominant pole, you can push it towards much lower frequency conveniently. So, that will be become our dominant pole and if there are other poles, but they are sufficiently higher frequency than this one then it is we can still meet the phase margin.

For example in this case you can if you want to further you know improve the phase margin, you can try to make the impedance of the difference pretty high. So, if you want to say make the ro of becomes pretty large by just reducing the bias current and increasing larger channel length over here. In that case ro over here will also become large and apart from cc you also have a significantly larger ro as compared to the main amplifier. So, that way also you can make this dominant. So, begins which we have assumed that the ros of this stage are similar to the ro of this state, but that may not be necessary.

So, you can intentionally make the ro of the stage much larger by applying largest one of them and having even much lower you know bias current in the stage and that will basically the hear noise consting are also you know less critical main differential amplifier you are much constrained because of which you cannot really reduce a bias current too much, but in the form of feedback amplifiers will be is less critical because whatever noise comes it comes in the common mode.

So, because that you can reduce the bias current of this one more aggressively and you can apply longer turbulent as well. So, that the ro of this stage becomes the dominant one that will help you in you know pushing the pole one to that you can see.

Student: Sir when we are not simply is the composition capacitor between node one and round.

Because you will not get the better composition (Refer Time: 33:59) multiplication we will need much larger capacitor in that case.

Student: (Refer Time: 34:02).

So, the capacitor is area hungry you would if you want to exploit measure capacitor, that will that will help you save area otherwise you will have to go for much larger see. We will resume the discussion.