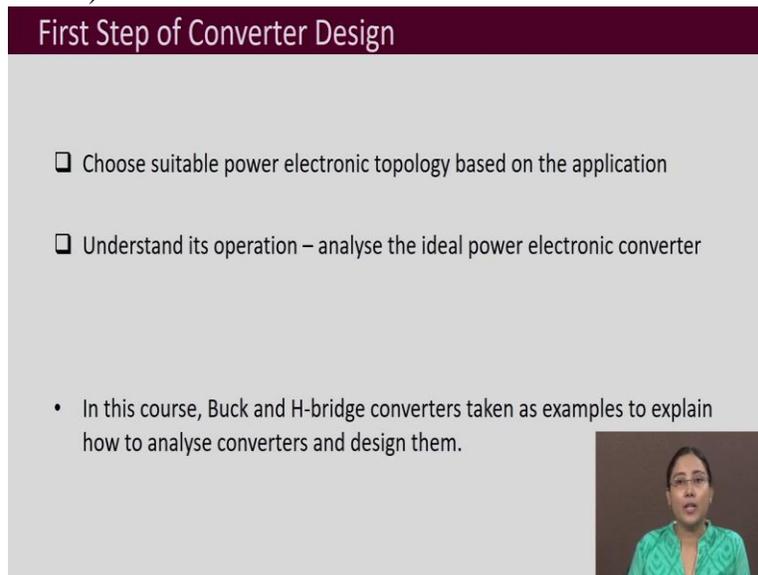


**Design of Power Electronic Converters**  
**Professor Doctor Shabari Nath**  
**Department of Electronics and Electrical Engineering**  
**Indian Institute of Technology, Guwahati**  
**Lecture 02**  
**Analysis of Buck Converter**

Today, we will begin with the module analysis of power electronic converters and the first lecture on it is going to be analysis of a buck converter. So, the first step in converter design is that you have to choose a suitable power electronic topology for that particular application.

(Refer Slide Time: 00:53)



**First Step of Converter Design**

- Choose suitable power electronic topology based on the application
- Understand its operation – analyse the ideal power electronic converter
- In this course, Buck and H-bridge converters taken as examples to explain how to analyse converters and design them.

Video inset of Professor Doctor Shabari Nath speaking.

Now, there are many applications of power electronic converters and in a given application also there are many topologies which can be used. You have to select the one which fits your purpose. There are many choices. There is no specific answer to it which topology is the best topology.

You can compare them and depending on the cost and design factors and several other factors that come during the analysis, you can choose the suitable power electronic topology for a particular application. For example, there is a battery charging application. So, for battery charging mostly I will be using DC to DC converters.

Now, if it is a buck type application, where a battery voltage is less than the available DC voltage at the input side, then you also have many choices. You can use isolated converters, non isolated converters. Even if you choose non isolated among them, there are also different topologies.

So, depending on your application, what are the requirements of it? You have to understand that and then based on it you choose a suitable power electronic topology. Now, once you have chosen one particular topology, you have to analyse it, and you have to understand its operation because then only you will be able to design it.

So, the first step of converter design is to choose the topology for the particular application and then understand its operation. That is basically to analyse the converter. Now, there are many converters and there are many applications. In this design course, it is not possible for us to discuss all of them.

So, I will take buck converter and H-bridge converter as an example to explain you how to analyse the converters from perspective of design and then we will be also taking these two converters again and again for explaining the design concepts. So, first, let us begin with the analysis of buck converter.

(Refer Slide Time: 03:13)

**Two Rules**

Steady state analysis

Rules

- 1) Avg. voltage across inductor is zero.
- 2) Avg. current through a capacitor is zero.

$T_{ON}, T_{OFF}$

$$V_L = L \frac{di_L}{dt}$$

$$i_L = \frac{1}{L} \left[ \int_0^{T_{ON}} V_L dt + \int_{T_{ON}}^{T_{ON}+T_{OFF}} V_L dt \right]$$

So, this is the circuit of buck converter which is shown here.  $V_{in}$  is the input voltage and then normally a MOSFET is used for DC-to-DC converters for buck converter in low powers applications. Then, this is the diode given in the circuit and over here you have got the inductor and then there is the capacitor and this is the load resistor given in the circuit.

Different names are given to different voltages and currents, and this switch voltage is represented by  $v_{sw}$  and the current through it is  $i_{sw}$  and the diode voltage is marked like this ( $v_D$ ). So, you have to look at the polarity, and the way, where this positive voltage is marked. That is important. You can mark it in the other way as well.

It is just the voltages that will become opposite then. Then,  $v_L$  is the inductor voltage,  $i_L$  is the inductor current and so forth. Now to analyse these DC-to-DC converters, there are two rules that are generally followed. So, those rules are, (i) average voltage across the inductor is 0, and (ii) average current through the capacitor is also 0. Now, why are these two rules followed?

Now, let us say the switch on time, and we will call it as  $T_{on}$ , and the switch off time, we will call it as  $T_{off}$ . Now, we draw this inductor current waveform. So, this is the inductor current named by  $i_L$ . For  $T_{on}$  period usually this current will increase, and then during the  $T_{off}$  period it will decrease.

Now, it may not come back to its original position. Suppose it does not come back. So, after some cycles, this current will keep on building up. It may so happen that finally, the average current is going to keep on building up and it may increase the saturation level of the inductor and then that will damage the inductor.

So, that is not of course. We will not want that. So, then we see the inductor voltage,

$$v_L = L \frac{di_L}{dt}$$

and from this if we write the inductor current equation then this will be

$$i_L = \frac{1}{L} \left[ \int_0^{T_{on}} v_L dt + \int_{T_{on}}^{T_{on}+T_{off}} v_L dt \right]$$

So, then for this current not to build up it is required that this should come back to its original position after  $T_{off}$ . So, then we see here that, if we take the average over this time period  $T_{on} + T_{off}$ , then it should be equal to 0, otherwise the current will continue building up.

So, that's why this rule is there that average voltage across the inductor is 0. Similarly, we can also explain it that average current through the capacitor is 0. Now, also note down that we are going to do the steady state analysis. There is transient analysis also. That is done for converters. But, for design purpose initially the steady state analysis is required. So, we will be doing the steady state analysis.

(Refer Slide Time: 08:40)

### Assumptions

1) Ideal ckt

2) C large enough  $\rightarrow V_o$  constant  
 $I_o$  constant

3)  $V_{in} > V_o$

4)  $I_h = \frac{V_o}{R}$

$f_s \rightarrow$  Switching frequency,      Switching time period  $T_s = \frac{1}{f_s}$

Duty ratio,  $D = \frac{T_{on}}{T_s}$        $0 < D < 1$

Next, there are certain assumptions that are taken before analysing these DC to DC converters. What are those assumptions? First, we assume that the circuit is ideal. So, it is an ideal circuit. So, in this circuit we have kept all the components here. For this inductor we are ignoring any parasitic resistances, a capacitor also, effective series resistances. We have assumed this switch to be ideal. That means it instantaneously turns on and turns off and there is zero voltage across it while it is conducting and similarly it is for the diode as well. So, all components in the circuit are ideal.

Then, next this capacitor ( $C$ ) that we have shown here, is large enough. So, this capacitor is so large that the voltage across it ( $v_C$ ) or this output voltage ( $V_o$ ) is to be constant. There will be some ripples. But, initially for the simplicity of the analysis, we will consider that  $C$  is large enough and  $V_o$  is constant.

So, it implies that  $V_o$  is constant. So, we can also say that load current ( $I_o$ ) is also constant. Then we will make another assumption that the circuit has reached steady state. So, the circuit has reached steady state and it means that,  $V_{in}$  is greater than  $V_o$ . This actually happens in the buck converter. So, that's why we are assuming here that  $V_{in}$  is greater than  $V_o$ . If it is a boost converter, then we would have assumed  $V_o$  is greater than  $V_{in}$  and so forth.

Then,  $I_o$  is  $V_o$  by  $R$  and it is a constant. You may already know few more terms. But, just for the sake of completion, let me tell you that again.  $f_s$  is the switching frequency, which means, it is the frequency at which this device is turned on or off. That is the ( $f_s$ ) switching frequency and associated with that is the switching time period  $T_s$  where,

$$T_s = \frac{1}{f_s}$$

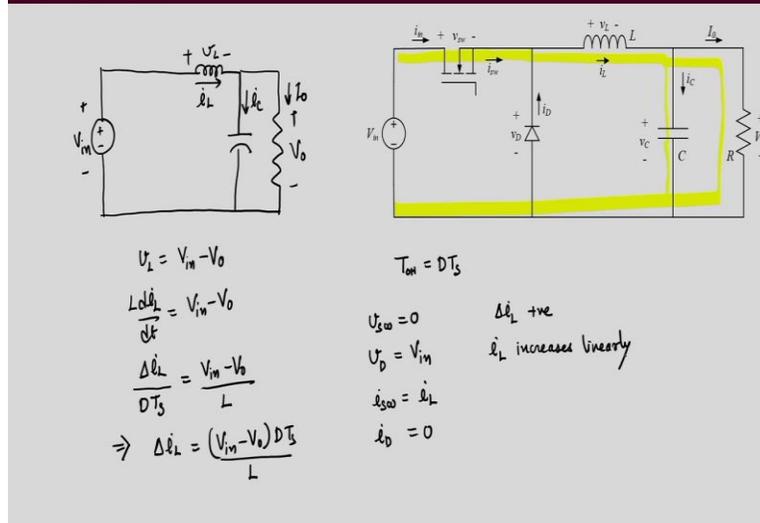
Then, we define another term named by duty ratio and this duty ratio is defined as  $D$ .

$$D = \frac{T_{on}}{T_s}$$

$T_{on}$  is the time for which the switch is on. So,  $T_{on}$  divided by the total switching time period is the duty ratio. Obviously, you can see that  $D$  will always be between 0 to 1.

(Refer Slide Time: 12:31)

## Switch ON



Let us look into the equivalent circuits that analyse the situation when the switch is turned on and when the switch is turned off. So, since we are assuming things to be ideal, when the switch gets turned on, we can assume it to be a short. We will consider MOSFET as a short.

Then we observe that since this is a short, the voltage appears over here is the source voltage ( $V_{in}$ ) and that will make the diode reverse biased. So, the current will simply then flow through the inductor and through these capacitors and resistors. So, if we have to draw the equivalent circuit, then this equivalent circuit will look like this.

If we write some simple expressions, then this inductor voltage is

$$v_L = V_{in} - V_O$$

That can be written as

$$L \frac{di_L}{dt} = V_{in} - V_O$$

So, since this voltage is a DC voltage, we can assume that this  $di_L$ , this change in current is to be linear.

This thing can be written as  $\Delta i_L$  and this time period is  $DT_S$ , because this is the on time period of the switch. We have already defined the duty ratio. So,  $T_{on}$  will be equal to  $DT_S$ . So, this will be

$$\frac{\Delta i_L}{DT_S} = \frac{(V_{in} - V_O)}{L}$$

It implies that

$$\Delta i_L = \frac{(V_{in} - V_O) DT_S}{L}$$

So, this is the expression for the ripple in the inductor current.

Now, we will be using this expression later on for a design purpose. Now, let us see the voltage across the device. So, we see here that, the voltage is 0 when the switch is on and the voltage across the diode when the switch is on, is equal to  $V_{in}$ . Current through the diode at that time is 0 and the current through the switch is the same as the inductor current.

So, then we can write it that

$$v_{sw} = 0, \quad v_D = V_{in}, \quad i_{sw} = i_L \quad \text{and} \quad i_D = 0, \quad \text{while the switch is on.}$$

Also, one more thing that you have to observe is that  $V_{in}$  is greater than  $V_o$ . We had assumed that before. So, that means this change in current is going to be positive. So, while the switch is on,  $\Delta i_L$  is positive and that means that  $i_L$  increases linearly.

(Refer Slide Time: 16:41)

Switch OFF

$$v_L = -V_o$$

$$L \frac{di_L}{dt} = -V_o$$

$$\Delta i_L = \frac{-V_o(1-D)T_s}{L}$$

$i_L$  decreases linearly

$$T_{off} = (1-D)T_s$$

$$v_{sw} = V_{in}$$

$$v_D = 0$$

$$i_{sw} = 0$$

$$i_D = i_L$$

Now, let us look into that when the switch is off. So, when the switch is off, this is open. So, we will consider this as open. Then there was already some current established in the inductor. Now, current through an inductor cannot change instantaneously. So, it will try to find out a path and this diode will then provide that path in the current. The current will then flow freely through this diode. So, accordingly we can draw the equivalent circuit.

So, now, again we can write the voltage across the inductor. If you apply KVL, it will be equal to  $-V_o$ . So,

$$L \frac{di_L}{dt} = -V_o$$

So, therefore, we can write

$$\Delta i_L = \frac{(-V_o)DT_s}{L}$$

The reason behind  $(1-D)T_s$ ,

$$T_{off} = (1-D)T_s,$$

That's why we are writing it.

Also, the voltage across the device, the switch voltage ( $v_{sw}$ ) is open. The voltage across the switch then is equal to  $V_{in}$ , the input voltage. So,

$$v_{sw} = V_{in}, v_D = 0.$$

Since it is conducting as an ideal, so it is 0.

$$i_{sw} = 0, i_D = i_L.$$

Now, the diode carries the inductor current. Also, we observe here that this is negative. So, change in current ( $\Delta i_L$ ) is negative. So, the current is going to decrease linearly. So, now,  $i_L$  decreases linearly. So, we did all these things.

(Refer Slide Time: 19:52)

**Duty Ratio**

Avg. voltage across inductor = 0

$$\frac{v_L |_{T_{on}} + v_L |_{T_{off}}}{T_s} = 0$$

$$\frac{(V_{in} - V_o)DT_s + (-V_o)(1-D)T_s}{T_s} = 0$$

$$\Rightarrow \boxed{V_o = DV_{in}}$$

Now, let us find out the expression for duty ratio. How do we calculate duty ratio based on certain input and output voltage? So, for that, we follow this rule that average voltage across the inductor is equal to 0. So, therefore,  $v_L$  for the on period multiplied by  $T_{on}$  plus  $v_L$  for the off period multiplied by the  $T_{off}$ , and divided by time period  $T_s$ , is equal to 0.

So, then if we substitute that means

$$\frac{(V_{in} - V_o)DT_s + (-V_o)(1-D)T_s}{T_s} = 0$$

So, if you solve it, you will be getting

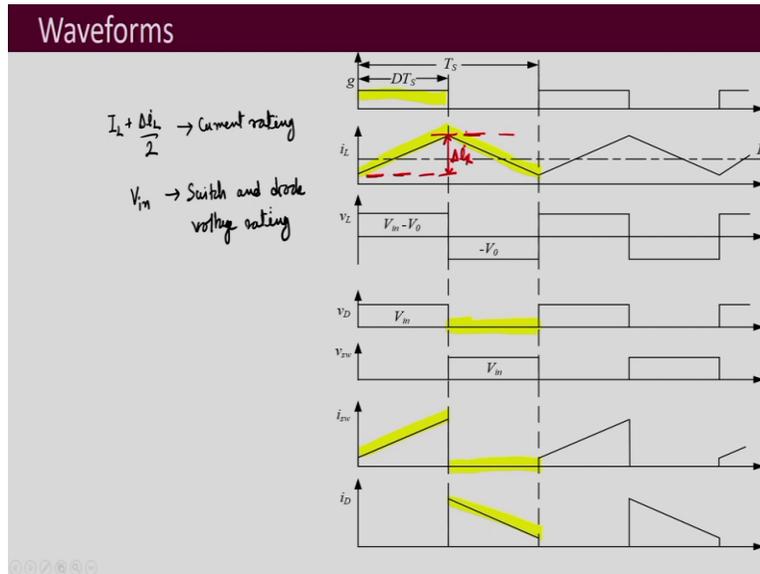
$$V_o = DV_{in}$$

So, this is the expression for the duty ratio that you obtain from here.

$$D = \frac{V_o}{V_{in}}$$

So, if you have given input voltage and you want a particular output voltage then you can calculate the duty ratio using this expression.

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Now, let us look into the waveforms. So, this is this gate pulse. So, this is the time period for which the switch is on and this is the time period for which the switch is off. Now, during the on time period we know that the current is increasing. Then the current comes back to its original position because that is the rule that we are following.

During that time this voltage across the inductor is  $V_{in} - V_o$ . We just saw all that. When the switch is off, the voltage across the inductor is  $V_o$ . By analysing the equivalent circuit you get it. Voltage across the diode when the switch is on, is  $V_{in}$ . We just saw that now. When the switch is off, at that time the diode conducts and so this is equal to 0.

Similarly, for the switch voltage also we see that the waveforms are drawn. The switch current is same as the inductor current here. When the switch is not conducting, it is equal to 0 and similarly for the diode when the diode is not conducting, the current is 0 and when the diode is conducting, this is same as the inductor current  $i_L$ .

So, these are the waveforms that we have plotted using the equivalent circuits. Now, what is the use of these waveforms? Why do we keep drawing waveforms in power electronics? Now, looking at these waveforms, you can observe that the voltage, which the diode has to block is the input voltage and the voltage, which the switch has to block is also equal to the input voltage in case of a buck converter.

So, when you have to choose the rating of the diode and the switch, the voltage rating has to be minimum equal to the input voltage. Also, they have to carry minimum current and it is equal to the maximum peak of the inductor current. So, that gives us the ratings of the devices. So, then we can see that here is this ripple in the inductor current. So, this is the ripple current defined by  $\Delta i_L$ .

Then, this is the average that is denoted as  $I_L$ . So, what will be the peak value from this waveform itself? The peak value is going to be equal to  $i_L + \frac{\Delta i_L}{2}$ . So, the current rating of the devices has to be equal to this. This gives you the current rating.

Also, the inductor also has to withstand this ripple and also the current rating of the inductor has to be equal to this minimum and it is equal to this peak current rating which is  $I_L + \frac{\Delta i_L}{2}$  and the voltage rating of the devices is equal to  $V_{in}$ . So, that is the switch and diode voltage ratings.

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**Key Points**

- ✓ Choose suitable topology based on application
- ✓ Analyse the ideal power electronic converter
  - ✓ Different possible equivalent circuits
  - ✓ Draw waveforms
- ✓ Find expression for duty ratios

So, what are the key points of this lecture that you should remember? First is that you choose a suitable topology depending on the application for which you are designing the power electronic converter. Next is that you analyse the ideal power electronic converter. The topology that you have selected, at the initial stage you do not have to introduce non-idealities. You analyse the ideal circuit.

You find out what are the different possible equivalent circuits in it. You can draw the waveforms analysing the equivalent circuits and from there you get the first idea of the device ratings and the component ratings that you require for the voltage and current levels. You should also be able to find out the expressions for duty ratios. Thank you.

