

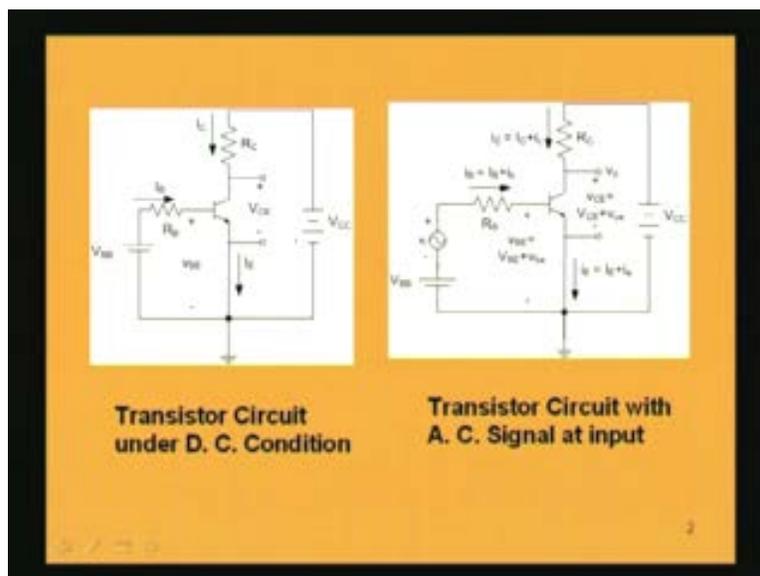
Basic Electronics
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Module: 2 Bipolar Junction Transistors
Lecture-3
Biasing the BJT - Part 1

In the last classes we have studied about the characteristic curve of different configurations of transistors and we have seen that the active region, the saturation region and the cutoff region are the three operating regions of the transistor. But under normal operation as an amplifier the transistor is to be biased in the active region. The saturation and the cut off regions are only used for exclusive applications like switching and cutoff. The transistor when it is used as an amplifier the first and foremost thing to remember is that it has to be biased in the active region. If it is properly biased in the active region, when we give a small AC signal at the input of the transistor then it will be able to amplify it to a large signal and this amplification again has to be proper because the shape of the input voltage signal has to be maintained correctly without any distortion. The faithful amplification of a weak signal is done by a transistor amplifier if that transistor is biased properly in the active region. Today we will discuss about biasing the transistor.

Biasing means the proper selection of the operating point or maintenance of proper level of DC voltage and currents in the transistor. Under DC circuit if we consider a transistor then we have a figure like this. Here we are using an NPN transistor which is common emitter and throughout our discussion we will be using a common emitter transistor because of the fact that it has high current amplification factor, beta which will be used for amplification of an input signal.

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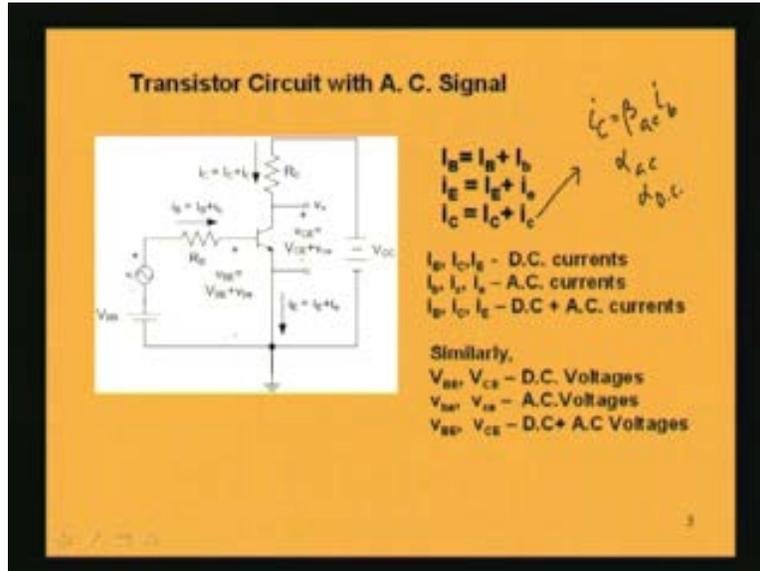


This beta value is high, so common emitter transistor is normally used for amplification purpose. Using a common emitter transistor in NPN configuration we have this input circuit between base and emitter. Emitter is grounded by V_{BB} . Biasing is done; forward biasing in the input circuit and the collector base junction is reverse biased by the application of the source V_{CC} . In this circuit resistance R_B and R_C are connected in the base as well as the collector circuit and this is practically what is done in a transistor biasing and we now consider application of an AC signal at the input.

Suppose we have an AC signal v_1 . Along with the biasing voltage V_{BB} this is being applied at the input and our purpose is to amplify this weak signal faithfully. That means we want the magnitude, peak to peak of the input voltage to be magnified without any distortion in the shape of the input signal. If it is a sinusoidal, we want perfectly sinusoidal output at the collector and it should not be distorted in any portion throughout the cycle. But we want the magnitude to be amplified; peak to peak voltage should be magnified. That is the basic of amplification. Here when we have an AC signal along with the DC voltage, V_{BB} the currents which are earlier flowing in the DC circuit were the DC currents I_B , I_C and I_E . Because of the application of the AC signal we will have AC currents also. Considering the base, we will have an AC current, small i, small b (i_b) denoting the AC quantity along with the DC value I_B . Similarly the collector current will be capital I_C plus small i_c . The instantaneous current in the collector will be capital I_C plus small i_c ; capital I_C being the DC component of the instantaneous current and small i_c being the AC component.

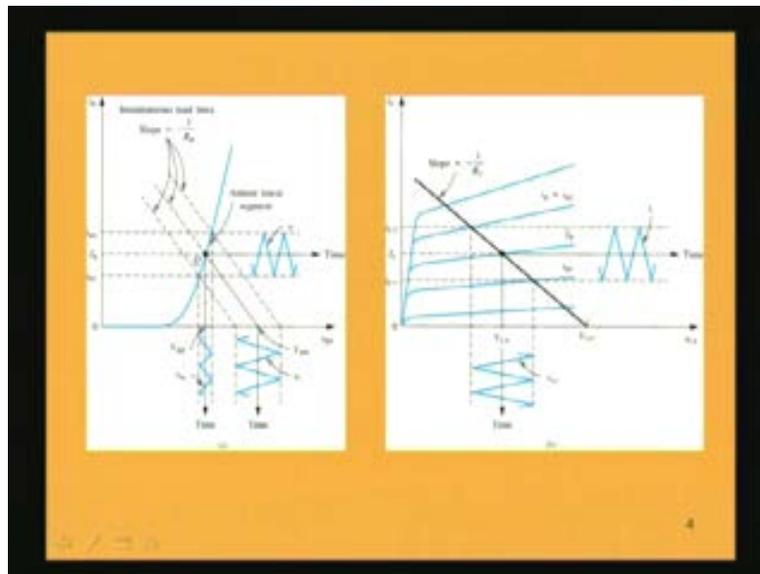
Similarly in the emitter we have capital I_E plus small i_e and if we consider the voltages then the base to emitter voltage will be capital V_{BE} plus small v_{be} and the collector to emitter voltage is capital V_{CE} plus small v_{ce} . Here we have the symbolic representation of the instantaneous current and voltage by small i capital C (i_c) or small i capital B or small i capital E denoting that this is the instantaneous current. Similarly small v_{CE} when we write, CE being capital and v being small we mean that it is instantaneous voltage which is a combination of the DC as well as AC. This is the symbolic representation for the instantaneous current, I_b , I_e and I_c where the capital part or capital notation is used for the DC and small notation is for AC. What we see here when we apply a small signal apart from the DC biasing voltages there will be current flowing in the circuit which will be having two components. One is the DC component and on it will be super imposed the AC component and here if we consider say small I, small c this is nothing but beta AC small i small b where this beta AC is the AC beta value and this is magnitude-wise not very different from the DC beta value. AC beta value and DC beta value are magnitude wise almost same; only a little difference is there and similarly the small alpha for AC that is alpha AC and alpha DC these are also magnitude wise not very different. For all practical purposes we can assume that beta and alpha have same DC as well AC values.

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Again if you look into the AC and DC components and the overall instantaneous current and voltages then we see here in these plots, you have only DC conditions prevailing. Suppose we are not giving the signal as such till now, only the biasing voltages are there.

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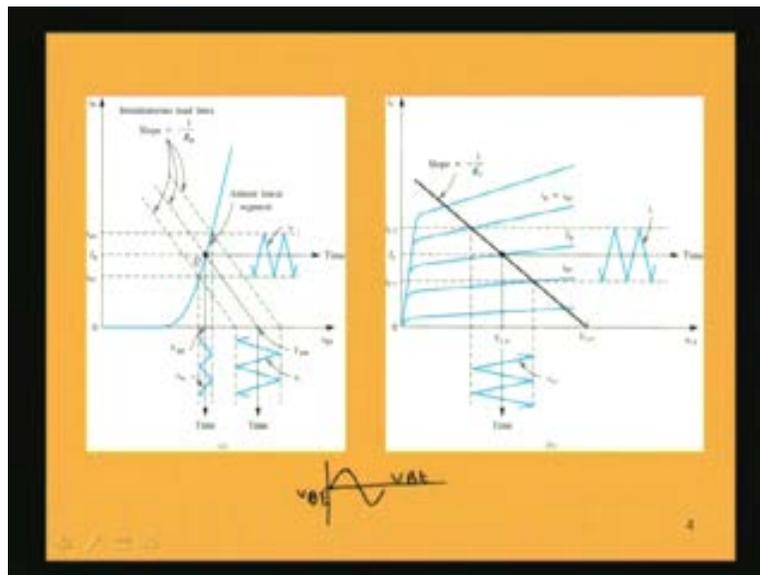


Then due to the DC biasing that is the input circuit is forward biased and output circuit is reverse biased, for that condition we are having the DC condition prevailing and the current and voltages for the DC condition is this is the point of operation. It is called Q point and the DC base to emitter voltage if you consider it is V_{BE} . This point is having base to emitter voltage V_{BE} , capital V and capital BE. That is the DC voltage and the

current flowing in the base which is capital I capital B, the DC current is I_B . For that particular voltage, this is the current I_B . The Q part in the input characteristic defines the DC voltage between base and emitter and the base current I_B . We are applying a small signal at the input. If we look back into the circuit, due to this small signal another current flows which is purely AC. That current is denoted by small s, small b for the base and corresponding current in the collector which is purely AC that will be small i, small c, which is equal to beta times, beta means the AC beta into small i, small b. This base region if we see and we concentrate on the input characteristic that is the characteristic between the base current and base to emitter voltage we have a change in the V_{BE} due to the application of the signal. If we consider the DC V_{BE} then when the signal is in the positive half cycle, that small signal is in the positive half cycle we have increment of this base to emitter voltage.

Initially this is the DC V_{BE} . It will be increasing. Due to the application of the small v_{be} , it will rise in the positive half cycle and it will reduce in the negative half cycle. If we consider the instantaneous value of the voltage between base and emitter starting from the DC value it will rise above the DC value when the signal is in the positive half cycle and it will fall below the DC value when the signal is in the negative half.

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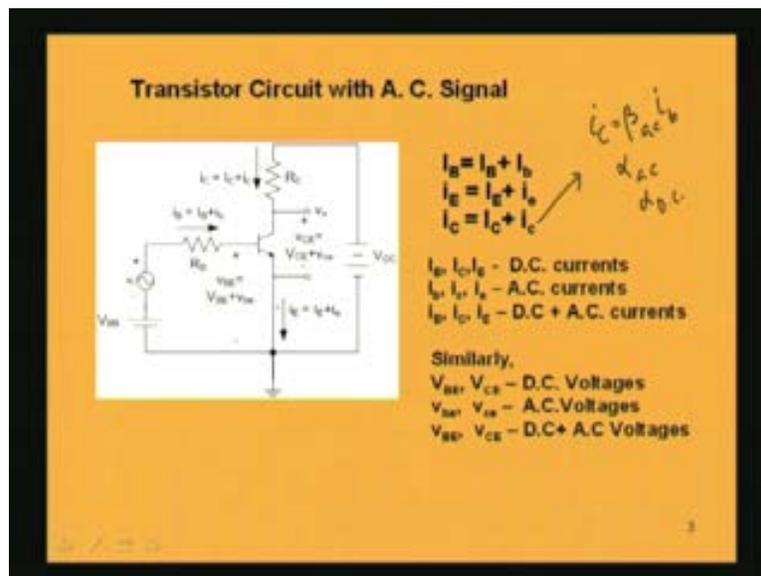


We have instantaneous voltage between base and emitter represented by this waveform. Starting from here we can see in the positive half cycle of the signal it will be rising and in the negative half cycle it will be falling. Instantaneous value of base to emitter voltage will be like this. Correspondingly base current if you see the DC base current is this one. When the signal is increasing the base current will be increasing because of the more biasing in the forward region. The voltage is increasing and then when it falls, the input signal falls in the negative half cycle then the base current will be also decreasing than the DC value.

We have this representation of the base current and for example we are considering a triangular signal. You can have sinusoidal signal or triangular signal but it is periodic and we are considering a triangular signal in the input. This is the triangular shape we are showing. This is happening because the input circuit is having this V_{BB} plus this signal V_I . V_{BB} is the DC voltage which is forward biasing. V_{BE} is this value and it will be increasing. This V_{BE} will be increasing because of this small signal from this V_{BB} value and it will be falling also in the negative. This is the V_{BE} value, DC and AC and this is the value of the increment of this biasing voltage and the decrement of the biasing voltage in this circuit.

What you have to notice is that this is the biasing voltage. But base to emitter voltage and this voltage are not same because after the drop occurs here we get the base to emitter voltage; that is this voltage minus this drop. The drop occurring across R_B is because of this instantaneous current I_B , so this voltage minus this drop is equal to V_{BE} . In this graph here both are shown. This is the biasing voltage but this is the voltage between base and emitter and this is the corresponding base current. In the input circuit the DC load line can be drawn by connecting the maximum and minimum values on the x- and y- axis and so maximum value for a particular R_B because if we change this value of R_B , our load line will differ. For a particular R_B we want to draw the load line. If we consider maximum point of this base to emitter voltage and this point which will be maximum on the I_B then it will be happening when you make this V_{BE} zero. If we consider DC load line then without application of the input signal the load line will be like this. That means here V_{BB} will be the maximum value of the voltage available across the base to emitter junction.

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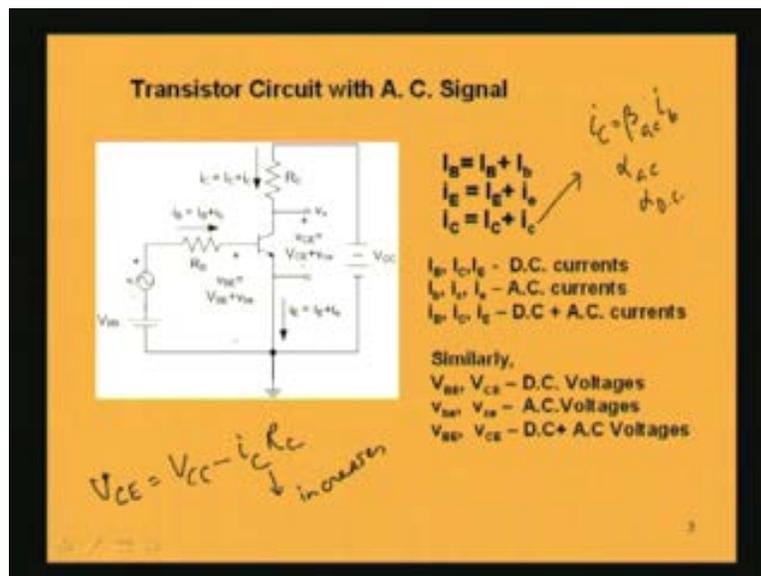
That will happen when I_B current is zero and the maximum value of the I_B current will occur when base to emitter voltage is zero. That is another point, maximum point. If we join this we can get the load line and for a particular value of R_B that you are choosing

the intersecting point between the characteristic and the load line will give you the operating point; that we all know and the slope of that load line is minus 1 by R_B . Minus sign is because it is decreasing. This slope is such that the straight line is having a negative slope. That is why it is negative and 1 by R_B is the slope.

If we look into output characteristics we see here that the output characteristic is nothing but the plot between I_C and V_{CE} and here it is instantaneous current and instantaneous voltage, combination of both DC and AC. Corresponding to a particular I_B we have that particular value of I_C . As I_B is increasing from its DC value correspondingly I_C will also increase. Initially when there is no signal then the DC value of that I_C is the capital I, capital C that is this point. Base voltage is increasing. V_{BE} is increasing, base current is increasing. Correspondingly there will be collector current increment because now the AC current small i, small c will be added up with capital I_C and small i small c, i_c is nothing but beta times small i, small c, i_c . So this collector current also increases. Similarly when the base current decreases collector current will decrease. We have this increasing and decreasing collector current across collector to emitter voltage.

Consider collector to emitter voltage. When there is no signal means only DC conditions are prevailing. This is the operating point that is the intersecting point between the load line and the characteristic. This DC value is V_{CE} DC value in the collector to emitter voltage. The value of V_{CE} when collector current increases, is given by $V_{CC} - i_c R_C$. $V_{CC} - i_c R_C$ is equal to V_{CE} . Instantaneous value if we consider then this instantaneous value of the voltage between collector and emitter that is equal to this V_{CC} minus $i_c R_C$. If i_c increases then this whole quantity will be decreasing because it is negative.

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$i_c R_C$ drop will increase means V_{CE} will decrease. An important fact to be noticed here is that when collector current increases, collector to emitter voltage will be decreasing. It is because of this negative factor here so it will decrease when i_c increases. Here starting

from this DC value when i_C is at this peak we will get the negative peak of the V_{CE} . So this point is important. When i_C is minimum, then we will get this V_{CE} maximum. For a particular value of resistance in the collector we can draw the load line. This DC load line if we want to draw joining the maximum points in the voltage as well as the current axis, maximum point of the voltage is V_{CC} . When you have zero current in the collector maximum voltage will be available and that cannot exceed V_{CC} . $I_C R_C$ drop is zero. So V_{CC} is the maximum upon and the collector current will be maximum when you have V_C is equal to zero and that value is V_{CC} by R_C . Joining these two points for a particular RC we get a load line.

Intersecting point between this load line and the characteristic for a particular base current at which the transistor is being operated is given by this point which is known as Q point. That is the operating point and this operating point is the point which is the DC point. That means we are not applying any signal. What will be the collector to emitter voltage? That is given by the Q point or it is called quiescent point. Quiescent means silent point, meaning it is not having any signal in the input. That means it is not having any AC voltage in the input, only DC biasing voltages are there. This Q point will give you the operating condition of the transistor and for a particular resistance in the base we have a particular value of I_B and for that particular value of I_B this is the Q point. If you go on changing I_B , for different values of I_B we will be getting different Q point and the slope of this load line is minus 1 by R_C ; minus because it is a negative slope as it is clear from the straight line. The slope is negative and 1 by R_C will be giving that slope. From this slope we can basically know about the resistance which is connected in the collector.

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$$V_{CE} = V_{CC} - I_C R_C$$

$$= V_{CC} - (I_C + i_c) R_C$$

$$= (V_{CC} - I_C R_C) - i_c R_C$$

$$= V_{CE} - i_c R_C$$

V_{CE} = D.C. Bias voltage at the collector

Considering only the A. C. Voltage at the collector,
 $v_o = v_{ce} = -i_c R_C$
 Voltage gain = v_o/v_i

Considering that DC as well AC conditions prevail together, we have apart from this DC biasing voltage the AC signal which you want to amplify. Basically why amplification is happening in the transistor that we will discuss in detail later but for the time being we have to see one point. When we talk about amplification we mean amplification of the AC

signal. While dealing with amplification of a signal we will be concentrating only on the AC conditions and DC conditions are only for biasing the transistor properly and for amplification or operating the transistor as an amplifier we will have to deal with the AC conditions prevailing exclusively.

But again if we consider this collector to emitter voltage this part is collector, this part is emitter and this part is base. Collector to emitter voltage is equal to V_{CC} minus $i_C R_C$. In this output circuit if we apply the Kirchoff's voltage law we get this. V_{CC} minus $i_C R_C$ is equal to V_{CE} and $i_C R_C$ we can write this. This if we again write that V_{CC} minus $i_C R_C$ equal to V_{CE} . Basically what we are writing by this equation is that the instantaneous voltage between collector and emitter is given by this V_{CC} ; that is the DC biasing voltage at the collector which is reverse biasing minus $i_C R_C$. This $i_C R_C$ if we consider this i_C is basically that instantaneous current having I_C plus small i_c . But we will only consider AC voltage in order to discuss about amplification of the transistor and then we will concentrate only on the AC component. AC component in this $V_{CC} - i_C R_C$ is only that small i_c , small c and R_C that product which will be now used for finding out the amplification and voltage gain happens because the product of this current and this resistance at the collector if we consider alone, i_C is nothing but beta times of I_B .

If we consider the voltage gain that is the ratio between the output voltage and the input voltage you are getting an output voltage V_O at collector point. That voltage if we name it V_O as the output voltage, V_O is basically minus small i_c into R_C and this minus is happening because we have seen just now that increment of i_C will cause decrement of that V_{CE} . This minus $i_C R_C$ if we consider with respect to this input voltage then later we will come to know that, that will have a very large amplification factor. V_O by V_I will be very large; hundreds of gain we can have because of the fact that in common emitter transistor when it is used as an amplifier that i_C is nothing beta times of I_B and input voltage will be this base current into the input resistance of the transistor and input resistance of the transistor is very small. Finally what we will be getting is V_O by V_I in terms of beta and that beta is very high and this beta will be affecting the overall gain. Why a transistor in common emitter configuration is used is because i_C is equal to beta times of i_b . This beta value is high and again it will be multiplied by R_C . The whole thing, this product will be high with respect to or in comparison with input voltage.

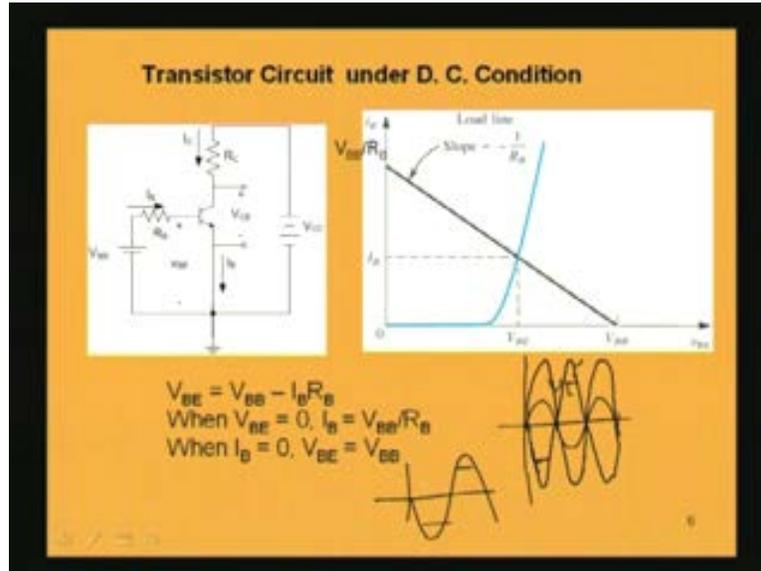
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$V_{ce} = V_{cc} - I_c R_c$
 $V_{ce} = V_{cc} - (I_c + I_b) R_c$
 $V_{ce} = (V_{cc} - I_b R_c) - I_c R_c$
 $V_{ce} = V_{cc} - I_c R_c$
 $V_{ce} = \text{D.C. Bias voltage at the collector}$
 $V_{cc} - I_c R_c$
 Considering only the A. C. Voltage at the collector,
 $v_o = v_{ce} = -i_c R_c$
 Voltage gain $= v_o/v_i$
 $A_c = \beta \times R_c$

Basically we get an amplification occurring in the transistor amplifier and how this amplification occurs we will discuss in detail. But at this point what is to be noted is that the signal should not be distorted while being amplified. Meaning is that suppose we are trying to amplify a small signal. For example it is a sinusoidal signal which we are amplifying. Then the output which we will get at this collector of point that is V_O with respect to ground if we find out V_O and see in the oscilloscope basically I must get a voltage which will be similar in shape, exactly in the same shape as the input voltage. But it is to be magnified. That means I expect a waveform V_O which will be like this in nature. That is the magnitude is amplified many times but the shape is exactly same. If it is sinusoidal input I must get a sinusoidal output at the collector end.

If it is a triangular I must exactly get a triangular. This will not be exactly in this same phase. We will find later that it will have an opposite phase. That means output voltage in common emitter transistor will be basically out of phase with the input. Basically with this will be the signal. How this signal is coming out of phase? One hint we have got just now that it is negative with respect to the collector current and collector current is again in phase with the base current. Basically what will happen is that the output voltage will be out of phase with input voltage. But nowhere during this amplification should the shapes change. That is we should not get an output voltage where a portion may be clipped in the positive or in the negative region. That means I should not get an amplified signal which is like this or like this and to ensure that, one point is important that we must properly bias the transistor. The transistor must be biased properly. That means we have to now again look into the DC conditions that is prevailing.

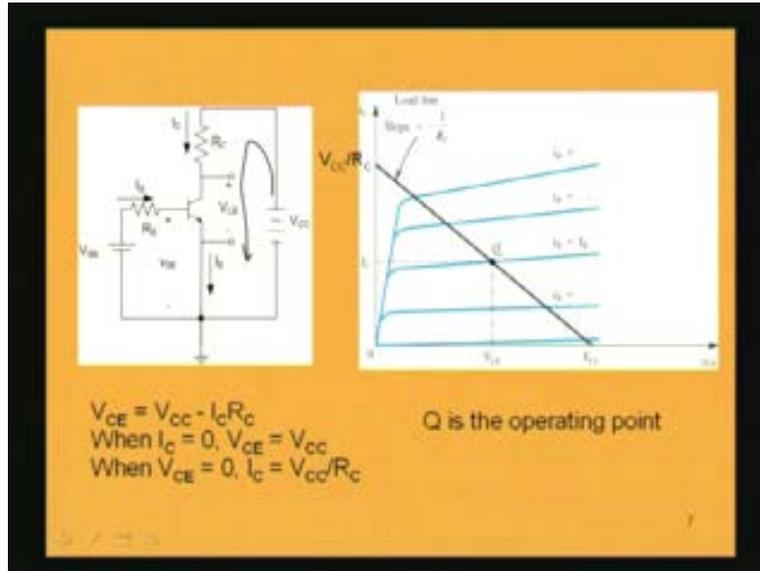
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I again consider the DC circuit which biases the transistor in the active region. The input circuit If I consider, draw the load line then this is the input circuit DC biasing point. The basing point means this point will give you the value of the DC voltage and the DC current in the input circuit which is the base emitter circuit. In this circuit what is the value between base to emitter and what is this base current? That is known by this point which intersects the input characteristic and the input circuit load line and that is evident from this input circuit equation. If you write down the Kirchoff's voltage law equation in the input circuit V_{BB} minus $I_B R_B$ is equal to V_{BE} . I can draw this load line very easily. If I make V_{BE} is equal to zero then I_B is equal to V_{BB} by R_B that is this maximum point and when I_B is equal to zero this V_{BE} is maximum which is nothing but it becomes equal to V_{BB} , the base biasing voltage. Joining these two points I get this load line. The point where it intersects this input characteristic that gives the input circuit operating point.

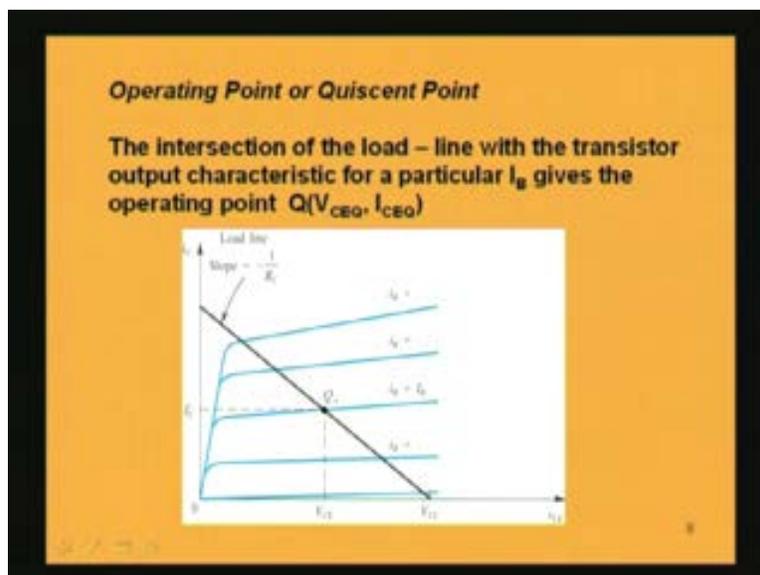
Similarly in the output circuit if I want to draw the load line and find out the operating point I must join these two maximum points. That is very easily obtained from the output circuit if I apply Kirchoff's voltage law in this loop. V_{CC} minus to plus rising minus $I_C R_C$ minus V_{CE} is equal to zero; V_{CE} is equal to V_{CC} minus $I_C R_C$. Here when I put I_C is equal to zero I get V_{CE} is equal to V_{CC} . That is the maximum voltage that is available on the x-axis that is the voltage axis and when V_{CE} is equal to zero I get the maximum collector current that is possible which is equal to V_{CC} by R_C . That is this maximum collector point. Joining these two points I get this load line and for a particular I_B which was this I_B for that particular DC condition of the input circuit means for a particular I_B which is determined by nothing but only this resistance in the base circuit. This is now operating point because this output characteristic, for a particular I_B we are considering intersects this DC load line at this point which is Q.

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This Q is the operating point or quiescent point or silent point. Various names are there but this point is nothing but the point which determines DC condition in the output circuit. The operating point is one important point which we must first set. Setting the operating point properly is the basic criterion for proper amplification in a transistor amplifier. What is this importance of properly sitting the operating point or by what factor will we be ascertaining that the operating point is proper? If we look into this output characteristic and this load line, here the operating point is almost in the middle of the load line. That is the operating point is situated almost at the middle of load line.

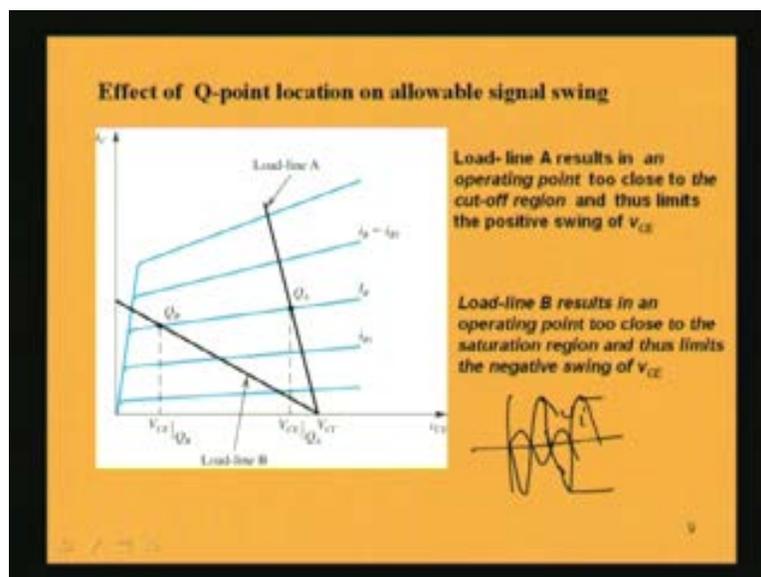
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This is an important fact because if the operating point is not around the middle of the load line or if the operating point is much closer to the cutoff region or to the saturation region then we will not get a distortion less amplification of the input signal which can be verified by examples.

What is the effect of this Q point location on the allowable signal swing? That means I want to get as much larger swing as possible in the output. Suppose I am giving an input signal, a very small weak signal, I expect that my output signal at the collector should be having a very huge swing means I must get peak to peak values. This swing must be as wide as possible.

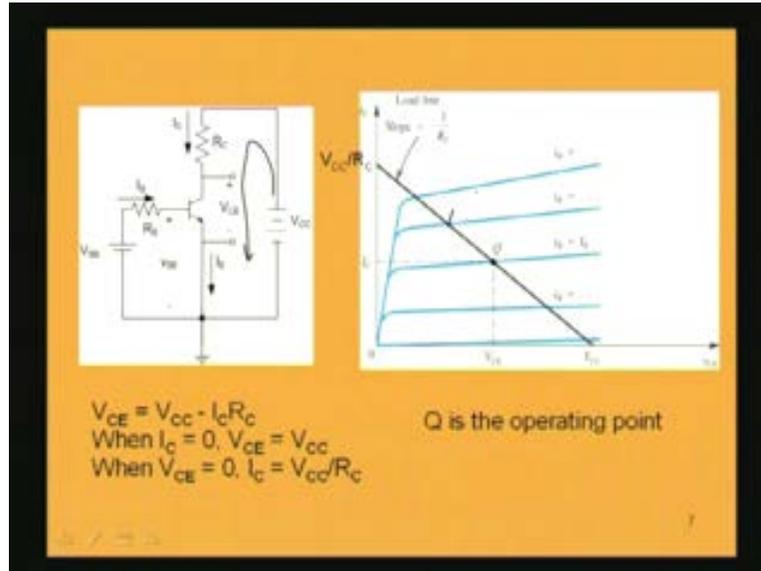
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That is also considering that the swing must be distortion less. I should not get a clipped output voltage.

If we look into the output circuit again then here the Q point is determined by this fact that for a particular I_B this intersecting point between the load line and the output characteristic in the DC circuit that is the Q point. If I have a different I_B my Q point will be here. Suppose I am considering for this I_B , I_B can be different only when I change this R_B value. R_B value is determining the I_B . If I have different R_B I may have I_B here, I may have DC value of I_B here. That means the Q point will be shifting above or below the ideal point.

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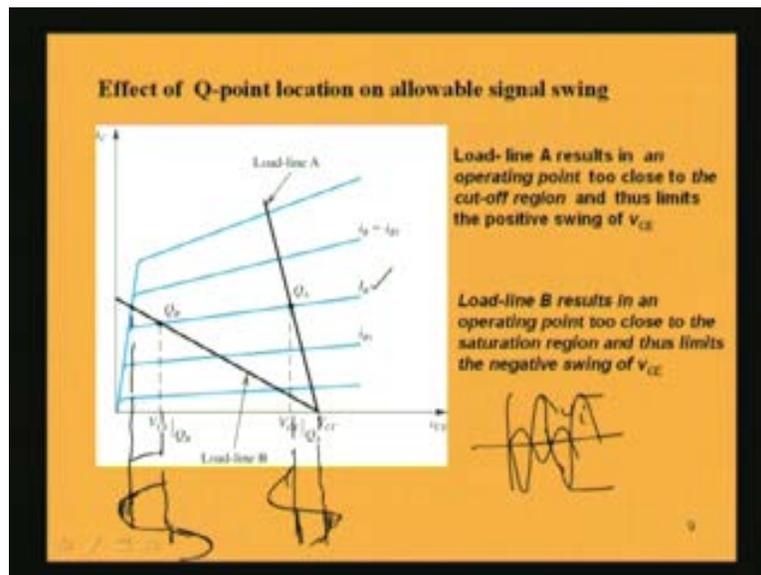
If I have such type of condition happening that my Q point is suppose shifting to this or this point; that means ideally I am not having in the middle of the load line. Load line is now different for different values of output resistance. Output circuit resistance if I change, R_C value also if I change then the load line slope will be different. If I have different R_C value in the output then the slope of the load line in the output circuit will be different as is evident here. This load line and this load line, load line A and load line B are different. The slopes are different because of the fact that the slope is determined by the resistance in the collector R_C . If I change R_C value I have a change in the slope of the load line. Changing the slope of the load line will be having an effect on the Q point. Q point for a particular I_B I am considering, suppose same I_B I am considering. I am not changing R_B value, input resistance value I am not changing, base resistance R_B is same. Then because of the slope being different, it is intersecting the I-V characteristic here and if the slope is different by this load line B, it is intersecting at another point Q_B .

I have different Q points, different from the earlier cases. Load line A is having this Q point Q_A and for that Q point Q_A , I am having the voltage at the collector to emitter by V_{CE} . The voltage at the collector if I consider the Q_A load line then as we see that this operating point is having this DC value. This DC value is very, very close to the cutoff region. Cutoff is when you have this I_B zero. Below the I_B zero portion will be the cutoff region. If it is suppose starting from this point then what will happen is that when you increase this base current, this base current is increasing and collector current will increase. Collector to emitter voltage will increase and when you decrease this base current, collector current will decrease and collector to emitter voltage will increase. If I see the V_{CE} profile, if I look into the positive swing I see that the instantaneous value of the collector to emitter voltage is clipped in this portion because at any point the value of the V_{CE} cannot be greater than V_{CC} . V_{CC} is the supply voltage we are providing. If we look back into the circuit this is the supply voltage which is reverse biasing and that is

V_{CC} . At any point you cannot have a value V_{CE} greater than V_{CC} . Our upper point, this point is fixed; we cannot go beyond this.

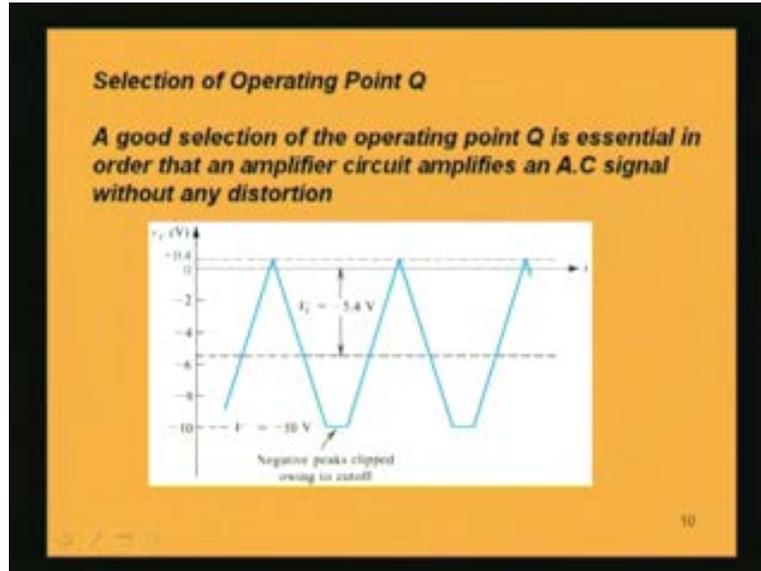
If the operating point is closer to the cutoff region, then we see that one portion of the positive swing is cutoff. We will get an output which will be clipping off one portion in the positive half cycle. Similarly if we consider this load line, this is the operating point. In the negative half cycle this operating point is closer to the saturation region. What will happen is that in the negative half cycle this is the maximum collector current that can flow in the circuit. Its upper point is fixed by the load line which is V_{CC} by R_C . You cannot go beyond this point. If we concentrate on negative swing, from this DC value it will be negatively increasing but it cannot increase beyond this point. This region will be cutoff. But upper portion does not have any problem. It will have the undistorted swing in the upper portion or positive portion but the negative portion has a clipped off representation and that is not desired.

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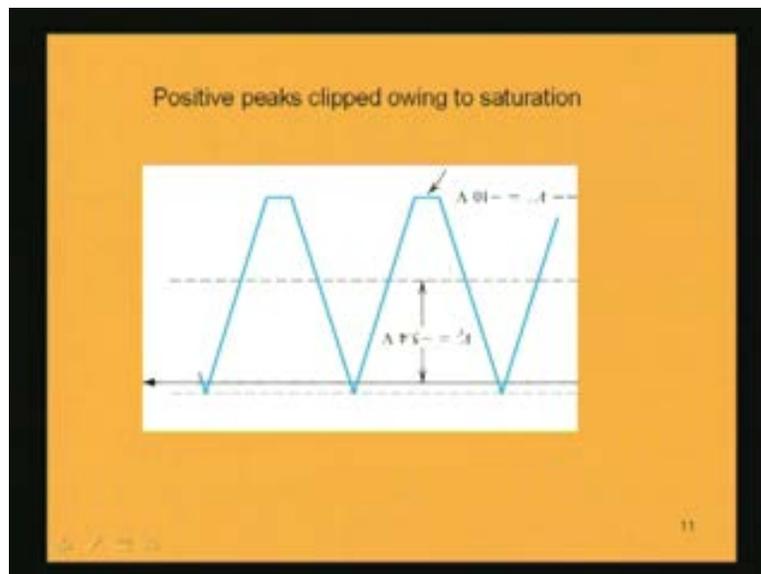
We cannot get an amplification having distortion. That is not desired. What we infer from this is that if the operating point selection is proper either it is too close to the cutoff region or too close to the saturation region. Then what we will be getting at the output, that signal will not be distortion less. That means it will be either clipped off in the positive or clipped of in the negative portion of the cycle and that is not desired at all. This Q point selection must be proper so that maximum on this total swing in the output signal is obtained. First and foremost thing that we have to emphasize is, proper biasing of the BJT. That is DC biasing of the BJT is to be discussed first and once we ascertain that it is properly biased then only we can proceed to have distortionless amplification of a weak signal. I just want to show you the output signal having negative clipped off as we discussed just now. When you have the operating point very close to the saturation region your negative signal will be not distortionless. It will be having a clipped off region.

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Ultimately output will be like this and if we have the operating point very near to the cutoff then we get a clipped off version in the positive swing. Output signal will be like this.

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There will be clipping off of the positive part of the signal and we do not want that. We will now concentrate on how to bias the BJT properly. Biasing means application of DC voltages to establish a fixed level of current and voltage. That means it is proper selection of the Q point to suitably accommodate maximum undistorted output signal swing that is the aim of our DC biasing. We have to select the Q point properly such that we have

maximum undistorted swing in the output signal. Maximum undistorted swing means in the output signal there should not be any clipping of any portion in the output signal. But again once we select a Q point properly it must also not be shifted. Suppose we have selected the Q point at the middle of the load line, just to have the maximum undistorted swing, like this. But even after selecting the Q point properly it may so happen and it happens that Q points shifts either towards above or towards below the properly selected initial selection. Then again we will be facing the same problem. Once we select Q we must also guarantee that it is not being shifted because of change of beta value or change of temperature.

When this Q point will shift? For any reason even after the selection of the Q point if the collector current I_C is changed, if it is becoming higher, then it will be shifting to the top and that happens because of two reasons. One is change of beta value. During operation of the amplification or operating the transistor as an amplifier suppose we are changing the transistor because of various reasons, it may so happen that you have to change the transistor, and if we change the transistor this beta value will not be same because it is very difficult to have the same beta value for two different transistors. Even though this fabrication is very much advanced now-a-days, still having two beta value exactly same is difficult. When you change the transistor it may have a different beta value. If the beta value changes then definitely I_C will change. I_C is equal to beta times of I_B . Even if you are keeping I_B same, we are not changing I_B but still I_C is changing because of change of beta value.

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Biasing the BJT

Biasing means application of D.C. voltages to establish a fixed level of current and voltage

i.e. to select Q point suitably to accommodate-

Maximum undistorted output signal swing

Also once selected properly, the Q point should not shift because of change of I_C due to

(i) β variation
(ii) Temperature variation

$I_C = \beta I_B$

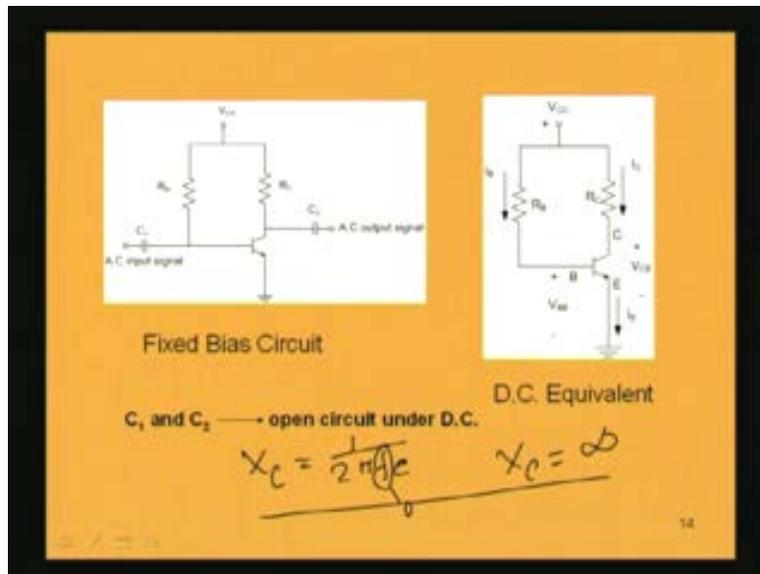
Another factor which affects the change of I_C is temperature. If the temperature has a variation, if the temperature rises while doing the operation of amplification, suppose the temperature is increasing and we know that if temperature is increasing we know the reverse saturation current, leakage current increases. That we have seen earlier while discussing diode also. For every 10 degree centigrade rise in temperature we have seen

that the reverse saturation current almost doubles. Reverse saturation current increases with rise in temperature mean ultimately I_C will also increase because I_C is equal to beta times of I_B plus beta plus 1 into I_{CO} . If I_{CO} rises because of the rise in temperature ultimately I_C will increase. I_C will increase means again the Q point will be shifted. You may reach again near the saturation or vice versa. If temperature is decreased you will have a decrease in I_C because of fall of I_{CO} and Q point will shift towards cutoff region and this should never happen once you select the Q point. That has to be ensured.

We will discuss about how different biasing schemes operate. We will first discuss the different biasing schemes and then see which biasing scheme is best or better with respect to this shifting of Q point that means stabilization of Q point. We will discuss the stabilization of Q point afterwards. Before that we will start to discuss the different biasing schemes and the simplest biasing scheme is fixed bias. That is a very simple circuit having only resistance in the base region and the collector region. This circuit is just the circuit of the amplifier and mind it here we are applying AC signal and we will get the output AC signal at the collector. These capacitances are there which are known as coupling capacitors to couple the AC signal to the transistor. We will see later the role played by these coupling capacitors. But before that we will concentrate on the DC equivalent circuit for this amplifier.

The fixed bias circuit is this one which is used as the transistor amplifier having NPN transistor and as usual we are discussing NPN transistor in the common emitter. If we consider only the DC circuit for this transistor amplifier then capacitors will be now ignored because these capacitors are open circuit for DC. If we consider the reactance of the capacitor, $\frac{1}{2\pi fC}$ is the reactance. Frequency for this DC circuit is zero. If f is zero then this whole capacitive reactance offered by this capacitance is infinite. When this capacitance is offering infinite reactance there cannot be any current flow. That means it is equivalent to open circuiting this and this part. Under DC condition that means we will have a circuit bereft of these capacitors, without these capacitors, because capacitor is open circuit like DC.

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The DC equivalent for this fixed biased circuit is this one and here in this DC circuit we have to now find out the DC operating point or Q point. DC operating point we have to find out means we have to find out I_C and V_{CE} for this particular I_B , because I_B is set by this resistance R_B . We redraw the circuit conventionally. For easy understanding I am separating the DC source. If we look into the circuit same V_{CC} is there for this base circuit as well as collector circuit. Both the circuits are sharing the same V_{CC} . I can redraw it more conveniently by separating out these two V_{CC} sources. This is the same circuit. Only for easy understanding I have just separated them out.

My analysis will become easier because we now concentrate on the input circuit that is the base emitter circuit. Apply Kirchoff's voltage law in the base emitter loop. Application of Kirchoff's voltage law is V_{CC} minus I_B into R_B minus V_{BE} equal to zero or I can write down what is I_B ? I_B is equal to V_{CC} minus V_{BE} by R_B . This is the base current in this DC circuit which is set by R_B . Others are constant you mind it. Here V_{CC} is constant because we are applying a particular reverse biasing voltage as well as a particular resistance and for that particular R_B , I_B is set because V_{BE} is 0.7 volt for silicon. It is constant. This is the base current. Corresponding to this base current the collector current DC collector current, which is flowing is beta times I_B . I can write this expression again. It is beta into V_{CC} minus V_{BE} by R_B .

This is your DC value of collector current and again in the output circuit that is in the collector to emitter loop, if I consider this loop starting from this point ending again here, apply Kirchoff's voltage law. Algebraic summation of all voltage drop is zero in a loop and applying that I get V_{CC} minus $I_C R_C$ minus V_{CE} is equal to zero. I must start from the same point I must end up in the same point. That is a loop. V_{CC} minus $I_C R_C$ minus DC is equal to zero. From here I get what is V_{CE} ? V_{CC} minus $I_C R_C$. This I_C I have already calculated. From this expression I know what is value of I_C ? I know the value of DC, I know what is the value I_C ? I have now fixed my operating point Q.

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Using KVL in the base-emitter loop,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

or, $I_B = (V_{CC} - V_{BE}) / R_B$ ✓

$$I_C = \beta I_B = \beta (V_{CC} - V_{BE}) / R_B$$

Using KVL in the collector-emitter loop,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

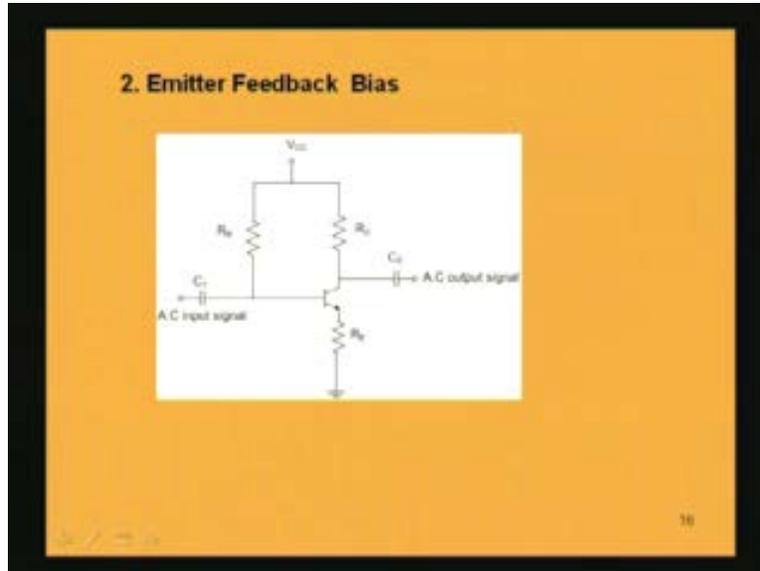
→ or, $V_{CE} = V_{CC} - I_C R_C$

Q(V_{CE}, I_C) is set

This is a simple biasing circuit known as fixed bias. But we will see later on that as for the stability of this operating point is concerned it is not a very good circuit because it is very, very sensitive to beta variation as well as temperature variation and that is very, very evident here. If I have a change of beta it will be affecting this collector current because in this expression itself you can see that beta is coming into that expression. Beta change means the collector current will change. Similarly if I have a change in the temperature, suppose temperature is increasing while operating the transistor then collector current will increase because of the increment of the leakage current I_{CO} . Again that I_C will increase. I_C will increase means V_{CE} will also be affected by that I_C . Whatever Q point I have set now it will be shifted again. Once I set this Q point it is not guaranteed that it will remain in the same position. It will be shifted because of the fact that it is very, very sensitive. This circuit is very, very sensitive to beta as well as temperature. That means it is a not a good circuit.

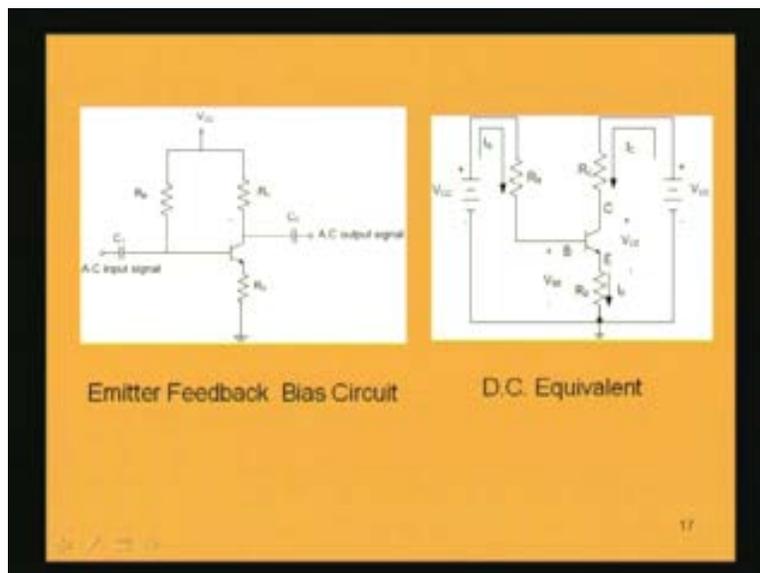
Another circuit for biasing the transistor is emitter feedback bias. Here the emitter is having a resistance. We will discuss later why it is called feedback. But for the time being this is the circuit which is emitter feedback bias. That means the difference between the earlier circuit fixed bias and this circuit is that there is an emitter resistance.

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That is the difference. Other parts are same. In this circuit also if we consider the DC equivalent circuit only that means when DC condition prevails there will be open circuiting by these capacitors C_1 and C_2 . In these two points there will be open circuit.

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We will be only left with this circuit without these capacitors and again I am separating off these two sources V_{CC} , just for easy understanding nothing else. Then I can analyze the circuit. Separately if I consider the base emitter loop apply the Kirchoff's voltage law in the base emitter loop, mind it that through this emitter resistance the current which is flowing is I_E emitter current. What will be this loop equation? V_{CC} minus $I_B R_B$ minus V_{BE} minus I_R is equal to zero. You don't forget about this base to emitter drop. It cannot be neglected or ignored, the base emitter drop which is constant 0.7 volt for silicon.

Simplifying this expression a little I can represent I_E by I_C plus I_B . Representing this I_E by I_C plus I_B I now take I_B common because I_C again can be written as beta times I_B . What will be finally obtained is this expression V_{CC} minus $I_B R_B$ plus beta plus 1 into R_E whole bracket minus V_{BE} is equal to zero. What is the expression for I_B ? I_B I get V_{CC} minus V_{BE} by R_B plus beta plus 1 into R_E . Again I_C is equal to beta times I_B . I_C can be known if I know I_B and I can also know I_E which is equal to I_C plus beta. Starting from this expression I know I_B first. Then I can calculate I_C . When I know beta I can calculate I_C and then I can calculate I_E by simple expression because I_E is nothing but I_C plus I_B or even I can write it as beta times of I_B plus I_B . So beta plus 1 I_B is equal to I_E . This or this (58:10) expression is same.

In the collector emitter loop if I again apply the Kirchoff's voltage law V_{CC} minus $I_C R_C$ minus V_{CE} minus $I_E R_E$ is equal to zero. From this expression I get what is V_{CE} . V_{CE} is equal to V_{CC} minus $I_C R_C$ minus $I_E R_E$. One more step further I can do by some approximation which is very valid approximation because I_E is almost equal to I_C . I_E is in the order of micron. So I can write this expression approximately as, this is actually approximately equal to V_{CE} is equal to V_{CC} minus I_C plus I_E into R_E because if I now consider I_E is equal to I_C , then I can combine these two. V_{CE} is equal to V_{CC} minus $I_C R_C$ minus $I_C R_E$ I can write, which is equal to V_{CC} minus I_C into R_C plus R_E . This is the expression; V_{CC} minus I_C into R_C plus R_E . That means I am taking this I_E to be equal to I_C . With this approximation I get a simpler expression than this. But exact equation is this one. Only simplification a step further will give you this equation.

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Base - Emitter Loop
 Applying KVL
 $V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$
 or, $V_{CC} - I_B R_B - V_{BE} - (I_C + I_B) R_E = 0$
 or, $V_{CC} - I_B R_B - V_{BE} - (\beta I_B + I_B) R_E = 0$
 or, $V_{CC} - I_B (R_B + (\beta + 1) R_E) - V_{BE} = 0$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

So, $I_C = \beta I_B$
 $I_E = I_C + I_B = (\beta + 1) I_B$

Collector - Emitter Loop
 Applying KVL
 $V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$
 or, $V_{CE} = V_{CC} - I_C R_C - I_E R_E$

As $I_E = I_C + I_B$
 $V_{CE} = V_{CC} - I_C R_C - (I_C + I_B) R_E$

Also, $V_B = I_B R_B$
 $V_C = V_{CC} - I_C R_C$
 $V_B = V_{CC} - I_B R_B$
 $V_B - V_{BE} = V_E$

$$V_{CE} = V_{CC} - I_C R_C - I_C R_E - I_B R_E = V_{CC} - I_C (R_C + R_E) - I_B R_E$$

Also here if I want to find out the voltage at this emitter point with respect to ground, that I can find out. Suppose that voltage V_E is equal to I_E into R_E and what is the voltage V_C ? When I mean V_C , I mean V_C that represents with respect to ground. There is the difference between V_C and V_{CE} mind it. V_{CE} is between the terminal C and E but when I say V_C it is the voltage at collector with respect to ground and that is equal to V_{CC} minus

$I_C R_C$ and what is voltage at B? That is V_B equal to V_{CC} minus $I_B R_B$ or again I can write another expression for V_E which is equal to V_B minus V_{BE} is equal to V_E . This also I write. All the voltages and currents I can find out in this circuit. This is emitter feedback bias circuit.

Two circuits we have discussed. One is the fixed bias circuit and second circuit is emitter feedback bias circuit where there is a resistance in the emitter that is R_E . If there is a resistance in the emitter then our whole expression for current and voltage becomes little different from the fixed bias. Fixed bias is the simplest circuit but that is not good for stabilization of the operating point. Once improvement has been done by incorporating the resistance in the emitter how it is going to stabilize the operating point that we will observe later. We have still more circuits for biasing a transistor and these circuits will be further and further improvements over the basic and very naive fixed bias circuit and those we will study gradually one after the other and see the drawbacks as well as advantages of each biasing circuit.