Semiconductor Devices and Circuits

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Lecture – 51
Introduction: Amorphous Semiconductors

So, so far the course is focused on Crystalline Semiconductors. Wherein, we had a periodic arrangement of atoms and we developed models such as the chronic penney model, wherein we used blocks theorem to identify a density of states profile. And in particular we looked at the density of states for 3 d materials, 2 d materials, etcetera. And, we identified a energy a density of state distribution where in we had states above the conduction band edge and below the valence band edge, but then no states inside a band gap.

And, now we reach the last bit of the course, wherein we are going to generalize all these ideas that we develop for a crystalline semiconductors, and in particular talk about non crystalline semiconductor. So, what happens, if the semiconductor is amorphous for example, what happens, if it has got a large number of defects; and, what is the physics that governs this and how do we build devices out of this and how to be model in study the transistors based on such materials.

So, we now look at the device which sort of defines non crystalline semiconductors. And in particular we look at something called as a thin film transistor.

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Thin Film Transistor (TFT)

So, what are the applications of non-crystalline semiconductors?

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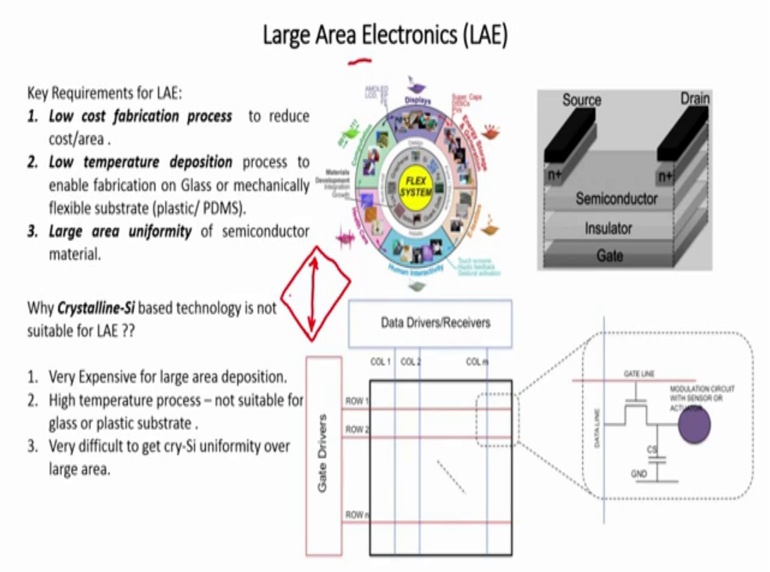

Large Area Electronics (LAE)

Key Requirements for LAE:

1. ***Low cost fabrication process*** to reduce cost/area .
2. ***Low temperature deposition*** process to enable fabrication on Glass or mechanically flexible substrate (plastic/ PDMS).
3. ***Large area uniformity*** of semiconductor material.

Why ***Crystalline-Si*** based technology is not suitable for LAE ??

1. Very Expensive for large area deposition.
2. High temperature process – not suitable for glass or plastic substrate .
3. Very difficult to get cry-Si uniformity over large area.

The strongest application is in the development something called as large area electronics. So, let us consider a display screen ok.

Now, if I have to build transistors etcetera on a substrate that is as large as a display screen. For example, a display screen is several inches to give in several feet in length, and if we need to build all the semiconductors and electronic devices, that are present on the screen using crystalline silicon. One would require either a large tile of these crystalline materials or 1 would require a very very large wafer.

And, both these are going to be quite expensive and it is a probably not the best way to go about building such a large area system. So, what is normally done is you know in order to develop these kinds of largely electronic systems. One starts with a substrate ok.

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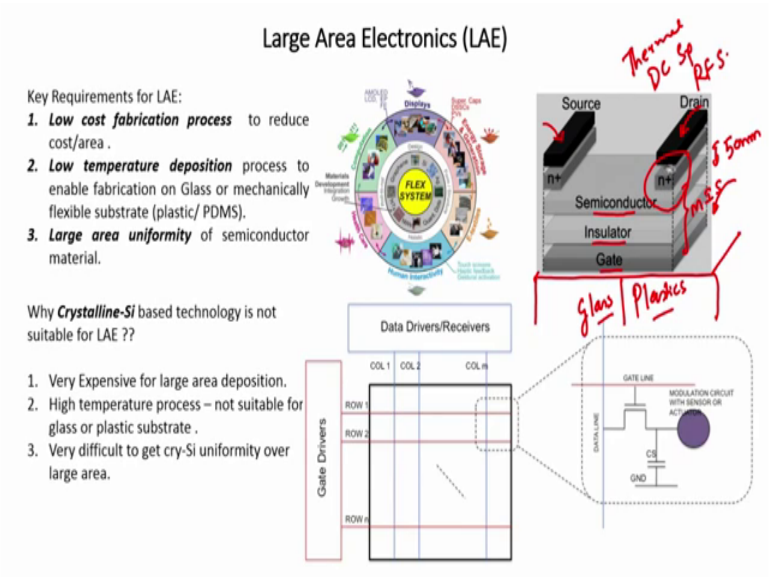

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And, this substrate is not a semiconductor wafer, when it could be any material. For example, glass or even plastics ok. And, on this substrate the different layers of your semiconductor device or the different, the different materials used to build your electronics are deposited as thin films ok. So, for example, if you want needs to build a MOSFET on this large area substrate. This is one possible method that it could be done, we first develop a thin we first deposit a very thin metallic film.

That will constitute the gate of the MOSFET we will then deposit an insulator a thin film that constitutes the insulator. And, then a thin film that constitutes the semiconductor. And, this would constitute the metal insulator, semiconductor stack. And, then we have a source strain electrodes, which if required would need the doping of the semiconductor or some kind of treatment in order to ensure low contact resistance and a good injection of carriers.

So, by depositing is various thin films using processes such as you know thermal evaporation for metals, or you know dc sputtering or RF sputtering for semiconductors or insulators etcetera. We develop these thin filaments of with each layer being about 50 nanometers; thin films of these materials to develop electronic devices.

So, by doing these over large areas and at low temperatures one develops larger electronic systems, for these various applications. Now, the problem of using these kinds of low temperature processes or you know is that we often end up with semiconductors that are not crystalline. So for example, if we take a material and you give all the atoms of the semiconductor.

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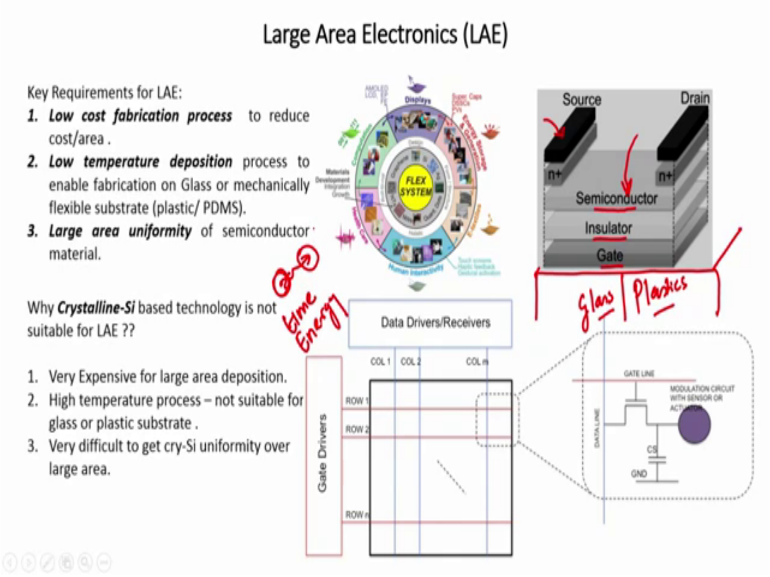

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Enough time and enough energy to move about, and arrange themselves in there least energy positions or the most favorable positions one would end up with the, one would end up with the semiconductor lattice that is almost perfectly crystalline. So, for example, if you look at your silicon wafers; the silicon atoms are allowed to arrange themselves into a periodic lattice, and they are grown from a melt and they given and the growth is done very very slowly.

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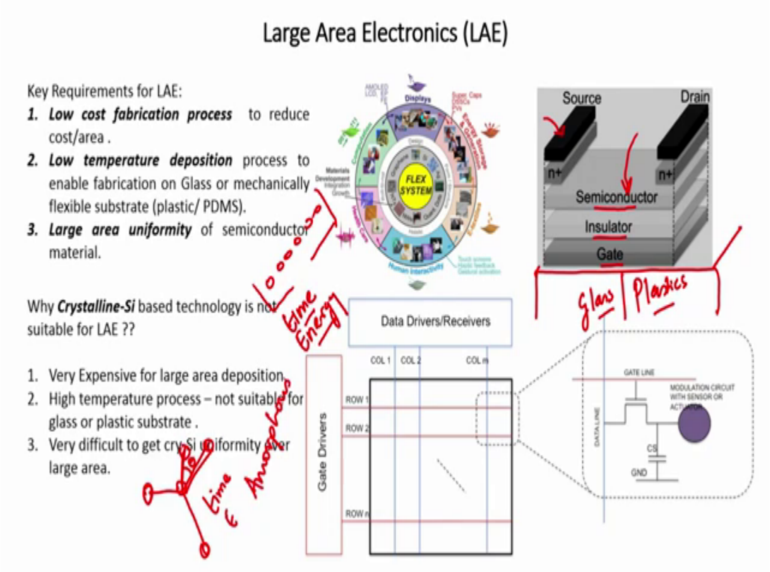

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So, this you are given the atoms enough time and enough energy, but on the other hand if you would do not give enough time or do not give enough energy to the atoms. For example, if you take the melt and you suddenly quench it, you will end up with the material that is quite disordered. The atoms did not have enough time and energy to end up in there least energy positions. And they instead formed a network of randomly arranged atoms. And, these atoms could have different bond lengths it could have they could have different bond angles etcetera.

And, they form a solid, but it is not a crystalline solid. So, you end up with materials that are amorphous in nature. So, generally and not I mean there are there are examples to counter this, generally speaking the kinds of the nature of the semiconductor that is used in the development of these kind of MOSFETs is amorphous ok.

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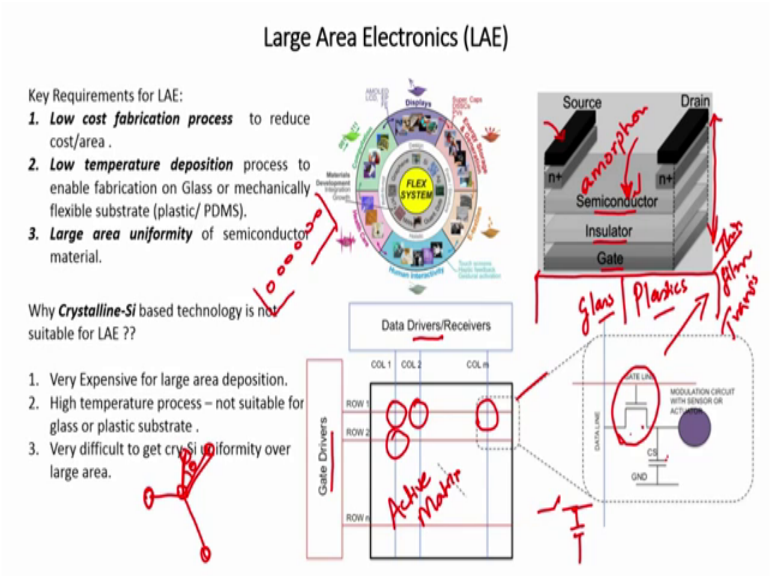

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So, you end up with the amorphous semiconductor or a non-crystalline semiconductor that forms that becomes a part of these devices. And, since these devices are based on thin films, these are also called as thin film transistors. So, they are field effect transistors, but they are just built in a different way on different substrates and called as thin film transistors or TFTs. So, you might have heard of TFT display and that is what this refers to.

Now, the general architecture of a displays like this ok, as shown here. You have gate drivers and you have data drivers, but you have the display has got many tiny pixels ok. And, the size of these pixels determine the resolution of this display. And, inside this pixel inside each pixel, you basically have a switch a capacitor and say a light modulating material ok. Now, the light modulating material could be an led it could be an LCD where in the LCD crystal is oriented in accordance to that brightness that we need etcetera, but the switch is most often a thin film transistor.

So, this switch capacitor circuit is almost a fundamental building block of any active matrix display system ok. And therefore, if one looks at a display screen, the number of pixels present there is equal to the number of transistors present in the display. For a simple for a simple system of this kind of course, you could have you could have larger thin film transistor circuits in each pixel.

And, in general this larger electronics has you know has led to a lot of interesting development in the area of displays, in the area of energy storage systems, in the area of variable electronics. And, since all these transistors can be grown on flexible material, mechanically flexible materials such as plastics, you could also have electronics that you can bend and flex.

So, the amount of applications or the creative use of these kinds of systems is quite large. The application space is quite large.

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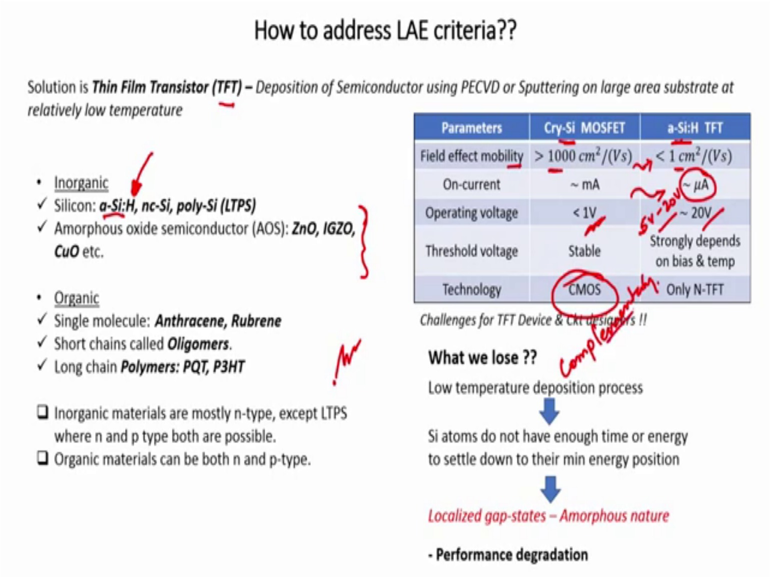

How to address LAE criteria??

Solution is ***Thin Film Transistor (TFT)*** – *Deposition of Semiconductor using PECVD or Sputtering on large area substrate at relatively low temperature*

- Inorganic
  - ✓ Silicon: ***a-Si:H, nc-Si, poly-Si (LTPS)***
  - ✓ Amorphous oxide semiconductor (AOS): ***ZnO, IGZO, CuO*** etc.
- Organic
  - ✓ Single molecule: ***Anthracene, Rubrene***
  - ✓ Short chains called ***Oligomers***.
  - ✓ Long chain ***Polymers: PQT, P3HT***

❑ Inorganic materials are mostly n-type, except LTPS where n and p type both are possible.

❑ Organic materials can be both n and p-type.

Parameters	Cry-Si MOSFET	a-Si:H TFT
Field effect mobility	$> 1000\ cm^2/(Vs)$	$< 1\ cm^2/(Vs)$
On-current	~ mA	~ μA
Operating voltage	< 1V	~ 20V
Threshold voltage	Stable	Strongly depends on bias & temp
Technology	CMOS	Only N-TFT

5V-20V

Complexity

Challenges for TFT Device & Ckt designers !!

What we lose ??

Low temperature deposition process

↓

Si atoms do not have enough time or energy to settle down to their min energy position

↓

Localized gap-states – Amorphous nature

- Performance degradation

So now, that we have seen you know how thin film transistor has grown, what does the, what is the problem? What are the materials used? What are the problems? And, what are the advantages? The advantages clearly are that all deposition etcetera can be done at relatively low temperatures, as compared to crystalline silicon. On the other hand it is come to lot of problems ok.

Now, before we understand the problems, let us look at the typical materials that one could use. For in terms of inorganic some of the common semiconductor materials that are used are amorphous silicon. And, hydrogen is added to amorphous silicon to passivate, you know all some of the disorder particularly dangling bonds.

You could also have poly silicon, which is much much better in terms of performance, but still less compared to crystalline silicon and you also have a amorphous metal oxides.

So, for example, zinc oxide or gallium indium zinc oxide etcetera. And, the semiconductor materials booklet is not limited to just inorganic materials, you also have organic materials.

Say for example, small molecule organic materials such as Anthracene or Rubrene. And, you also have long chain polymer like organic materials. So, it is a it is a quite a large set of materials that one could choose a semiconductor from. Now, nevertheless in all these cases we have some very fundamental limitations.

And, the biggest limitation comes in the form of the mobility of carriers. Now, since we are talking about a disordered material, we find that the effective mobility of your electrons in the material is quite low; so just to give you a comparison.

Here is a comparison of crystalline silicon with amorphous hydrogenated silicon. So, you have a field effect mobility for your transistors ok. The electron mobility in the case of crystalline silicon is about is greater than 1000 centimetre square per volt second ok. Whereas, in the case amorphous silicon is less than one centimeter square per volt second, which means that the speeds are about a 1000 times slower on the other hand the on currents.

And therefore, the on currents in the case of crystalline silicon are about 1000 times larger than amorphous silicon. So, you have currents of the order of milliamps in the case of a transistor that is on whereas, in the case of amorphous silicon and the currents are of the order of micro amps for a transistor that is on. The operating voltages or the voltages required to create the field to make these electrons move is again, you need much smaller voltages in the case of crystalline silicon, whereas, in the case of amorphous materials the voltages do vary from say anywhere between 5 volts to 20 volts. And, this very much depends upon your process, the device structure, and you know the nature of the semiconductor, and particularly the semiconductor insulator interface on the contacts.

And, in crystalline silicon we have both N MOS and C MOS transistors, which means you have a comp complementary metal oxide semiconductor process.

Whereas and we saw that this has a lot of advantages, when it came to circuit design particularly in the development of amplifiers.

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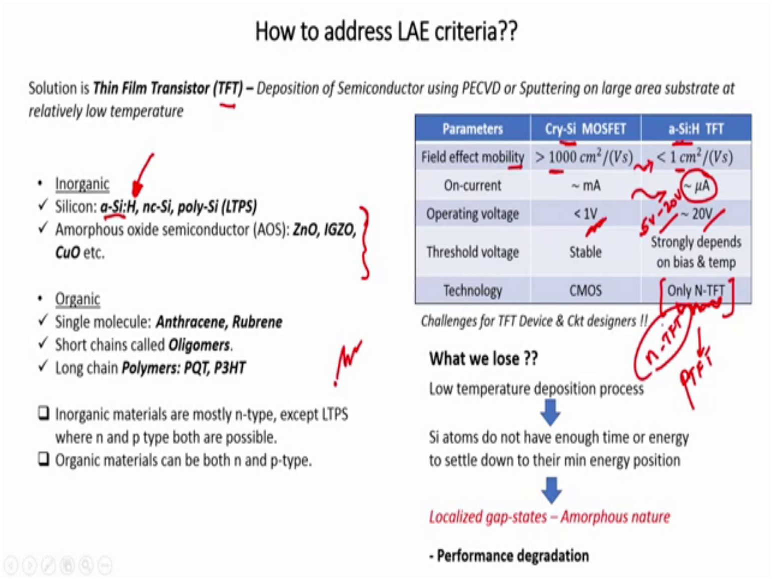

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Whereas, in the case of amorphous semiconductors most of the time. Or in the case of most of the materials practically speaking we only have N type transistors or we only have P type transistors. So, most of the organics gave you p type transistors and say amorphous silicon for example, gives you N type behaviour.

And not and we do not have complementary MOS transistors in most materials. But, having said that, there are also several organic materials that allow you to have both n and p type transistors, which means you do have a C MOS process in these materials.

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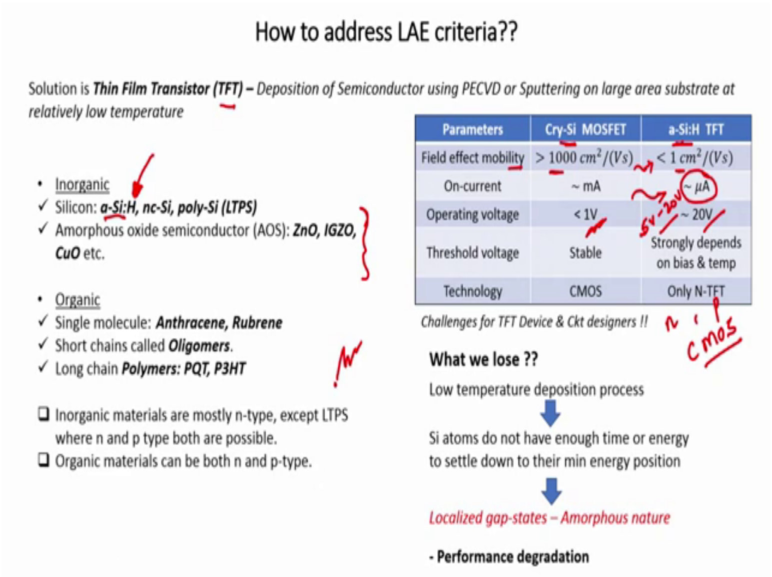

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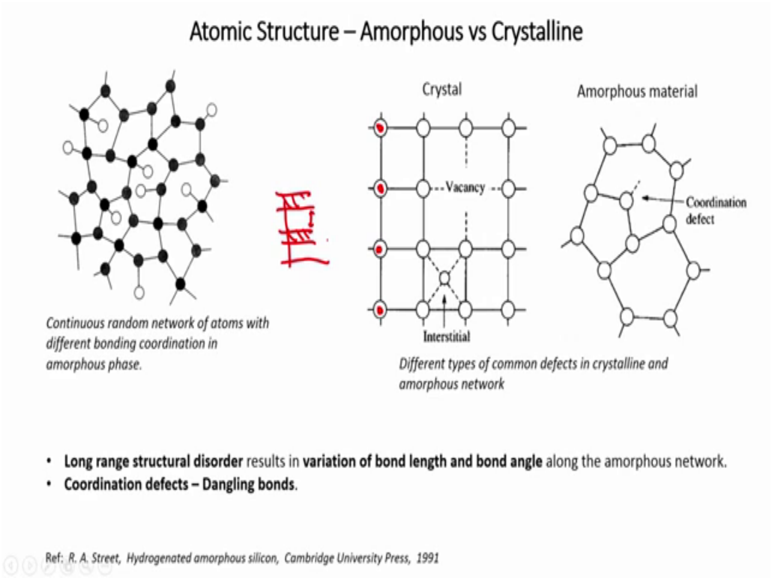

Atomic Structure – Amorphous vs Crystalline

Continuous random network of atoms with different bonding coordination in amorphous phase.

Different types of common defects in crystalline and amorphous network

- **Long range structural disorder** results in **variation of bond length and bond angle** along the amorphous network.
- **Coordination defects – Dangling bonds.**

Ref: *R. A. Street, Hydrogenated amorphous silicon, Cambridge University Press, 1991*

So, let us now look at the consequence of the structure of crystalline and amorphous materials. And, you know what the consequences with regards to the density of states.

Now, the case of crystalline materials we had a periodic lattice ok, you had a nice arrangement of atoms, and you we did have defects, but that is those we have a quite rare ok. And, because of this nice arrangement of atoms one could we saw that, we could use the chronics penny model, and we could use the blocks theorem. And all that led us to the fact that, we have several energy levels and we have clean energy gaps between these energy levels.

So, we had a forbidden gap and that was very very clean.

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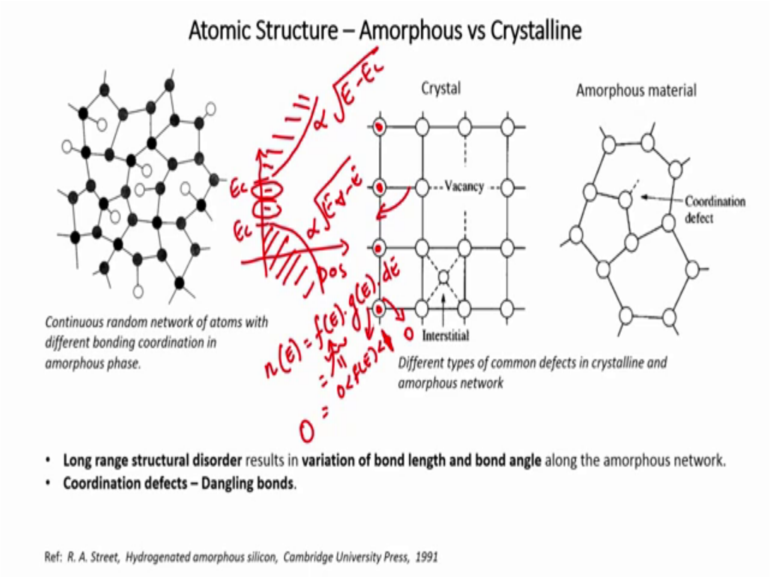

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And, in terms of the density of states picture for a crystalline for 3 D crystalline materials; we saw that, we have the valence band edge, that was the conduction band edge, and we had a density of states. Density of states that varied as the square root of energy, square root of E minus E c and the square root of E minus E v minus E, in that conduction bands and valence bands respectively.

That is behind states in these regions and then we had a band gap with say band gap of energy E g and in the band gap there were absolutely no states ok. So, this was the density of states diagram for a crystalline material.

And, what this meant is meant was that, if you want to count the number of carriers, say the number of electrons, inside the band gap. The number of electrons is dependent ok. And, any energy level E is dependent on the Fermi the value of the Fermi function, at that energy level into the density of states of that energy level d E. And, so, this is the number of electrons per unit volume. And, although the Fermi function had a value that was you know between 0 and 1.

The density of states had a value of 0 inside the band gap. And therefore, this product was equal to 0 ok. So, in other words there are no electrons to be found in the density of states.

However, if say a defect, due to a defect if a few states appear in the band gap, it is possible that that is possible for us to find electrons at these energy levels, depending on the value of the Fermi function and the number of states that appear. So, this was the story in the case of crystalline silicon or crystalline semiconductors.

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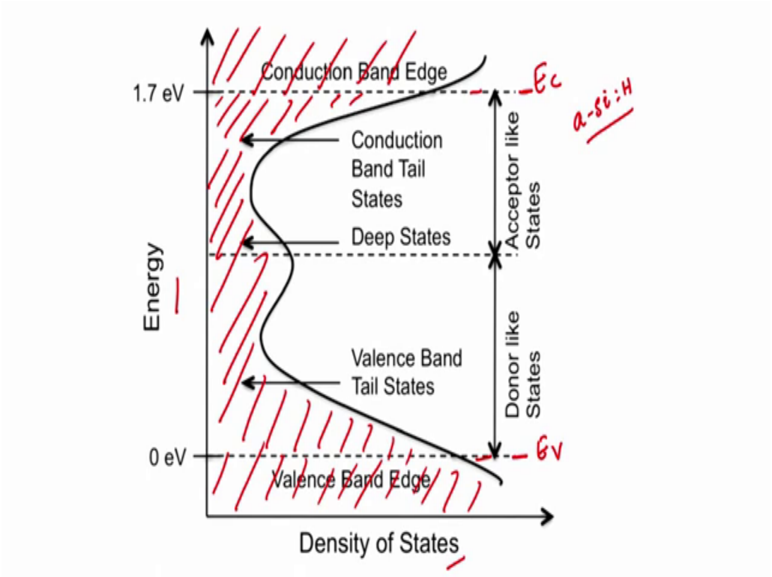

Now, the story in case of amorphous semiconductors is quite different.

So, here we could draw. So, this example this example is shown for amorphous hydrogenated silicon ok, but there is something equivalent for any amorphous semiconductor. So, we could draw something called something equivalent to our conduction band edge. And we could draw something equivalent or valence band edge. And, this is the plot of the density of states versus energy for an amorphous material. So, the first thing that one observes is that there is no clean band gap.

So, here is your conduction band edge here is the valence band edge in the case of crystalline materials, this entire region was void of any states, but in the case of amorphous materials you find that you have a large number of states. So, you have states throughout the band gap or throughout the energy distribution ok.

So, it becomes quite hard to state as to which is the conduction band edge and which is the valence band edge. So, you have states throughout the distribution ok; that is the first point to notice.

And, the only definition for what constitutes the conduction band edge and what constitutes the valence band edge comes from the definition of the mobility of carriers and we will come to that in a minute. So, it is generally seen that carriers sitting above E c move a little faster as compared to carriers that are below E c.

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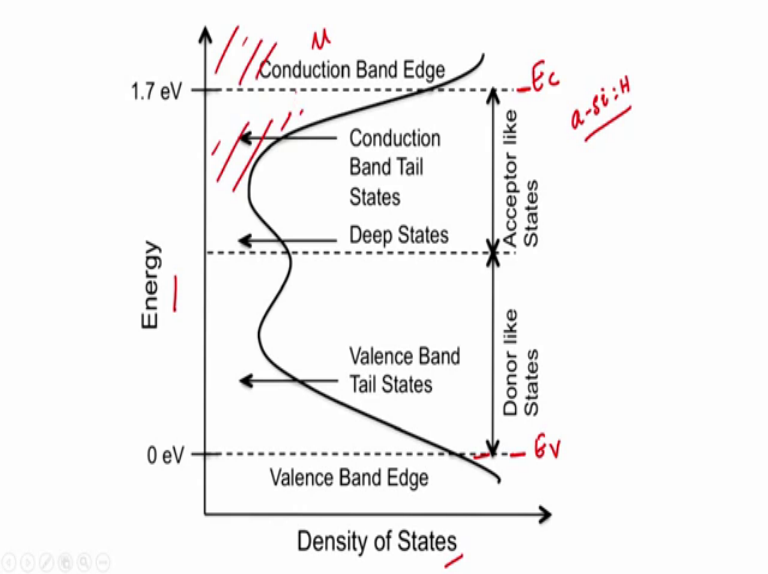

And therefore, all these states that sitting above the conduction bandage, and below the valence band edge are also called as extended states ok.

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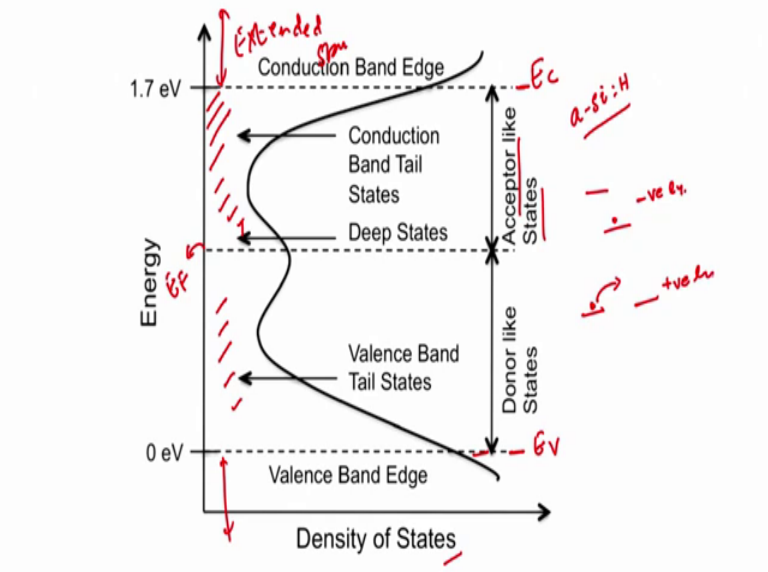

And, we will talk about this in a minute. So, now let us focus on the states inside the band gap. Now, this dotted line here indicates the Fermi level position. Now, all these states that are present in the band gap, and that lie above the Fermi level are called as acceptor like states. And, these are called acceptor like states. Because, they are neutral when they are empty, and the moment an electron occupies these states these states become negatively charged ok. And, the states that lie below the Fermi level are called donor like states.

So, they are neutral when they are filled with an electron. And, the moment an electron leaves them they become positively charged. There are 2 further classification of the states in the band gap. The states that are located near the band edges.

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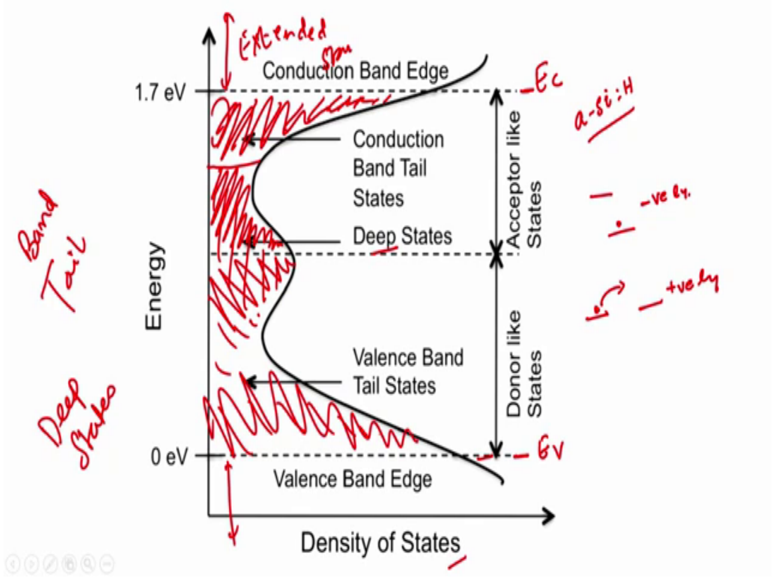

So, that is these regions here and these regions here are called as tail states; or band tail states ok. And, the states that are located in the middle of the band gap, that is closer to mid gap are something called as deep defect states or deep states ok.

So, therefore, one can have acceptor like band tail states that are basically the states here; one can have acceptor alike deep states which are basically the states here close to the mid gap, but above the Fermi level. One could have donor like deep states, which are the states located here, and one could have donor like tail states, which are essentially the states located here.

So, these are definitions these are the definitions associated with that density of states diagram for amorphous semiconductors.

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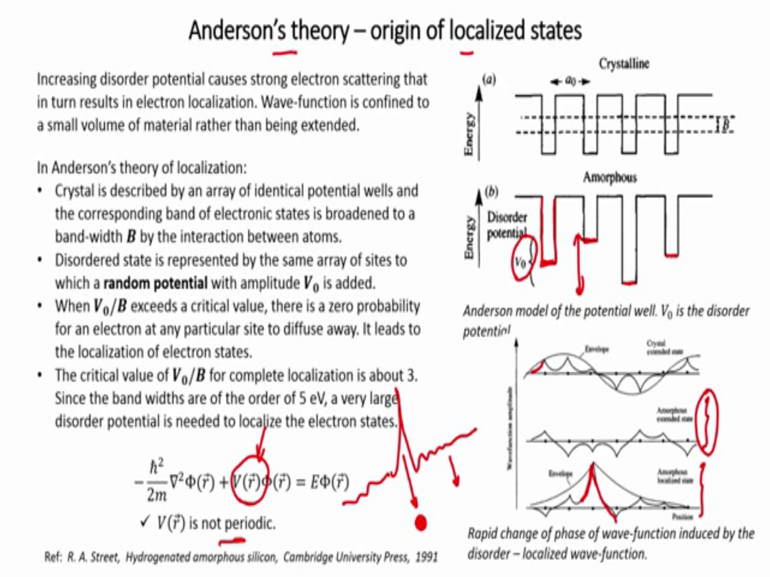

Anderson's theory – origin of localized states

Increasing disorder potential causes strong electron scattering that in turn results in electron localization. Wave-function is confined to a small volume of material rather than being extended.

In Anderson's theory of localization:

- Crystal is described by an array of identical potential wells and the corresponding band of electronic states is broadened to a band-width B by the interaction between atoms.
- Disordered state is represented by the same array of sites to which a **random potential** with amplitude V_0 is added.
- When V_0/B exceeds a critical value, there is a zero probability for an electron at any particular site to diffuse away. It leads to the localization of electron states.
- The critical value of V_0/B for complete localization is about 3. Since the band widths are of the order of 5 eV, a very large disorder potential is needed to localize the electron states.

$$-\frac{\hbar^2}{2m}\nabla^2\Phi(\vec{r}) + V(\vec{r})\Phi(\vec{r}) = E\Phi(\vec{r})$$

✓ $V(\vec{r})$ is not periodic.

Ref: *R. A. Street, Hydrogenated amorphous silicon, Cambridge University Press, 1991*

Anderson model of the potential well. V_0 is the disorder potential

Rapid change of phase of wave-function induced by the disorder – localized wave-function.

So, a key idea with regards to understanding the behaviour of carriers in amorphous materials is defined by something called as Anderson's theory of localization. So, in the case of crystalline materials we found that the crystalline material had a very periodic potential; well, which we used in our model, which was called as a chronic Penney model.

And, we use along with the blocks theorem we found that the electrons, the electron wave function could propagate through the lattice ok. Although, there were very clean gaps, which the electron could not possess, the electron wave function extended through the lattice. And, we had and it permitted electron conduction through the solid. But, in the case of amorphous materials we find that the potential well has got varying levels of disorders.

So, you have you have the floor of the potential well that is quite disordered. In means some sense the material is not periodic or the potential well is not periodic. So, it is a consequence of that, we find that in Schrodinger equation, your potential energy term is no longer periodic. And, as a consequence of that you find that there are 2 possible states in which the electrons could exist.

The electrons that stay above your conduction and valence band, you know which we defined as the extended states. Have a wave function that actually propagates through the solid ok. Whereas, the electrons that are sitting inside the gap states inside the band gap, they have something called as a localization of the wave function.

And what that means, is that, if you look at the amplitude of the wave function, you find that the amplitude or the carriers the amplitude of the wave function is quite large at certain points and is negligible at other points. Which implies so, the probability of finding the particle at these locations is very large and therefore, whereas, the probability of finding the particles in the other locations is very small. Therefore, the electrons could be thought off as just particles that sit there that remained trapped inside these particular states. And, they are not available for conduction in the material.

Now, all this is a consequence of the disorderness or the disorderness of this potential. And, this happens this is a direct consequence when this disorderness crosses a certain of threshold. So, that is what Anderson's theory tells us.

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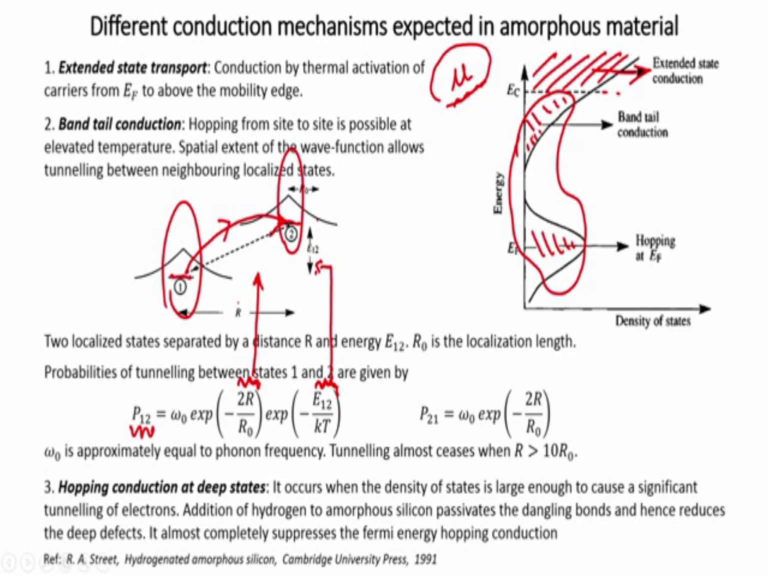

Different conduction mechanisms expected in amorphous material

1. ***Extended state transport***: Conduction by thermal activation of carriers from E_F to above the mobility edge.

2. ***Band tail conduction***: Hopping from site to site is possible at elevated temperature. Spatial extent of the wave-function allows tunnelling between neighbouring localized states.

Two localized states separated by a distance R and energy E_{12}. R_0 is the localization length.

Probabilities of tunnelling between states 1 and 2 are given by

$$P_{12} = \omega_0 \, exp\left(-\frac{2R}{R_0}\right) exp\left(-\frac{E_{12}}{kT}\right) \qquad P_{21} = \omega_0 \, exp\left(-\frac{2R}{R_0}\right)$$

ω_0 is approximately equal to phonon frequency. Tunnelling almost ceases when $R > 10R_0$.

3. ***Hopping conduction at deep states***: It occurs when the density of states is large enough to cause a significant tunnelling of electrons. Addition of hydrogen to amorphous silicon passivates the dangling bonds and hence reduces the deep defects. It almost completely suppresses the fermi energy hopping conduction

Ref: *R. A. Street, Hydrogenated amorphous silicon, Cambridge University Press, 1991*

So, to summarize the different conduction mechanisms in an amorphous material, all them all the electrons or all the carriers that sit above the conduction band edge are said to be sitting in the extended states. And, these electrons are available for conduction. And, you can define a certain mobility for these carriers, and you can define that transport in a manner that is similar to what was defined in the case of crystalline materials.

But, all the electrons that are sitting in the trap states, which is basically the band tails states or the deep defect states. These electrons are more or less trapped ok. And, they are not available for conduction in a manner as seen in the case of electrons in extended states. And, the only way these carriers can move about is via tunnelling or via mechanism called as hopping.

And, a general nature and a general method or a model that describes the transport of carriers in trap states is as shown here. So, you can imagine 2 trap states ok. And, these electrons have got a certain wave function, and this wave function is heavily localized. So, it is got a very large amplitude that sits, you know that very large amplitude at around these locations. And, the probability that an electron moves from state 1 to state 2 or vice versa is given by P 1 2. And, this probability depends upon the distance between these states. As well as the energy differences between these 2 states.

And, it depends as the exponential of the negative of the distance and exponentially the negative of the energy, which implies that if these states are very far apart or if they are located they have very large energy gaps between them. There is a much smaller probability of the electron actually getting from state 1 to state 2.

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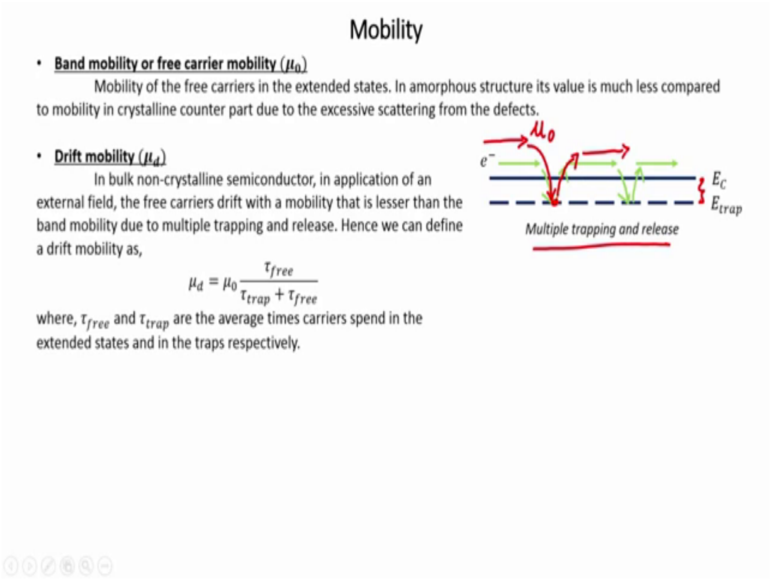

Mobility

- **Band mobility or free carrier mobility (μ_0)**

Mobility of the free carriers in the extended states. In amorphous structure its value is much less compared to mobility in crystalline counter part due to the excessive scattering from the defects.

- **Drift mobility (μ_d)**

In bulk non-crystalline semiconductor, in application of an external field, the free carriers drift with a mobility that is lesser than the band mobility due to multiple trapping and release. Hence we can define a drift mobility as,

$$\mu_d = \mu_0 \frac{\tau_{free}}{\tau_{trap} + \tau_{free}}$$

where, τ_{free} and τ_{trap} are the average times carriers spend in the extended states and in the traps respectively.

Now, with regards to the electron movement in the extended states, the movement can be thought off as shown in this picture here. So, let us say that is the conduction band edge and all these states are the extended states. And, below the conduction band edge and very close to it, there are the trap states that that would try to trap the electrons and hold it and localize them.

So, the movement of the electron in the extended states is described as something called as a multiple trap and release model. And, what happens here is that the electrons move quite quickly in the extended states and they have some mobility called as mobility of mu naught ok. Now, once in a while the electrons get trapped in these trap states.

And, they spend some time in these trap states, but if the electrons are trapped in trap states that are quite close to the extended state edge, which is close to E c. A small amount of energy is can release these electrons ok.

So, let us say a small amount of thermal energy allows these electrons to get free from the trap state and get back into the extended state. So, the movement of the electron is a periodic is a sequence of a extended state transport, and then some amount of trapping, wherein the electron spends some time in the trap states.

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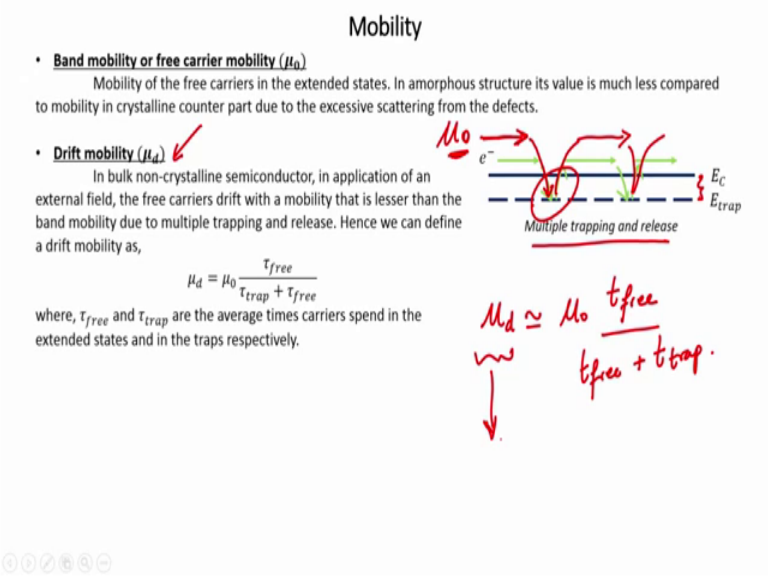

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$$\mu_d \simeq \mu_0 \frac{t_{free}}{t_{free} + t_{trap}}.$$

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And, then gets free again and then moves through the extended states and then gets trapped again etcetera. And, therefore, one can define if one defines the extended state mobility of the carriers ok. Which is which we call the free carrier mobility as mu naught, then the effective mobility that on sees for carriers moving in a disordered material is say mu d which we will call a drift mobility. And, that mu d is given as Mu naught into the time taken time spent by the carriers in the free states divide by the total time spent by the carriers in the semiconductor, which is basically a summation of the total time spent per the carrier in the free states plus the time spent per that carriers in the trapped states.

So, this is the definition of the effective or the drift velocity or the drift mobility of carriers. And, this is the mobility definition, that we would use while trying to define the drift velocity of the carriers.

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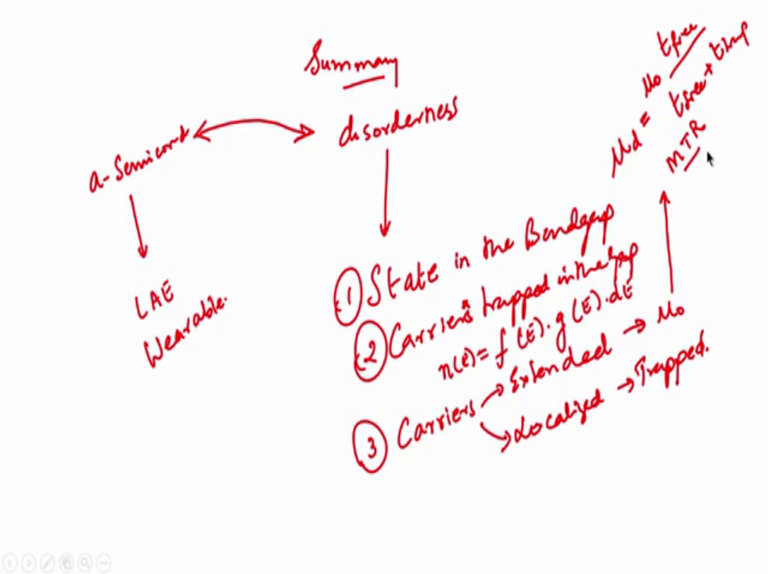

So, just to summarize ok: so everything we have seen so, far. So, we see that we want a amorphous semiconductors, amorphous semiconductors for applications and say may a larger electronic systems or variable electronic systems etcetera, and the consequence of amorphous semiconductors or the consequence of the disorderness of the lattice.

Is that, you have firstly; you have states in the band gap ok. So, the band gap is not clean you have states in the band gap. And therefore, you have carriers trapped in the band gap. And, if one if one is interested in calculating the carrier concentration inside the gap, then we just need to define, you know the density of states in the gap and multiplied with the Fermi function ok.

The third consequence is that the carriers in the gap ok. So, the carriers can either be in extended states where they have a mobility say mu naught or they could be trapped in the gap which are basically a localized states, where they are trapped. And, these carriers do not in any practical sense contribute to conduction in your semiconductor devices.

And, the carriers that are present in extended states can move with an effective velocity given by the drift mobility, defined by the drift mobility, which is nothing but your extended state mobility into this ratio, which is the ratio of the time spent per the carrier in the extended states divided by the total time spent by the carrier in the material which is your T free plus T trapped. And, this is defined by something called as the multiple trap release mechanism.

So, this is the summary of everything we have looked at so far.