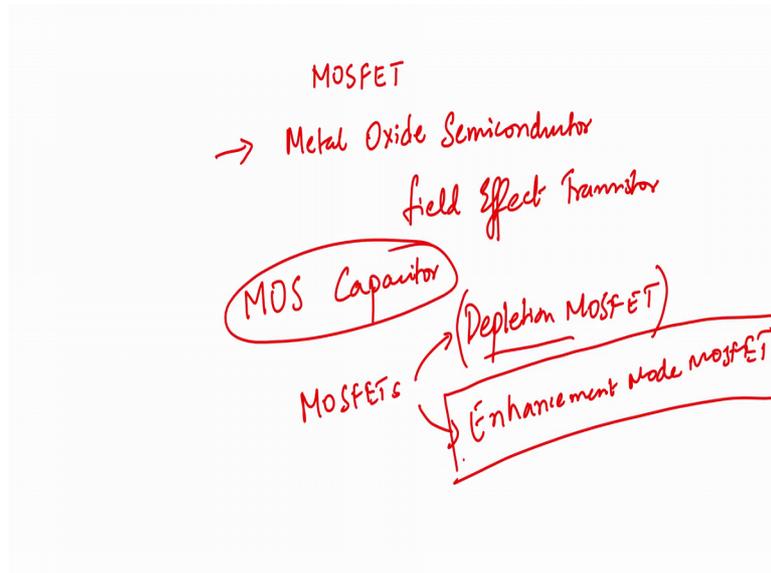


**Semiconductor Devices and Circuits**  
**Prof. Sanjiv Sambandan**  
**Department of Instrumentation and Applied Physics**  
**Indian Institute of Sciences, Bangalore**

**Lecture – 32**  
**Metal Oxide Semiconductor Capacitor (MOSCAP)**

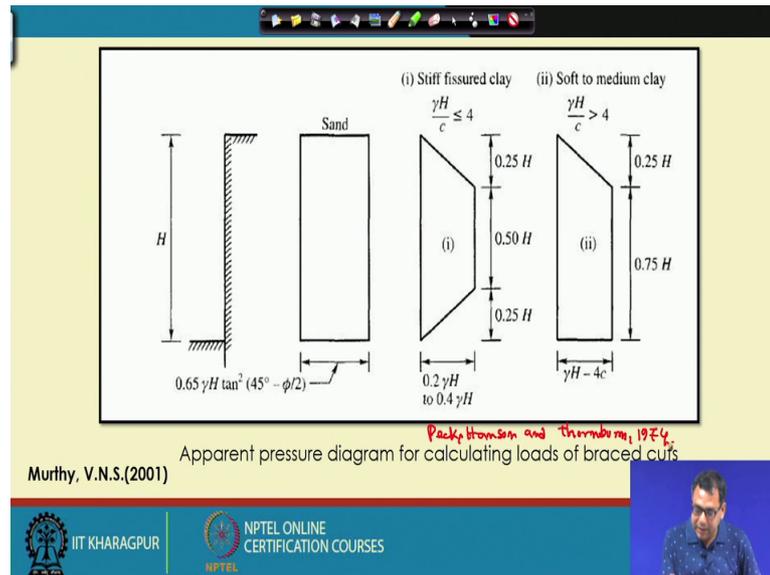
(Refer Slide Time: 00:14)



We will begin our study towards looking at this very important device which is the Metal Oxide Semiconductor Field Effect Transistor and this device is quite important because it is the building block of all modern day integrated circuits ok and before we get to understanding all the details regarding MOSFETs. We will initiate our study on something called as the MOS capacitor that is the Metal Oxide Semiconductor capacitor.

Now, MOSFETS itself I mean there are generally speaking there are two kinds you could say ok. So, you have two modes of operation one is the Depletion MOSFET ok, which is built a little differently from something called as the Enhancement mode MOSFET. The focus of our study is going to be the Enhancement mode MOSFET and before we start this we will look at the MOS capacitor.

(Refer Slide Time: 01:38)



So, the MOS capacitor has got a structure of as shown here. So, you have a Gate Metal you have an Insulator or an Oxide you have a Semiconductor and you have a contact to the semiconductor. So, this gate metal is your control terminal of your MOSFET, when you talk about sending a signal from A to B ok. So, we have not yet built the MOSFET here. So, this is just the MOS capacitor. So, what you see is it just a capacitor circuit.

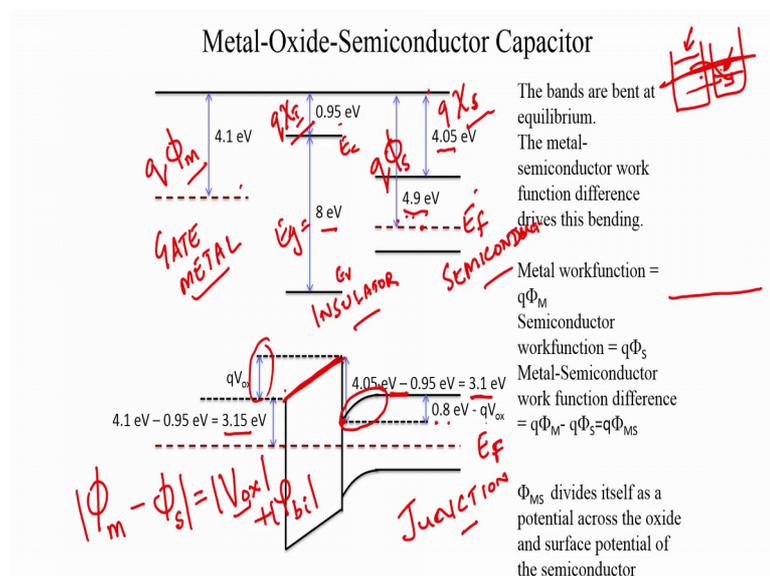
So, this gate metal is given a gate voltage  $V_G$  which is measured with respect to the reference then the reference contact is the back contact. So, here we accept the reference contact ground and this  $V_G$  is with respect to ground. So,  $V_G$  is the GATE VOLTAGE provided to the gate metal and then the gate metal sandwiches an insulator sandwiched between the gate metal and the semiconductor ok. So, this is a very key difference. So, which means that if this insulator is an ideal insulator there is no current flowing from the gate to the semiconductor so, this current is ideally 0 at low frequencies ok. So, you have a gate metal and you have an insulator.

Now, since this insulator in the case of silicon technology since the most commonly used insulator is silicon oxide or some other oxide the insulators also called as an oxide layer. So, that is why you have this main metal oxide semiconductor a good equivalent name is metal insulator semiconductor and the insulator sits on top of a semiconductor and this semiconductor is likely doped either P or N type ok, but in this case for our example and for this study we will consider a P doped semiconductor.

So, you have the gate insulator semiconductor and back contact or the reference terminal, which provides not only the voltage reference, but which also supplies this semiconductor layer with an infinite source of carriers ok. So, this is the structure that we will be looking at and we let people analyze for some time. Now, as usual let us start looking at the band bending diagram ok. So, let us say be a good it take the a metal the gate metal we will we will not worry about this back contact we will just assume it is an ideal Ohmic contact not worrying so much about it, because everything that is interesting with regards to this device and with regards to the study happens here at the insulator semiconductor interface. So, this is the region of interest ok because that is where the junction is ok.

So, we are basically creating a junction since we have looked at junctions of typically all our junctions have been a metal semiconductor junction or a P N junction, but here you are looking at a gate insulator and an insulator semiconductor junction ok. So, since this is our region of interest all our focus will lie in this particular region.

(Refer Slide Time: 05:16)



So, let us draw the band diagram. So, I have just thrown in some numbers just to give you a feel for some typical values. So, we have three different structures. So, first let us say this is the GATE and this is the GATE METAL. So, we have chosen a metal whose work function is 4.21 electron volts this is the insulator or the oxide and we have chosen an oxide or an insulator whose band gap is about 8 electron volt, so, it is a large band

gap. So, that is the conduction band that is the millions band and that is a large band gap in the insulator and the electron affinity of the insulator ok.

So, the electron affinity for the insulator is about 0.95 electron volt. So, the electron affinity has to be a constant and is irrespective of what kind of junction you create or what bias you apply etcetera and similarly the work function for a metal is a constant once you pick a metal you pick the work function and then finally, you have a semiconductor. So, we have not yet created the junction in this diagram. So, we have the semiconductor and here you have some band gap.

So, for example, let us say the band gap is about if you take silicon it is about 1.12 electron volt, ok. We have some band gap and the semiconductors doped P type which means that the Fermi level of the semiconductor lies a little below mid gap ok, it is closer to the valence band edge is compared to the conduction band edge because it is doped P type and the work function of the semiconductor is the difference between the vacuum energy level and the Fermi level of the semiconductor and that is about 4.9 electron volt, so that is that is what we have chosen. So, these numbers are just examples I mean these are not the only numbers that you have to use I hope that is obvious and the electron affinity of the semiconductors again a constant. So, once you pick the semiconductor your picked electron affinity and let us say the electron affinity is about 4.05 electron units.

And now we are going to create a junction. So, when you create the junction the work function of the metal will not change, the electron affinity the insulator will not change and the electron affinity the semiconductor will not change and if it is a thermal equilibrium the Fermi level will align ok.

So, let us say we have now created the junction, we have brought these three pieces together and we have now created a junction and that junction is shown in this figure here. So, what happens? So, here you have the metal. Firstly, the work or the Fermi levels of a line the metal Fermi level is in the same position as the semiconductor Fermi level ok and since there was some work function difference between the metal and the semiconductor in order to align these two Fermi levels there has to be some residual voltages ok, because charge has been transferred and in this case charge has been transferred from the metal to the semiconductor.

So, here is an interesting question. So, far we have when whenever we did a band diagram at thermal equilibrium let us say it is a p n junction or a metal semiconductor junction. We said that the Fermi levels align at thermal equilibrium and the Fermi levels align because of the charge transfer and very early on we looked at you know some very poetic analogies like you know water in a bucket. So, you have these two buckets and you have less water here and more water here and this correspond to a Fermi level that was higher or you know work function that was lower whereas, this corresponds to a work function that is higher and when you merge these two buckets the water flows from that here there by aligning the Fermi levels ok.

So, we looked at all these analogies and we know it had a mathematical derivation of you know why the Fermi levels should align at thermal equilibrium because the flux, so the carriers have to be balanced, but here is the question. So, for the Fermi levels to align you need to have charge transfer like for example, in this case electrons are moved from the metal to the semiconductor, but you now have an insulator sitting in the middle. So, the question is how did the charge transfer ok.

So, there is something for you to think about, but let us just say that the charge did transfer and the Fermi levels have aligned and this is a reasonably good assumption ok. So, the metal has transferred electrons to the semiconductor which means there is going to be some band bending in the semiconductor, but since there is also an insulator the driving force for any band bending which is the metal semiconductor work function difference leads to not only a built in potential in the semiconductor, but also a potential across the insulator or the oxide.

So, this difference in the metal and semiconductor work functions is the driving force for the band bending and this difference is split between the built in potential of the semiconductor and the voltage drop across the oxide, but then what else do you see here. So, since at this edge now let us come to this particular edge lets come to the met the gate metal insulator interface, so, you see this barrier here.

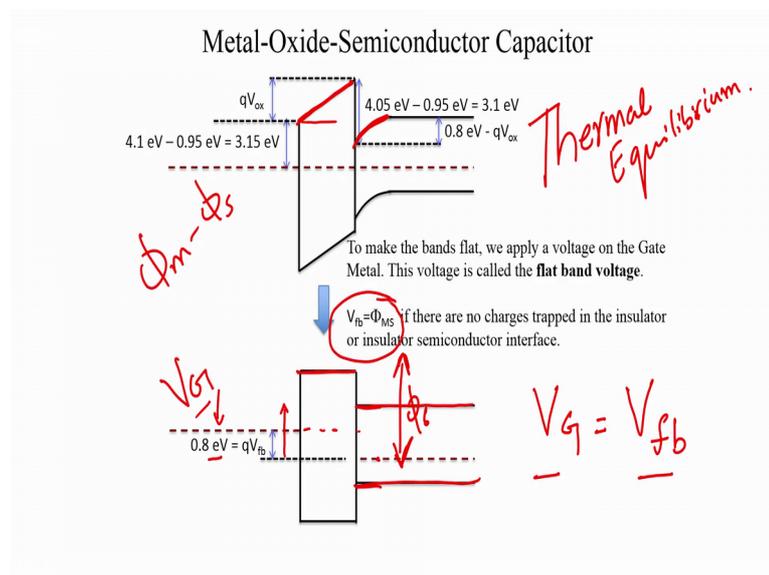
Now, since at this point the electron affinity of the insulator was about 0.95 electron volt and the electron affinity of the semiconductor of the gate of the work function of the gate metal at this point is 4.1 electron volt. So, that is 4. 1 electron volt and therefore, since

these two are constants this barrier height has to have a value that is the difference of these two energies and that is going to be about 3.15 electron volt.

So, similarly you can do the same thing for the semi conductor insulator interface the semi conductor. So, if you look at this particular point here with where the conduction band is meeting the insulator at that particular point the semiconductor has got a well has got an electron affinity of 4.05 electron volt the insulator has an electron affinity of 0.95 electron volt and therefore, this barrier is going to be the difference of those two energies and it is going to be about 3.1 electron volt. And this work function difference that is if you think of it in voltages, so we have removed the  $q$  here. So, we are looking at the voltages now this work function difference which is say  $4.1 - 4.9$  minus  $4.1$  ok.

So, that work function difference. So, in this case the work function of the semiconductor is larger. So, let us say well let us just instead of using negative signs let us just say its  $\phi_{MS}$  let us just take the modulus of all this ok. So, this work function difference has led to a drop of  $V_{ox}$  across the oxide. So, that is why you see that there is an electric field in the oxide ok and the remaining which is  $0.8$  electron volt minus  $q V_{ox}$  is the energy difference between the bulk conduction band and the point, where the conduction and the point near the interface the conduction band energy near the interface ok. So, this is what happens when you form the junction, when you form the metal insulator semiconductor and junction.

(Refer Slide Time: 14:10)



So, this is all at thermal equilibrium. So, we have formed the junction and it is all sitting at thermal equilibrium with the Fermi levels aligned and we see that simply because of the work function difference between the metal and the semiconductor, you have all this band bending, you have an oxide that is got a built in field, you have a semiconductor with a built in field and we can now solve Poisson's equation here and estimate the field etcetera.

Now, the question is how do I not have any band bending ok, let us say I want to make all these bands flat again ok. So, which means that I want to get the bands back to the way they were before the junction was formed, but I want to do it when after the junction has been formed ok. So, I do not know if I am clear enough, but the point is in order for me to get these bands to be flat again artificially, what I need to do is I need to apply a voltage on the gate ok, I need to apply a voltage on the gate and by applying a voltage in the gate what we are essentially doing is we are going to recreate the initial Fermi level difference.

So, that is the metal work function, that is the semiconductor work function and we want to recreate the difference of 0.8 electron volt because the only way we are going to get the bands to be flat is if you go back to if you get the metal and semiconductor to have a work function difference that is 0.8 electron volt.

So, you want the metal to you want the metal Fermi level to go up relative to the semiconductor Fermi level and this has to be done by applying a gate voltage. So, when you since we are looking at in all these band diagrams, we draw it is all drawn such that the electrons run downhill and the holes like to run uphill, which implies that if I apply a positive voltage to the metal all the energy levels will go down and if I apply a negative voltage to the metal the energy levels will all start moving upward ok.

So, essentially what we need to do in this case is apply a negative voltage to the metal and shift the metals Fermi level upward by about 0.8 electron volt. So, if you can create this difference of 0.8 electron volt between the metal and the semiconductor Fermi level then we can get all the bands to be flat because we have removed the cause that created these built in potentials.

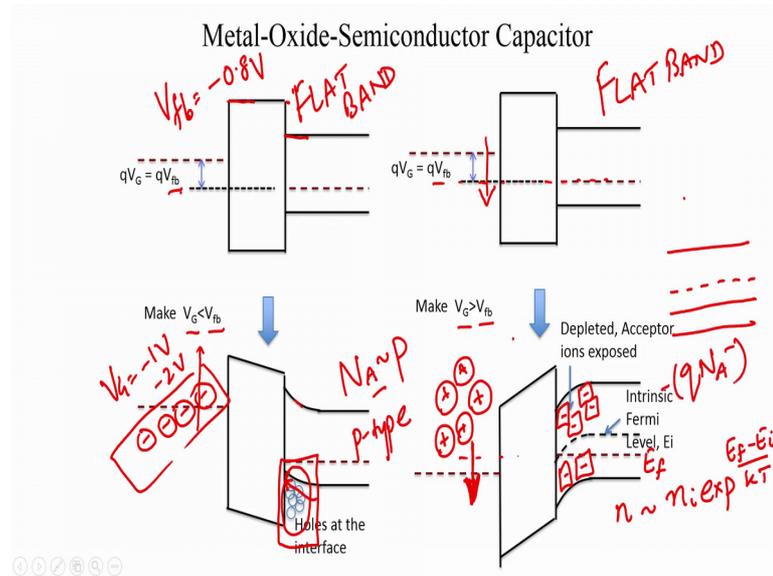
So, you can see that the insulator the bands are all flat here, the semiconductor does not have any band bending and all the band bending has disappeared, but of course, we are

now not at thermal equilibrium because we are applying a gate voltage and therefore, the Fermi levels are not aligned at this point and the moment you remove the gate voltage the material head back towards equilibrium with the metal transferring electrons to the semiconductor and therefore, the conduction band edge near this interface will start bending towards the Fermi level in the semiconductor.

Now, this gate voltage needed to create this flat band condition ok, something called as a flat band voltage ok. So, this is a technical term ok. So, at thermal equilibrium we had some situation it need not always be this is the situation for the numbers we have chosen, the bands could be bent the other way it really depends on what the work function differences are what the work function difference is between the metal and the semiconductor, but in our particular case the bands were bent downward and in order to achieve flat band condition we needed to apply this gate voltage and the gate voltage at which the bands become flat that is the gate voltage at which there is no potential drop across the oxide and there is no built in potential in the semiconductor is something called as the flat band voltage and we will give it a special symbol we will call it  $V_{fb}$ . So, when my  $V_g$  is equal to  $V_{fb}$  all my bands are flat ok.

So, in this particular case we need our  $V_{fb}$  is definitely your  $\phi_{ms}$  which is the work function difference between the metal and the semiconductor. It is not the work function sorry the work function difference divided by  $q$ . So, if you are looking at the potential here, so  $V_{fb}$  is the potential it is not energy all right.

(Refer Slide Time: 19:11)



So, now let us say what happened? Let us start playing with this system ok. So, this is our flat band condition, so let us look at the figure on the left hand side first. So, this is our flat band condition you see there is no banding there is no bending of bands in the semiconductor, there is no band bending in the insulator and that is because we have artificially applied we have applied a gate voltage  $V_g$  which is equal to  $V_{fb}$  which is the flat band voltage.

So, now let us say we start making  $V_g$  further we start making  $V_g$  less than  $V_{fb}$  ok. So, we have already applied a negative voltage we start making it more and more negative ok. So, let us say in this case  $V_{fb}$  was what  $V_{fb}$  was minus 0.8 volts because  $\phi_m$  was  $\phi_m$  is 4.1 electron volt,  $\phi_s$  is 4.9 electron volt and  $\phi_m - \phi_s$  which is  $\phi_m$  minus  $\phi_s$  is going to be minus 0.8 volts. So, that was our flat band voltage.

And now we are going to make  $V_g$  less than  $V_{fb}$ . So, which means that let us say we start making  $V_g$  equal to minus 1 volt and then minus 2 volts etcetera. So, what are we doing? So, we are further increasing this difference between the metal work function and the semiconductor work function. So, the metal Fermi level will start moving further away from the semiconductor Fermi level and it will move it will increase this energy gap between energy difference between these two levels.

So, this means that at  $V_g$  equal to  $V_{fb}$ . We were at flat band and if I make it further negative, then we are again going to drift away from flat band, but in the opposite

direction ok. So, since my  $V_g$  has now become minus 2 volts you will find that the bands start bending the other way ok. So, the electric field in the oxide is going to change direction and you are going to have band bending in this manner and the bands and the semiconductor will start tilting upward ok, as compared to the downward tilt it had at thermal equilibrium it will now start bending the other way because we are making  $V_g$  less than  $V_{fb}$ .

And when we start making  $V_g$  less than  $V_{fb}$  this band bending is going to encourage all the majority carriers since remember this is a P type semiconductor and it is got a lot of holes ok. So, for example, if its doped with the doped concentration of  $N_A$  and if all these dopants are ionized then the hole concentration is about  $N_A$  if  $n_a$  is much greater than the intrinsic carrier concentration. So, plenty of holes and these holes are going to start running up the hill and they are going to accumulate at the interface. So, as I make  $V_g$  as I continue making  $V_g$  less than  $V_{fb}$  they are going to encourage holes to appear at the interface.

Now, let us go the other way around. So, let us say we head back to a flat band condition and the way we go back is we start bringing this voltage higher and we make it equal to the  $V_{fb}$ . So, let us say we are back at flat band and now we start taking  $V_g$  the other way around. So, we make  $V_g$  greater than  $V_{fb}$  ok, now all as you start making  $V_g$  greater than  $V_{fb}$  the Fermi level of the metal will start moving downward ok and you know we will pass. So, here we have crossed the thermal equilibrium point when these two fermi levels were aligned. So, as you start pushing the metal work function metal Fermi level below, you will reach the point where it was you know you will artificially recreate the thermal equilibrium point because you are to set  $V_g$  equal to 0. So, you will make you are moving from  $V_g$  equal to minus 0.8 volts through 0 which is your equilibrium state and now beyond 0.

So, let us say we make it 0.1 0.2 etcetera. So, we start increasing  $V_g$  ok, so, when  $V_g$  is greater than  $V_{fb}$  the bands start bending the other way. So, because we are now pushing the Fermi level of the metal below the Fermi level of the semiconductor and what happens at this stage. So, we are now started adding positive charge on the gate. So, when  $V_g$  was less than  $V_{fb}$  we were adding negative charge on the gate right, we were applying a negative gate voltage and all this negative charge in the gate was balanced by the positive positively charged holes at the interface.

But now by making  $V_g$  greater than  $V_{fb}$  you started adding positive charge on the gate. So, how is this positive charge in the gate balanced? This positive charge in the gate is balanced by two mechanisms the first is that the semiconductor starts getting depleted near the semiconductor insulator interface, so that is the first reaction. So, what does depletion do it exposes all the fixed negatively charged acceptor ions.

So, it is a P doped semiconductor it has got negatively charged acceptor ions and free electrons which have given up holes to the semiconductor and these negatively charged acceptor ions or the space charge starts getting exposed. So, this region is depleted, so that, firstly compensates for any positive charge that you are applying on the gate and this bending of the bands begins to encourage the negatively charged electrons and encourages them to appear at the interface. So, you have two potential mechanisms the negatively charged electrons and the negatively charged space charge, which is the negatively fixed negatively charged fixed acceptor ions in the semiconductor that can balance the positive charge on the gate.

Now, the electrons will not appear till  $E_f - E_i$  is going to go greater than 0 ok. So, what does that mean? So, we have also shown the intrinsic Fermi level, so this is the Fermi level after doping. So, you have the semiconductor it initially had an intrinsic Fermi level position and then after doping we created that we shifted the Fermi level to a both P type semiconductor and we are using the P type to create your MOS capacitor, but having said that I have just indicated the intrinsic Fermi level.

So, this is the Fermi level after doping and this is the aligned Fermi level and we have also indicated the intrinsic Fermi level here ok and that is an it is a very good indicator because if you recollect your electron concentration is dependent on the exponential of  $E_f - E_i$  by  $K T$  ok.

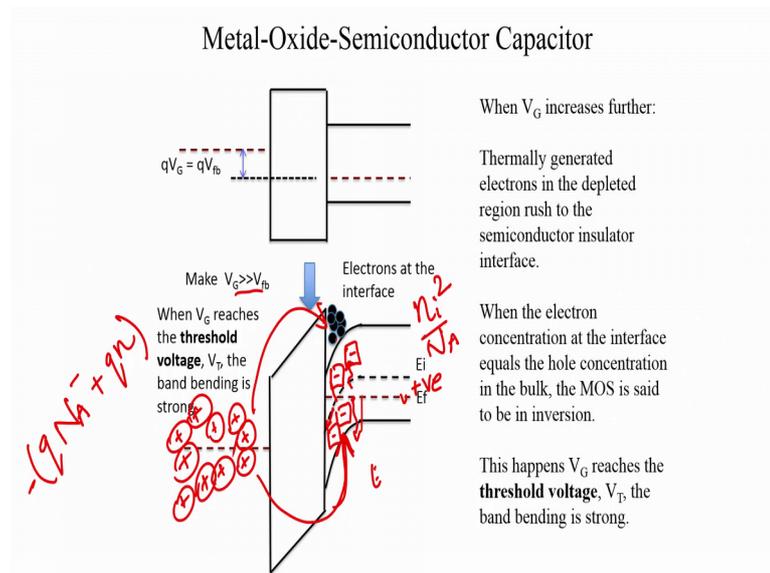
So, it is only when  $E_f$  is greater than  $E_i$  when the electrons start appearing. So, as you are bending the bands so, for a very low positive gate voltage, so, very so, let us say  $V_g$  is just slightly above  $V_{fb}$  the bands would not have bent that to that extent. So, let us say the bending was only so, let us say this is the Fermi level and let us say the intrinsic Fermi level has just bent this much.

So,  $E_f - E_i$  is still negative in this case ok,  $E_f - E_i$  and that is  $E_i - E_f - E_i$  is still negative and therefore, you do not have so many electrons at the interface, but all the

charge all the positive charge in the gate is being compensated by the exposed acceptor ions ok. So, that is the depletion region, but the moment you make the gate voltage more and more positive  $E_f$  at some point will start bending more and more  $E_i$  start bending more and more and it will ensure that  $E_f$  minus  $E_i$  becomes positive near the interface.

So, that is when the electrons start participating ok. So, in this case we have just made  $V_g$  slightly greater than  $V_{fb}$  and it is mostly the acceptor like ions that are being depleted the semiconductors depleted and expose the acceptor like ions.

(Refer Slide Time: 28:53)



But then as I mentioned if I you make  $V_g$  much greater than  $v_{fb}$ . So, when I say much it just simply means; that, we have bent we have managed to make the band bending so large or so severe that if I were to imagine, what the intrinsic Fermi level would be doing it would have gone past the Fermi level of the semiconductor. So,  $E_i$  has; so, if you look at  $E_i$  minus  $E_f$  in the bulk it is negative, but  $E_i$  minus  $E_f$  in the bulk is positive and  $E_i$  minus  $E_f$  in the at the interface has now become negative ok, or in other words  $E_f$  minus  $E_i$  at the interface has become positive.

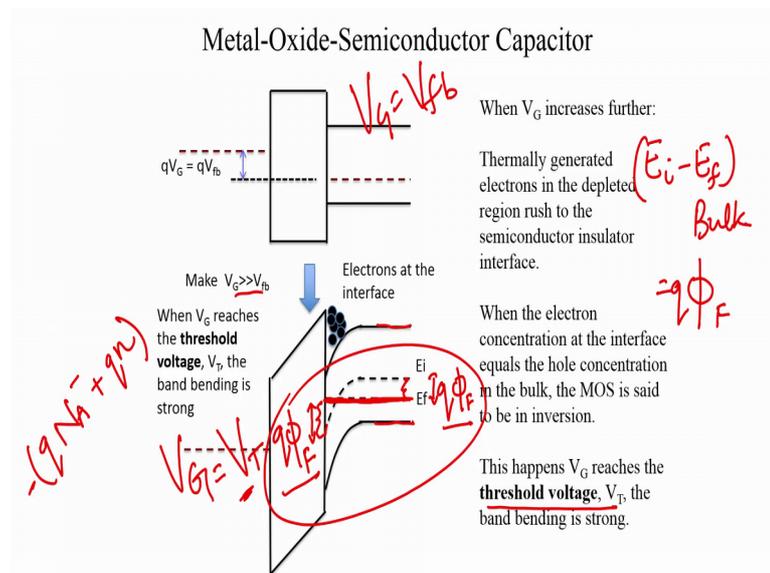
So, at this point we will start encouraging electrons to start appearing at the interface ok, because the band bending is. So, severe now where are these electrons coming from? There are no electrons in the P type material ok, so the type material has got very few electrons its only got  $n_i^2$  by  $N_A$ . So, these electrons are not you know there are migrating ok, definitely not these are electrons that are thermally generated in the

depletion region. So, we had this depletion region before heading here. So, we have these exposed acceptor ions ok, you still have the depletion region here, but beyond a certain point electrons also start participating and these electrons are thermally generated in the depletion region ok.

Since your region is depleted it encourages generation of carriers and these are thermally generated carriers and our depletion region and is those electrons that start appearing at the interface. And now to compensate for the heavily positively charged gate because your  $V_g$  is now very large. So, you have a strong positive charge on the gate metal, this positive charge is now compensated by not only the exposed acceptor ions ok. So, these acceptor ions the space charge but also by the negatively charged electrons. So, both  $qN_A$  minus and  $qn$  start compensating for the positive charge on the gate.

Whereas in the previous case when  $V_g$  was just slightly greater than  $V_{fb}$  and  $E_i$  was not yet bent so much. It was mostly it was only the acceptor ions that was compensating for the gate charge. Now the bending the bending could become more and more severe and we reach a point we could reach a point at some particular gate voltage, we reach a point where the  $E_i$  minus  $E_f$  in the bulk matches or becomes equal to the  $E_f$  minus  $E_i$  at the interface ok. So, what does that mean? So, let us say we define we define the  $E_i$  this energy difference ok.

(Refer Slide Time: 32:22)



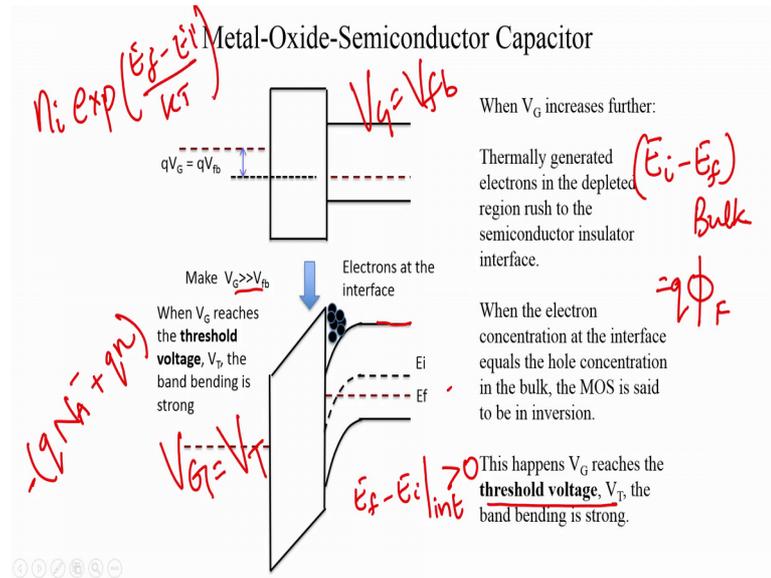
So, let us say we say  $E_i$  minus  $E_f$  in the bulk of the semiconductor bulk means very far from the interface. So, this region here it knows nothing about the junction formation ok, the semiconductors as it works. So, you have the Fermi level there you have the valence band there and you have the conduction band and we this dashed line here there are two dashed lines ok, but what the black one if you can see it is  $E_i$  ok. So, that is  $E_i$  all right and I will draw  $E_f$  as a continuous line just for clarity.

So,  $E_i$  minus  $E_f$  in the bulk is let us say we will give it a special symbol we will call it  $\phi_F$  ok. So, we will say that this difference is that is a  $q\phi_F$   $q\phi_F$ . Now at the interface the band bending has become so, severe that  $E_i$  is bent to such an extent that  $E_i$  has gone below  $E_f$ , but there is a special point where then  $E_i$  is as much below  $E_f$  near the interface as it is above  $E_f$  in the bulk ok. So, if you look at this difference let us call this energy difference also equal to  $q\phi_F$ .

So, let us say we have applied a gate voltage at some particular gate voltage the band bending is such that, this difference between  $E_i$  and  $E_f$  this modulus of this difference is same as the difference between  $E_i$  minus  $E_f$  in the bulk. So, let us say this is  $q\phi_F$  and at some particular gate voltage this difference also becomes  $q\phi_F$  ok. So, at this gate voltage we say that the MOSFET has reached threshold voltage or threshold operation ok. So, this gate voltage, so, just like how we define the flat band voltage and we said that the gate voltage, when the gate voltage equals the flat band voltage is the bands become flat. So, then and  $V_g$  was equal to  $V_{fb}$  the bands became flat and when  $V_g$  is equal to the threshold voltage you would have this condition ok and the threshold voltage is given by a special symbol  $V_t$  and it is an important modeling parameter ok.

And we say that when we build MOSFETS we say that the MOSFET is considered to be on or you know in or it has got a significant current through it, when the only after  $V_G$  crosses  $V_T$  ok. So, but  $V_T$  is not some kind of a magical boundary it is not that the electrons are waiting in the background and saying that you know let us just wait and  $V_g$  still not reached  $V_T$  that is definitely not the case, it is just a very useful modeling parameter ok. So, for example, even when the band bending is here for example.

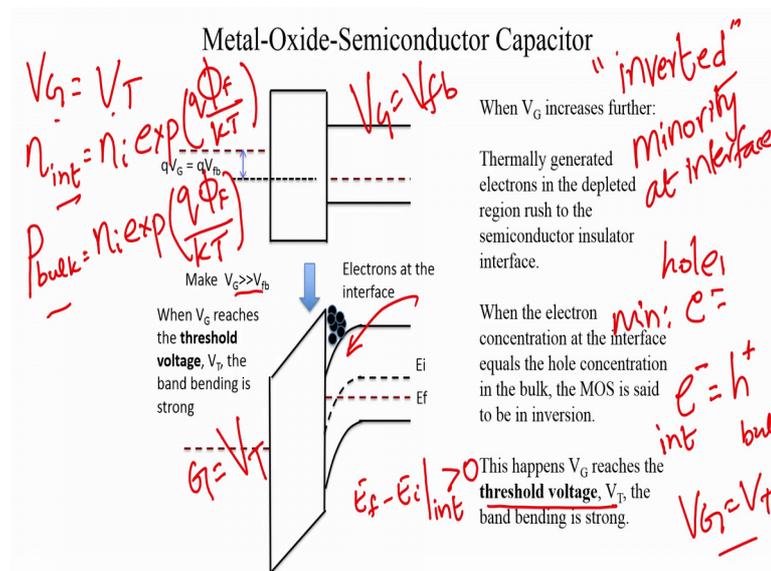
(Refer Slide Time: 35:29)



So, let us say  $E_f$  minus  $E_i$  at the interface is greater than 0, but it is still not equal to  $\phi_F$  you still do have electrons ok and this region is supposed to be you still do have a small number of electrons at the interface ok and how many electrons do we have at the interface? It is quite easy to calculate it is simply  $n_i$  exponential of  $E_f$  minus  $E_i$  by  $K T$ . So, you have that many electrons at the interface. Now how many holes do you have in the bulk ok? So, that is the; so, let me just write this out neatly because it is ok.

So, if you look at the so, let us say  $V_g$  is equal to  $V_T$  ok.

(Refer Slide Time: 36:22)



So, let us say  $V_G$  is equal to  $V_T$  at  $V_g$  equal to  $V_T$  the number of electrons at the interface. So, electrons per unit volume at the interface is  $n_i$  which is the intrinsic carrier concentration into exponential of  $E_f$  minus  $E_i$  ok. So, is going to be basically your  $\phi_F$   $q \phi_F / K T$ . So, that is the number of electrons at the interface the number of electrons per unit volume.

What is the number of holes in the bulk? So,  $P$  in the bulk ok. So, how many holes are present here? It is  $n_i$  exponential of  $q \phi_F / K T$  again because  $E_i$  minus  $E_f$  is  $q \phi_F$  and  $V_G$  equal to  $V_T$  we said that this difference is also  $q \phi_F$  and hence the electron population illness. So, another way of defining threshold voltage is the gate voltage at which the electron concentration at the interface, the electron or the minority carrier concentration at the interface matches the majority carrier concentration in the bulk. So, that is another definition of threshold voltage ok.

So, here we have a p type semiconductor therefore, the majority carriers are the holes the minority carriers are the electrons. So, when the minority carrier concentration is the interface which means the electron concentration at the interface matches the hole concentration in the bulk, then you say that the that  $V_G$  is equal to  $V_T$  ok. I hope this is clear and what we have done now is by making  $V_G$  much greater than  $V_{fb}$  we have brought in electrons at the interface.

So, you look at the previous case. So, here when  $v_g$  was less than  $v_{fb}$  we had holes at the interface and holes are the majority carriers they were accumulated at the interface and by making  $v_g$  much greater than  $v_{fb}$  we have brought in the minority carriers at the interface and therefore, the semiconductor interface semiconductor insulator interface is said to be inverted ok. So, there is a technical term inverted and what this means is, that we have brought the minority carriers of the semiconductor close to the interface. The interface become populated with the minority carriers ok and that is and we say when that happens we say that the semiconductor insulator interfaces inverted or the MOS capacitor is an inversion regime.