Electronics Enclosures Thermal Issues
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Lecture – 12
Combined Rth of devices

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Since an increase in asperity contact reduces the contact resistance, increasing the pressure is often a good way in which to reduce ΔT. In some applications it may be possible to insert a thin foil of a soft, thermally conductive metal in the interface. Table 2.10 shows the results of some researchers' experiments.

TABLE 2.9
Typical Values of the Ratio Y/σ as a Function of the Surface-Finishing Operation

Finishing Operation	Y/σ
Grinding	4.5
Hyperlap	6.5
Sandpaper	7.0
Superfinish	7.0
Lap with loose abrasive	10.0

If you use finishing operations like grinding, seen this know; grinding is what we put it on a grinding wheel. Grinding wheel typically; how grit, which are held by some binding medium, and it will be rotating. So, grinder can rotate here, or know it can rotate here, or you can have something which is the typically a little like the materials used in your car, or for this thing. Next we have as we come down, lot of finishing techniques; saying as we go down know; so we have lapping and so on and so on.

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TABLE 2.10
Thermal Contact Resistances of Various Interfaces

Interface	$\theta \times 10^3$ (m^2 K/W)	Ref.
Silicon chip to lapped aluminum in air (27–500 kN/m^2)	3.0 to 6.0	17
Aluminum to aluminum with indium foil (~100 kN/m^2)	~0.70	18,19
Aluminum to aluminum with lead coating	0.10 to 1.0	20
Aluminum to aluminum with Dow Corning 340 grease (~100 kN/m^2)	~0.70	14,15
Silicon chip to aluminum with 0.02-mm-thick epoxy	2.0 to 9.0	21
Ceramic to ceramic in air	0.50 to 3.0	7
Ceramic to metal in air	1.5 to 8.5	7
Graphite to metal in air	3.0 to 6.0	7
Stainless steel to stainless steel in air	1.7 to 3.7	7
Aluminum to aluminum in air	27.5	22
Aluminum to aluminum in silicone oil	5.25	18
Stainless steel to aluminum in air	3.0 to 4.5	7
Copper to copper in air	10.0 to 25.0	7
Iron to aluminum in air	4.0 to 40.0	7
Brass to brass with 15-μm-thick tin solder coating	0.025 to 0.14	23

A measured values contact resistance of various interfaces have been put here. You seen this last one seem to be most favorable. Brass to brass with 15 micron tin solder coating.

So, the meter square means a total meter square, you know degree Kelvin per watt total amount of area that is in contact. See, this very very small, it is very very, know encouraging thing. And the other extreme, we have this thing saying know; iron to aluminum in air; it just put them both together. Similarly, if you were to bond it even with very thin layer of epoxy; we still have appreciable material here.

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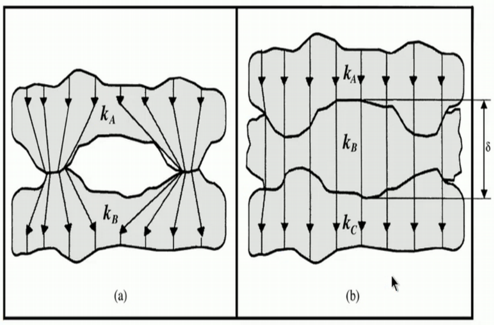

FIGURE 2.24 Heat flow across contacting surfaces: (a) without interstitial material, (b) with interstitial material. The interstitial material greatly increases the contact area available for heat transfer.

Heat flow across the thermal interface is quite complex. Conduction in the interface is parallel and three-dimensional as the heat appears to "squeeze" through the points of contact. Heat flow also occurs by radiation and by conduction through the interface material, which might be air. We can show that convection in the void fluid is insignificant if the Rayleigh number is <1700, which is almost always the case.

So, let me go back to the very first lecture; first point. Heat flow across thermal interfaces is complex conduction in the interface is parallel in 3 dimensional as the heat appears to squeeze through the points of contact. This is what I was telling you. Heat flow occurs by radiation and by conduction through the interface material. Main thing is conduction here, and because this is closed and you have no other thing, little bit of radiation takes place here depending on the differences in temperature. We can show that convection in the void flow is insignificant if the Rayleigh number is less than 1700, means there is no flow which is always the case.

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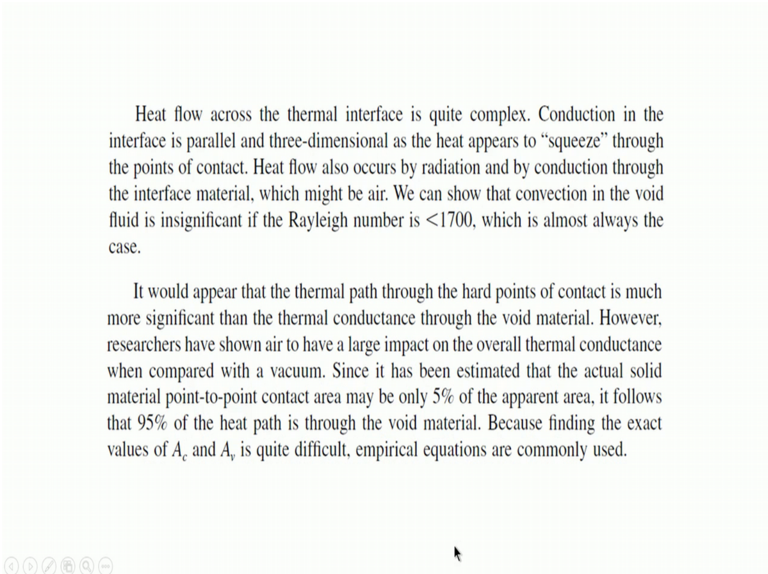

It would appear thermal path through the hard points of contact is much more significant than thermal conductance through the void material. We just said know, if you ignore this convection in the void material means no air can circulate. There almost like closed cells. Researchers shown air to have a large impact on the overall thermal conductance one compared with the vacuum.

Some amount of this thing happens; meaning even small amount of quarter pair will be better than trying to assemble then in a vacuum. We assemble things in a vacuum, or vacuum may not be such a good idea. It may be when we want to preserve food materials, but what assemble two things in vacuum, it does not matter. But then, it does help in trying to push in any other interface material through it. If you want to put a silicone fluid or if you want to put some other thing, which has a higher conductivity may be assembling it in vacuum then releasing the pressure may help. It does; it is done in the case of our things like our transformers which are vacuum impregnated. The impregnation uses vacuum technique. There is not a vacuum inside the atmosphere.

But, what you call the varnish something; which goes into the surfaces in those cases aids directly in the conduction, because it hardens a little and you do not have a air pockets. If you do not impregnate it, chances are air pockets will form they have a tendency to expand in contract, and sometimes undesirable you know things like fungus growth and all can happen; will it grow at that high temperature? I would not know, but it does create voids and then it makes temperature this thing.

So, we have here; it has been estimated that the actual solid material point to point contact area may be 5 percent of the apparent area. 90 percent of the heat path is through the void material because finding the exact values of is quite difficult.

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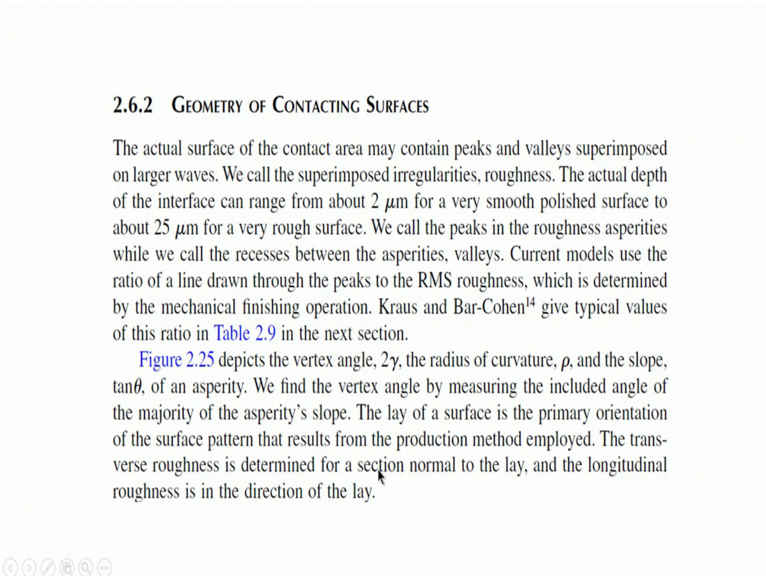
2.6.2 Geometry of Contacting Surfaces

The actual surface of the contact area may contain peaks and valleys superimposed on larger waves. We call the superimposed irregularities, roughness. The actual depth of the interface can range from about 2 μm for a very smooth polished surface to about 25 μm for a very rough surface. We call the peaks in the roughness asperities while we call the recesses between the asperities, valleys. Current models use the ratio of a line drawn through the peaks to the RMS roughness, which is determined by the mechanical finishing operation. Kraus and Bar-Cohen[14] give typical values of this ratio in Table 2.9 in the next section.

Figure 2.25 depicts the vertex angle, 2γ, the radius of curvature, ρ, and the slope, $\tan\theta$, of an asperity. We find the vertex angle by measuring the included angle of the majority of the asperity's slope. The lay of a surface is the primary orientation of the surface pattern that results from the production method employed. The transverse roughness is determined for a section normal to the lay, and the longitudinal roughness is in the direction of the lay.

Empirical equations are quite common. You have seen this; the actual surface of the contact area may contains peaks and valleys superimposed on larger waves;. superimposed irregularities as roughness.

So, we have this; what you call RMS value, must have heard about 3 triangle finish. 1 triangle, 2 triangle is 3 triangle, depending on they use a lapping compound and try to what they call run it against a different surface to contacts, then something settled down;

something is and eventually they have been beautiful contact. Once again you remove that, and then now pack it with heat conducting material or a silicone material, and then if you squeeze it; what was 5 percent can eventually, you know increase to probably 75 to 80 percent, It cannot be made 0 so, but significantly higher. Then after that, next slide also talks you; it is not just about the material, but about this positive curvature and, is there a way of increasing the pressure at the interface.

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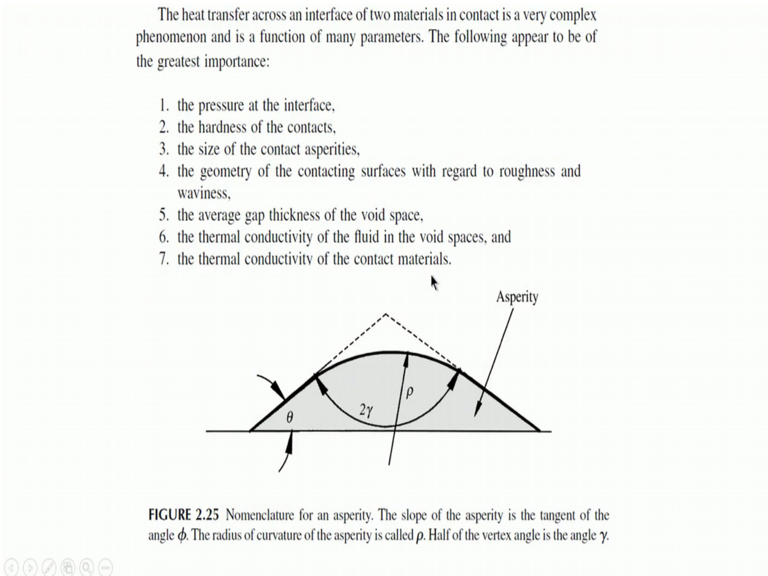

Heat transfer across an interface of two materials is very complex. They appear to be of great importance. You understood know? It is not fully understood except in idealized cases where I know they have actually taken various type of things. One of them is pressure of the interface and hardness of the contact, size of the contact asperities.

So, as you squeeze them more and more, they get flattened out and they meet each other. This positive curvature is very good because it has a tendency to squeeze in. It will happen like, you know when I put both of my hands together can see that it is there. Geometry of the contacts with regard to roughness and waviness, average gap thickness of the void space, thermal conductivity the fluid in the void spaces. Seem that no; it is not air; it could be any conductive fluid and thermal conductivity of the contact materials.

So, if you consider the conductivity of the fluid and the contact materials, they have given here; this is what you call radius of curvature is you know mentioned as rho. Half of the vertex angle is the gamma. So, the next slide which I showed you earlier know gives you list, so many other things.

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2.6.3 Contact Resistance in a Typical Application

Cooper et al.[15] formulated a reasonably useful relationship for the heat transfer interface coefficient, h_i, as

$$h_i = 1.45 \frac{k\left(\frac{P_a}{H}\right)^{0.985}}{\sigma} \tan\phi$$

where:

$k = 2\frac{k_1 k_2}{k_1 + k_2}$ and k_1 and k_2 are the thermal conductivities of material 1 and material 2 (W/m K)

P_a = contact pressure at the thermal interface (N/m^2)

H = hardness of the softer material (N/m^2 × 10^{-8})

$\sigma = \sqrt{\sigma_1^2 + \sigma_2^2}$ and σ_1 and σ_2 are the RMS roughness of material 1 and material 2 (μm)

$\tan\phi = \sqrt{\phi_1^2 + \phi_2^2}$ and ϕ_1 and ϕ_2 are the absolute asperity angles of material 1 and material 2

This correlation shows a good relationship to test data within the following range of applicability:

$$0.35 \times 10^{-3} < \frac{P_a}{H} < 0.01$$
$$13.80 < k < 133.2 \text{ (W/m K)}$$
$$1.0 < \sigma < 85.0\ \mu\text{m}$$
$$0.08 < \tan\phi < 0.160$$

So, typically there are you know, formulations made reasonably useful relationship for the heat transfer interface coefficient tell all these things where; k 1 k 2 are the thermal conductor is a material, contact pressure at the thermal interface that is newtons per meter square, hardness of the softer material. The softer material deforms and flows around the harder material. So, more contact is there. So, both are hard; obviously, none of them give. So, nothing gets formed. That is where, when you have things like copper and aluminum they are generally relatively soft.

So, basic aluminum, if it is not analyzed it is the surface is relatively soft. If you have a hard analytical layer it becomes very very hard. You do analyze it sometimes to get heat stroke electrical conductivity. All analytic layers are electrically non conductive, there insulated. So, we have a problem, once again the because of the direct following of 1, 2, 3. Looking back at these relationships, you see here we have the sigma 1 and sigma 2 square, the R M S is roughness of the material.

So, if you put it on a, what you call; there are machines where measure these things directly, as a small scriber reach a little like you are old vinyl records. So, if you see here, we have grooves; vinyl records usually have grooves. There is the that we call the needle know, needle goes in the grooves. So, if you have these grooves and it will goes in the grooves and then, and the walls of the grooves you have the audio content recorded on that.

So, the what you call; meter loosely I will call it; the roughness meter, also has the same stylus which writes across the surface and then it will directly give you a output, and then it will give you the R M S value also, saying how much of deviations are there more values obviously, this thing. So, we have oh sorry. The asperity angles shows a good relationship to test data within the following range.

So, when I know this pressure by hardness of the material is less than 0 1, and when k is between these values 13 and 133, when the what you call the roughness value is within this and then tan phi is very very shallow.

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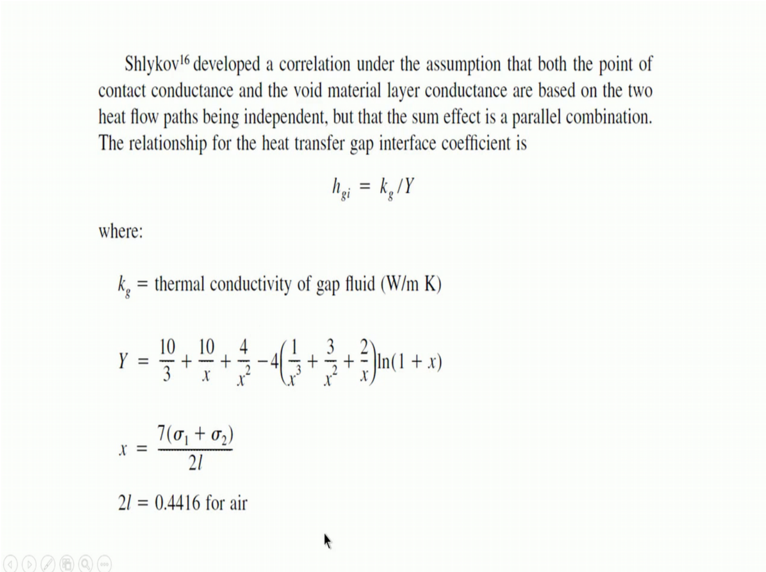

Shlykov[16] developed a correlation under the assumption that both the point of contact conductance and the void material layer conductance are based on the two heat flow paths being independent, but that the sum effect is a parallel combination. The relationship for the heat transfer gap interface coefficient is

$$h_{gi} = k_g / Y$$

where:

k_g = thermal conductivity of gap fluid (W/m K)

$$Y = \frac{10}{3} + \frac{10}{x} + \frac{4}{x^2} - 4\left(\frac{1}{x^3} + \frac{3}{x^2} + \frac{2}{x}\right)\ln(1 + x)$$

$$x = \frac{7(\sigma_1 + \sigma_2)}{2l}$$

$2l$ = 0.4416 for air

Similarly, while this has been made by one sector, they developed a correlation under the assumption that both the point of contact conductance and void material layer are based on the two heat flow of paths being independent, some effect is a parallel combination.

So, they have given all these things saying, thermal conductive the gap fluid and then I mean, it is if you know the values know everything depends on; obviously, what is x and all that is possible for you to determine, but then provided you know all the values. So, Y by gamma is a function, and all these things are already available in case somebody is trying to make a huge; what you call software this thing.

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TYPE	PACKAGE CODE	STYLE LEAD COUNT	THETA JC °C/W	THETA JA °C/W	PIN COMMON TO SUBSTRATE — BOARD TYPE
Metal Can	K	TO-3 2L	3	35	Case
		TO-3 4L	3	35	Case
Metal Can	H	TO-5	40	150	—
		TO-39	15	150	Pin 3*
		TO-46	80	440	Pin 3*
		TO-52	N/A	360	Pin 3*
CERDIP	J	J8	30	110	—

But in reality what we do is, we follow the nearest available values of this directly; degree centigrade per watt for the case as well as if mounted on a standard heat sink.

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Consult individual data sheets for product-specific values or requirements.

1. These values are offered for general reference use.
2. High effective thermal conductivity board (JEDEC 4 layer) was used for the calculations.
3. DFN and QFN package type dimensions are in millimeter.
4. All QFN/QFN are Cu lead frames.
5. The values for Plastic Packages are for copper material and non-fused type unless otherwise shown in STYLE LEAD COUNT column.
6. Construction variations, such as die size, material, leads fused internally to Die Attach Pad, and PCB copper layout, significantly influence thermal performance.
7. For θ jc (Theta JC) calculation on e-pad packages, the heat sink applies to package bottom exposed pad only.
8. Cu = Copper; A42 = Alloy 42.
   * 3-Lead Versions, metal can.

You are seen here, this I think I showed you earlier. Considered, I mean consult individual data sheets for product specific values. Values given by any book are generally for general reference only; not specific. High effective thermal conductivity board was used for the calculations. Understood know? It moves a lot J E D E C 4 layer is was. And then I will avoid this. Then we have copper lead frames. Plastic packages are for copper material and non fused type unless otherwise shown in style, die size material leads internally to die attach pad significantly influence thermal performance. This is where know, it comes to individual data sheets; because individual data sheets after the manufacture; there were taken a relatively large number of samples and view a minimum effective things.

So, if you see any data sheet, you usually have three values one is typical and one is guaranteed minimum and guaranteed maximum. So, we are all familiar with sometimes, what we think is the thing may not be typical value. Best example I can give you is your rechargeable cells. Nicely the number 2500 milliampere hours is written, but that is typical. Guaranteed minimum, most of them are 1800. The best lithium ion cell is probably 1800, but they keep depending on the condition of measurement and rate of for this thing. It is not a directly multiplication of amperes into hours milliampere hours, it is also a lot on the rate.

So, depending on that condition, the 2500 effectively can become on 1800 guaranteed minimum. Sometimes you will be surprised because of you know, effective management you may get little more. Heat sink applies to package bottom, and then they have given some other things. Huge amount of thing, now these days, packages keep improving more and more and more.

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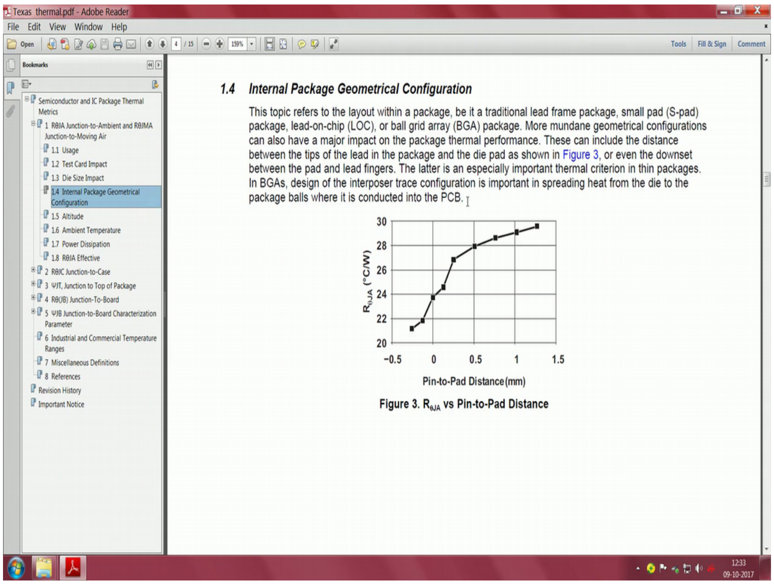

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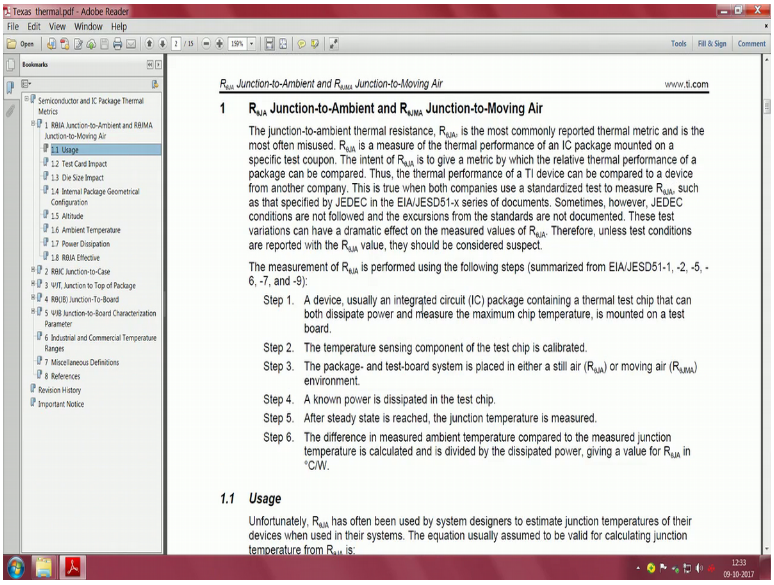

Now, I will try to jump to. Tremendous detail is given here saying where is the; you know, how junction to ambient junction to moving air the calculations have been made. This is directly available to you on the, it has been retrieved; I will say in October 2 0 1 7. So, variants of it will be available. Nothing for you; I mean do not feel lost. If you cannot get this thing at all.

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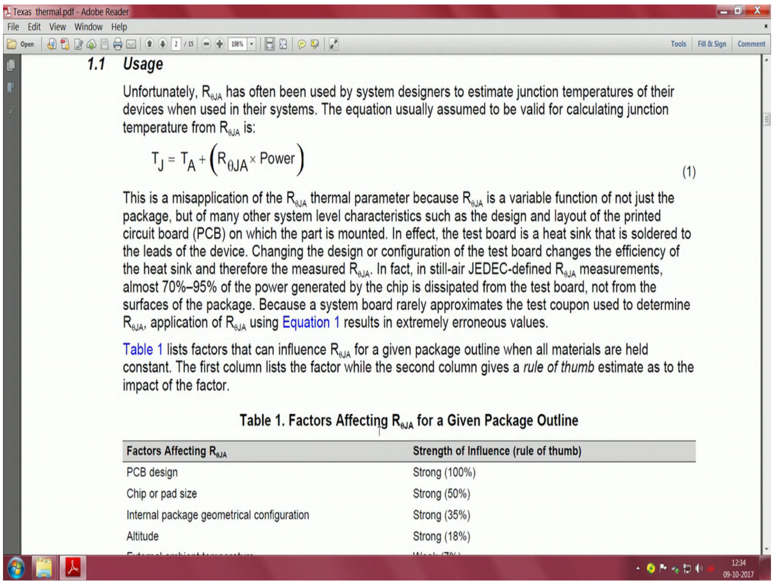

1.1 Usage

Unfortunately, $R_{\theta JA}$ has often been used by system designers to estimate junction temperatures of their devices when used in their systems. The equation usually assumed to be valid for calculating junction temperature from $R_{\theta JA}$ is:

$$T_J = T_A + \left(R_{\theta JA} \times Power\right) \quad (1)$$

This is a misapplication of the $R_{\theta JA}$ thermal parameter because $R_{\theta JA}$ is a variable function of not just the package, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the part is mounted. In effect, the test board is a heat sink that is soldered to the leads of the device. Changing the design or configuration of the test board changes the efficiency of the heat sink and therefore the measured $R_{\theta JA}$. In fact, in still-air JEDEC-defined $R_{\theta JA}$ measurements, almost 70%–95% of the power generated by the chip is dissipated from the test board, not from the surfaces of the package. Because a system board rarely approximates the test coupon used to determine $R_{\theta JA}$, application of $R_{\theta JA}$ using Equation 1 results in extremely erroneous values.

Table 1 lists factors that can influence $R_{\theta JA}$ for a given package outline when all materials are held constant. The first column lists the factor while the second column gives a *rule of thumb* estimate as to the impact of the factor.

Table 1. Factors Affecting $R_{\theta JA}$ for a Given Package Outline

Factors Affecting $R_{\theta JA}$	Strength of Influence (rule of thumb)
PCB design	Strong (100%)
Chip or pad size	Strong (50%)
Internal package geometrical configuration	Strong (35%)
Altitude	Strong (18%)

The equation usually assumes to be valid for calculating junction temperature theta junction to ambient the misapplication, because the variable function of not just the package to do many other system level characteristics, as seen here know. I think, it is you know reasonable.

Now, let me just go back a little. The design and layout of the printed circuit board on which the part is mounted. Test board is a heat sink that is soldered to the leads of the device. Changing the design, test board changes the efficiency of the heat sink and therefore, the measured R J J A. In fact, the still air J E D E C defined measurements is dissipated from the test board.

You seen that know? The issue seems to me that things are dissipated from the test board. You understand know? Even the things which are given by the J E D E C defined are cut it a junction to ambient are not directly the device hanging in air. You to would have noticed it if you are to, what you call test any transistor or any other thing know even a small thing like a diode. The rate of heating becomes tremendous and chances are it will fail. Because the rate of heating is more and the accumulated heat is there.

And then, here where now is, what I would like to point out. System board rarely approximate the test coupon used to determine, so on. So, test coupon is somewhere in the small print, it is given here. While the word infinite is not used, in practically large areas are used. Is where it is said when you go to golden dragon that l e d mounting in all the g d, I think it is by ashram. They just coupon itself who talks about the pattern to be almost 25 m m by 25 m m. And there is a slug in the middle, and then the leads also have a larger pad. While the actual contact pad may 1 m m by 2 m m, or I am sorry; 1 m m by 0.5 m m. It sees a pad which is already 5 m m by maybe 10 m m, and then after that spreading in a triangular way. Same thing would heat in the slug also spreads all the direction.

So, effectively you have almost 25 into 25; 600 to 25 square millimeters of area that is there, as compared to if you are take 2 leads and then connect your, if you try to pass 300 milliamperes at 3.7 volts, it wants stand long. And the way beautiful l e d which is you know, stops giving light.

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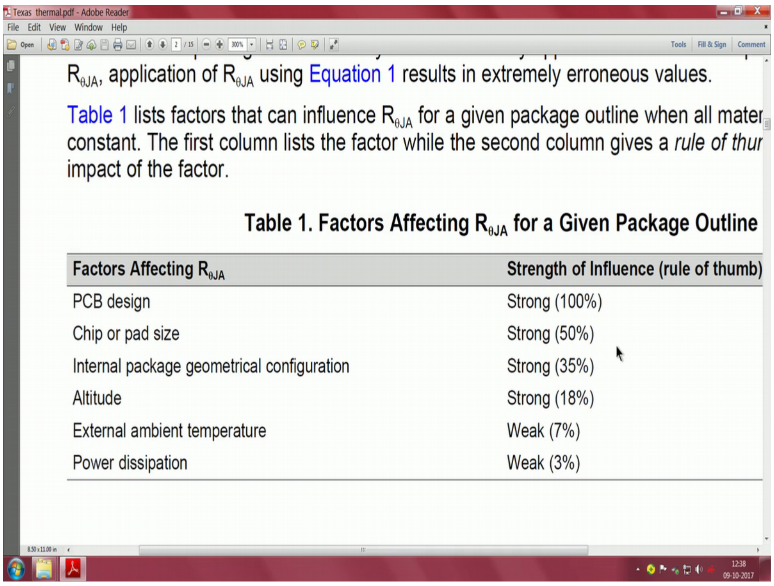
$R_{\theta JA}$, application of $R_{\theta JA}$ using Equation 1 results in extremely erroneous values.

Table 1 lists factors that can influence $R_{\theta JA}$ for a given package outline when all mater constant. The first column lists the factor while the second column gives a *rule of thur* impact of the factor.

Table 1. Factors Affecting $R_{\theta JA}$ for a Given Package Outline

Factors Affecting $R_{\theta JA}$	Strength of Influence (rule of thumb)
PCB design	Strong (100%)
Chip or pad size	Strong (50%)
Internal package geometrical configuration	Strong (35%)
Altitude	Strong (18%)
External ambient temperature	Weak (7%)
Power dissipation	Weak (3%)

If we go down, for a given package outline, it looks like P C B design is the all encompassing thing. Chip or pad size is somewhat partly true, not 100 percent true. But then you cannot ignore it also. Understand know? Chip or pad size is partly true. Internal package geometrical configuration, then the altitude, that is where you know you have the heat carrying capacity of the air. And then ambient temperature and then power dissipation. It seems to be ambient temperature in power dissipation seem to have lesser and lesser effect then the system level P C B design.

So, this is coming from the actual manufacturer, that is Texas. Texas has been in this business for ever as long as it is what I can remember.

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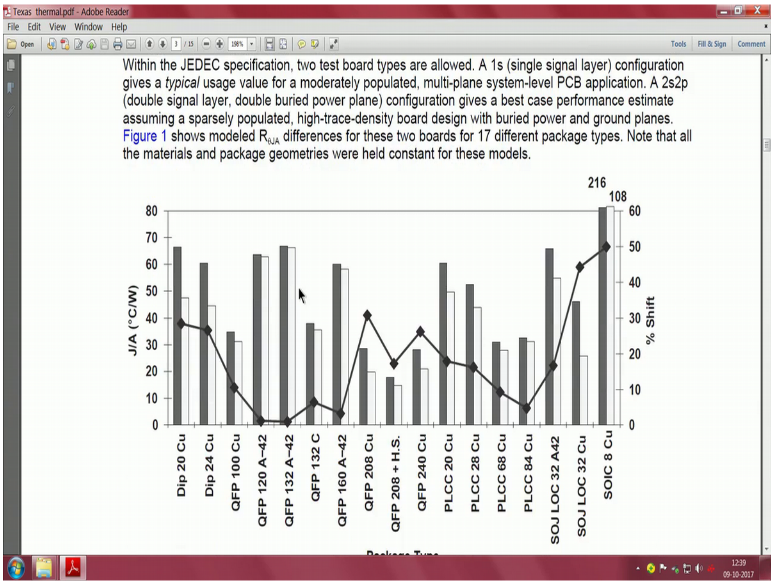

Seen is here; so, many junction to ambient know? So, many types of shifts. So, it is more for you to you know read about it saying we have a die size impact. and then, slowly we come to here.

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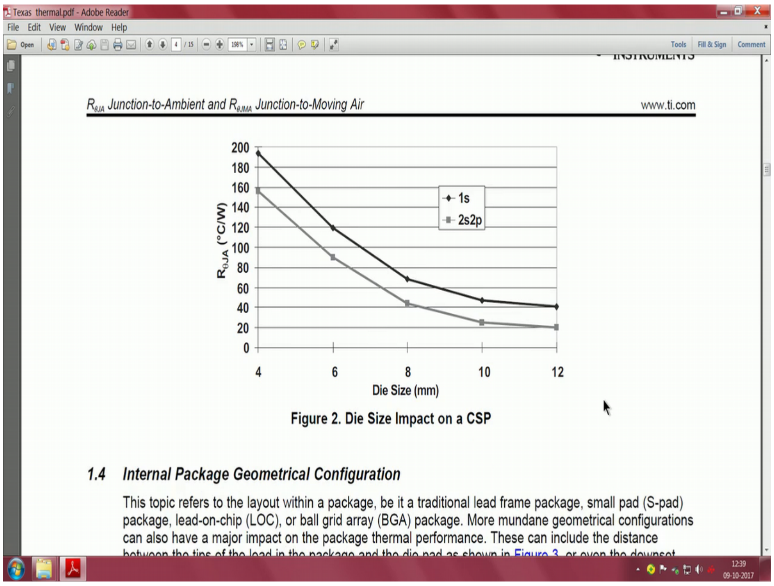

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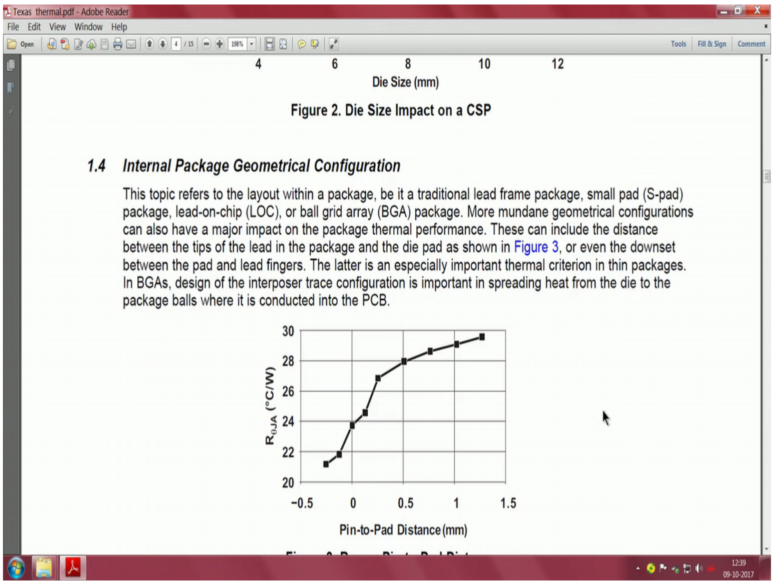

If the die size is small, and geometry configuration saying, pin to pad distances; every known material has been formulated and given here.

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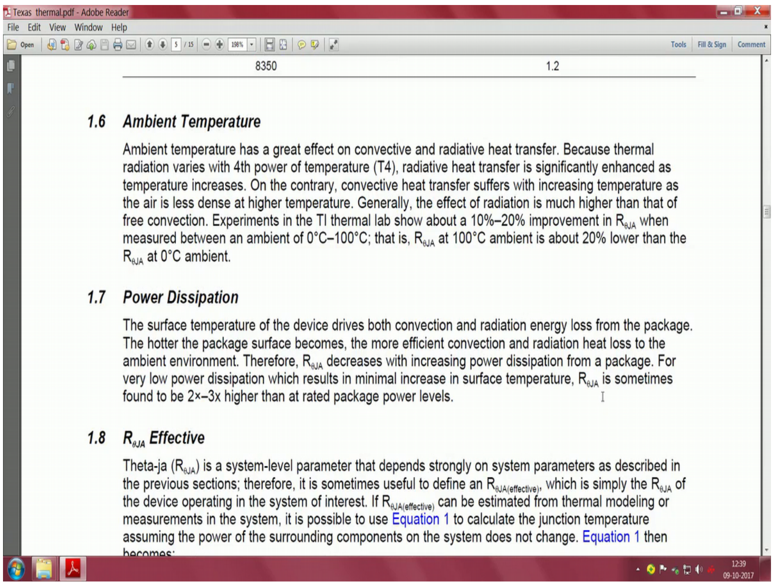

So, easy for you if you can just try to read up these things.

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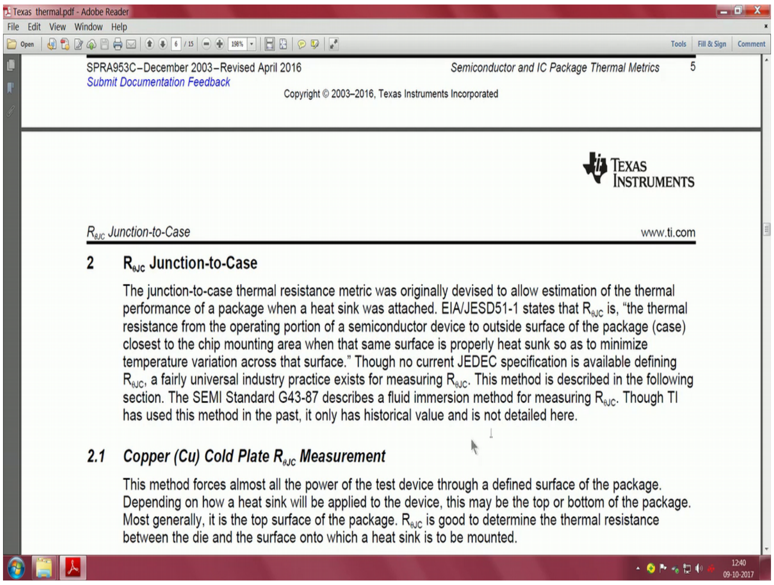

Semiconductor I C and Package Thermal Matrix; we come to junction to case thermal resistance was originally devised to allow estimation of the thermal performance of a package when a heat sink was attached. The, by definition itself, thermal resistance from the operating portion of semiconductor to outside surface of the package closest to the chip mounting area with the same surface is probably heat sunk as to minimize temperature variations across that surface.

So, we have this problem of, even the definition. That is why know, the word top the start with the metric.

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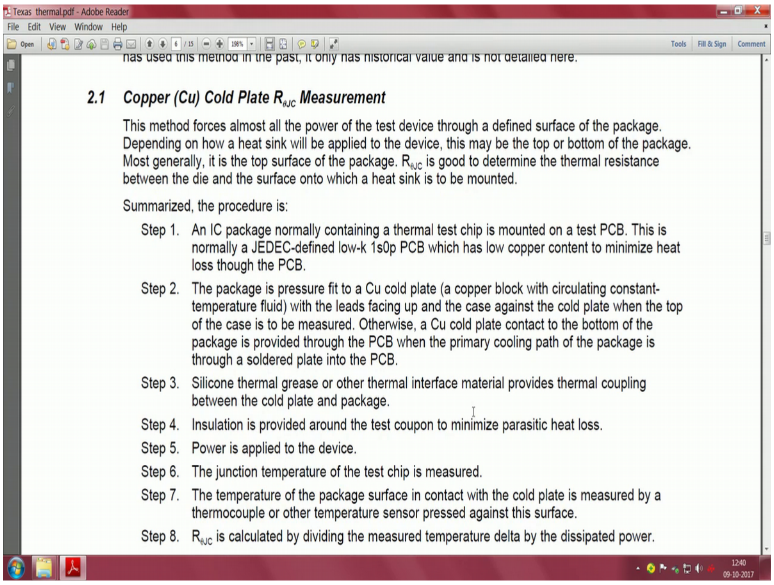

The procedure is, some test chip packages pressure fitted to a copper coal plate; copper block with circulating constant temperature fluid. The next picture is what I have shown you earlier, which will show you how those things are. Silicon thermal grease or other thermal interface material provides coupling between the coal plate and the package. Installation is provided around the test coupon to minimize parasitic heat loss, that is because we are measuring in. So, we have all this here. We have a thermal grease, then we have a test coupon, we have a cold plate.

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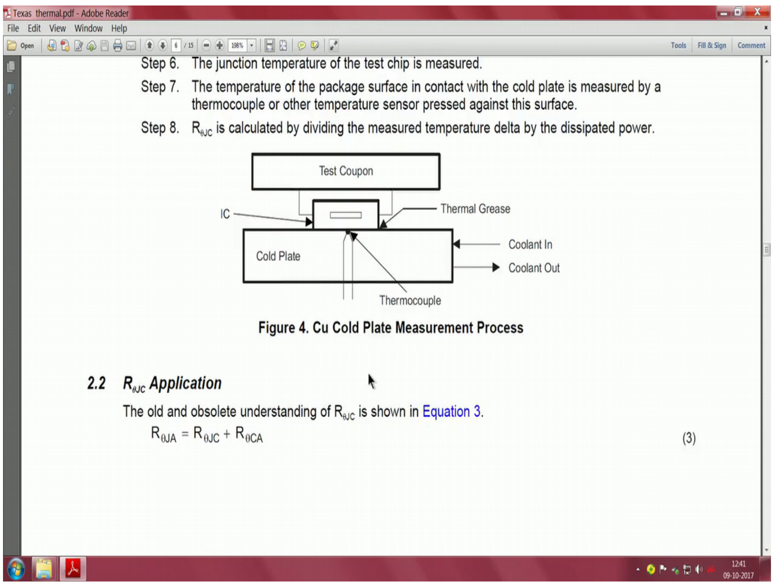

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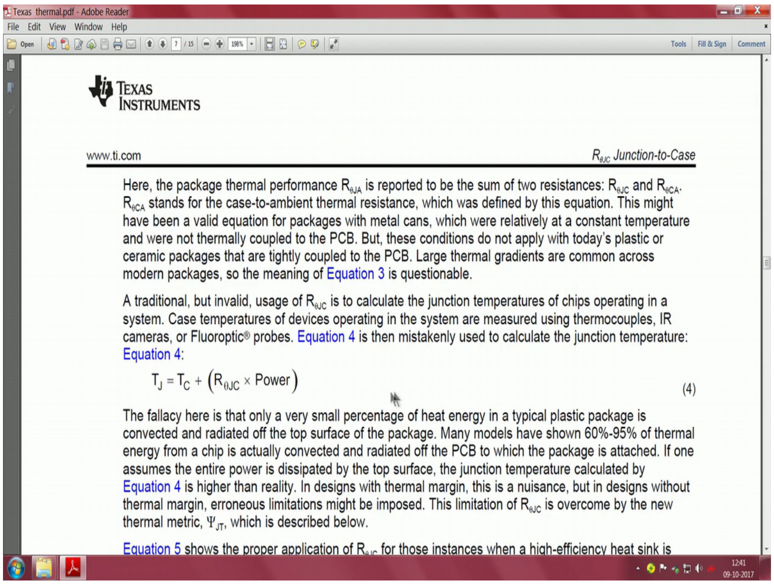

Finally, based on this, traditional, but invalid usage of the junction to case is to calculate the junction temperature of or a chip operating in a system. Devices operating system are measured using thermocouples. I R cameras are something, mistakenly used to calculate the junction temperature like this. You seen this know? This is directly, what you call from the manufacturers.

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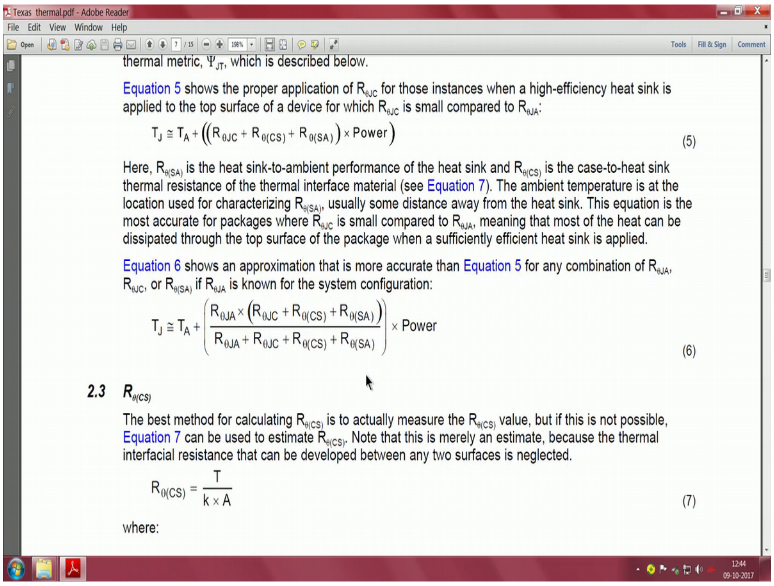

So, I am just quoting it because I was also surprised about saying. The fallacy here is that only a very small percentage of heat energy in a typical plastic package is convicted and radiated off the chip surface. Many models have shown 60 percent to 90 percent from its convicted and radiator of the P C B to which the package is attached. So, in the case of aircraft and such applications, if you have a large P C B; show me this sir. We have a large P C B like this.

You have a lot of components mounted, occasionally on both the directions. Usually they have thick copper area on both sides. Here in here, and probably and both the surface is the whole thing is attached to a case, in which there are grooves. And after it lower it in the grooves, something holds it hard against it. This looks like is a reliable only way of taking away heat.

And, there are metal core P C B. The printed wiring board, instead of using the word P C B, let me now changeover to the other thing. Printed wiring board has metal core on which an insulator is, I do not know how it gets attached to it. Probably there are various methods on it. On top of it you have the conductive thing. So, you have a heat conductive core, and both of it, both sides of it you have the electrically insulated area, which is getting smaller and smaller. What used to be, around, I think 400 500 microns is barely 100 microns now.

And on top of it, you now have one more time, a conductive copper; which is thick. So, you have thick copper, and then very thin, what you call insulating layer and then conductive core. With that, lot of heat transfer takes place directly through the P C B itself. If we can make things like that, it will make life easy for chip mounting technologies here.

So, we have usually, huge this thing. Thickness of interface and so on. So, we have huge amount of what you call, way of calculating and making things.

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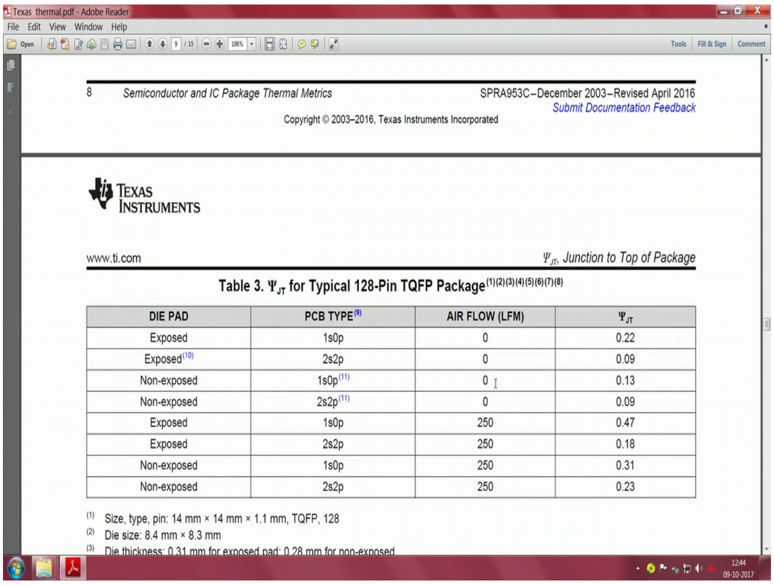

So, depending on the air flow and so on and so on; the measurements are calculated. So, maybe at this point know, I will go back to the old good old thing here.

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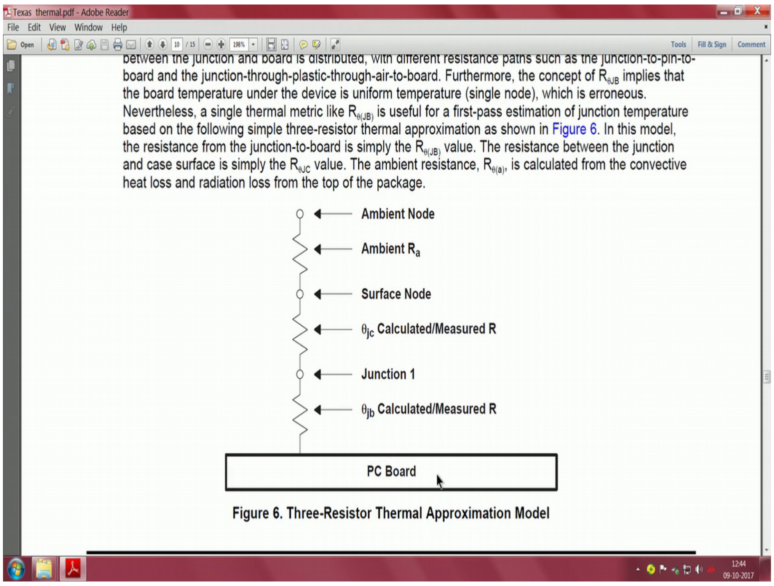

Say I printed that cardboard, then we have all these thermal resistances.

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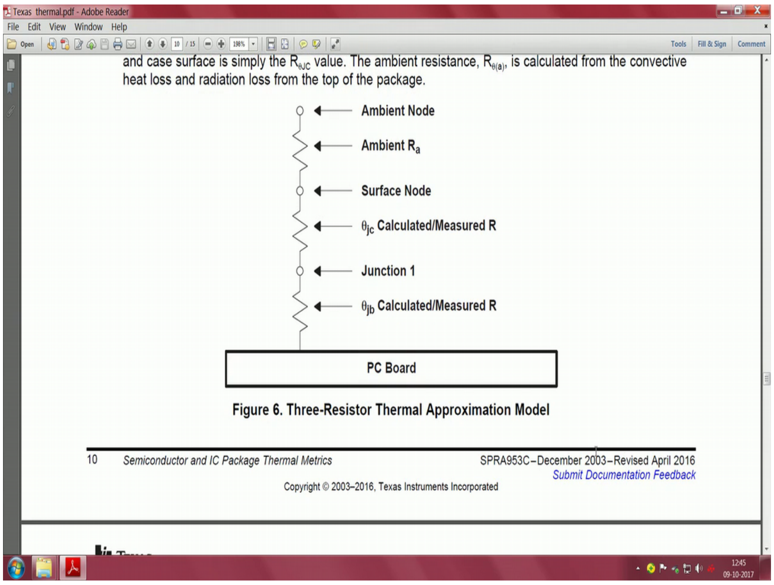

And, this is where why I am stressing on this is though, what is directly quoted on the device like, if you take it T O to 23 package, happily they say internal resistance is so much, from the chip to the surface of the case; that itself usually knows little variation is there. That now has to be mounted on a heat sink or on to the P C B.

So, if you go down, we have all these you know, more and more you know, what you call complicated things. I suggest you read them out yourself.

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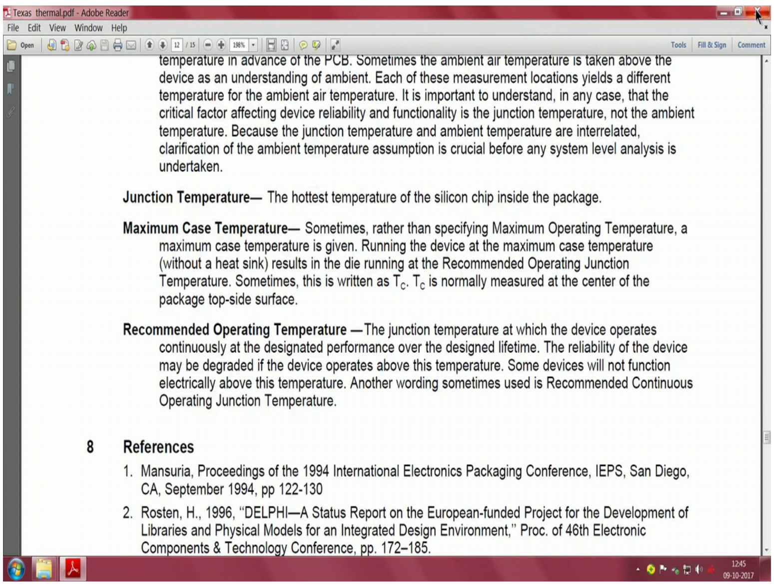

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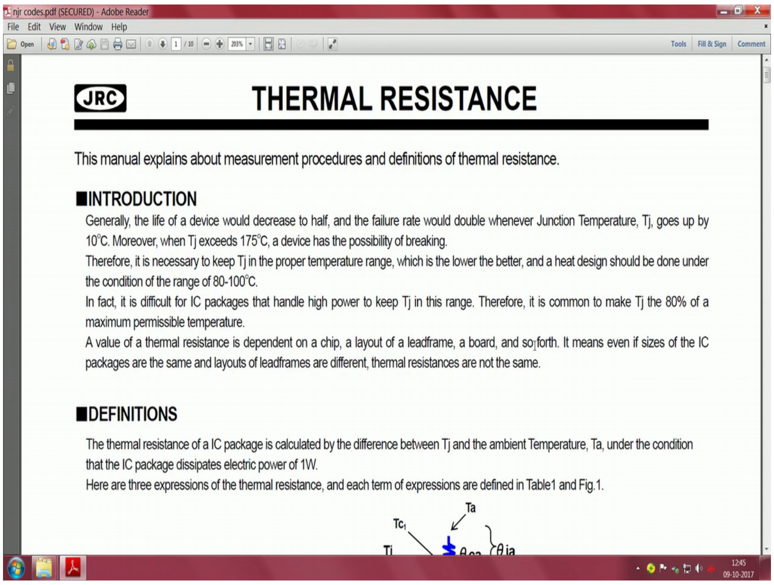

Same thing, this is the good old Japan radio company. Read up what has happened of; how the, what you know R C A victor and all has come. Now this particular thing is called New Japan radio company. They have also given similar things aborted. So, you have what is the thermal resistance and measurement and so on and so on. But in the end, after little while, you will notice that, you have no choice, but to conduct a empirical experiment before you finalize the design.

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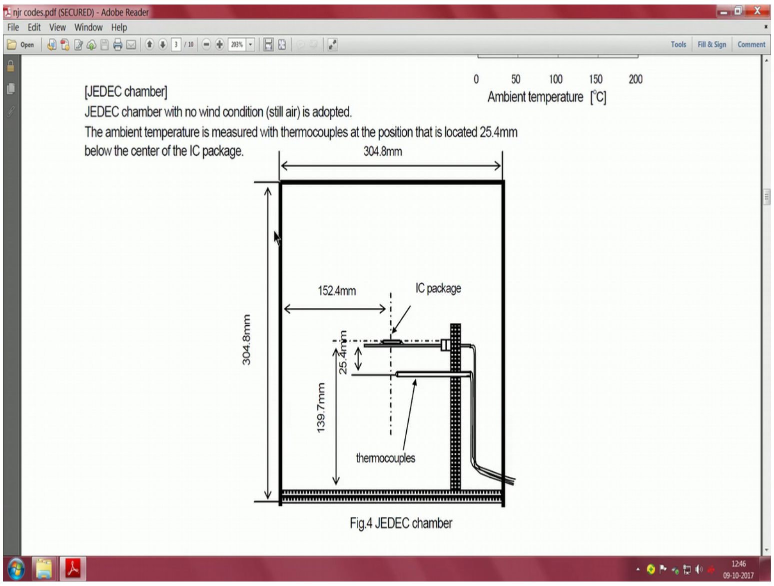

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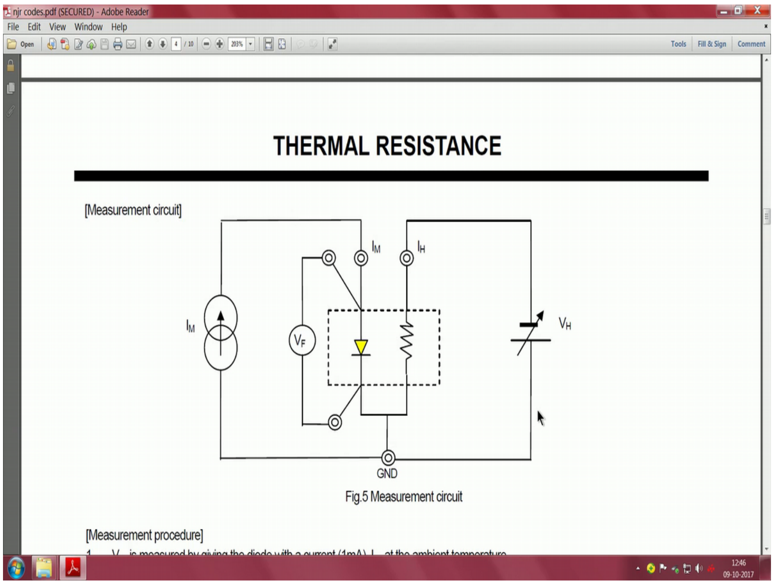

So, we have all these models, and how to circuit, how to make it and how to generate heat in the first instance.

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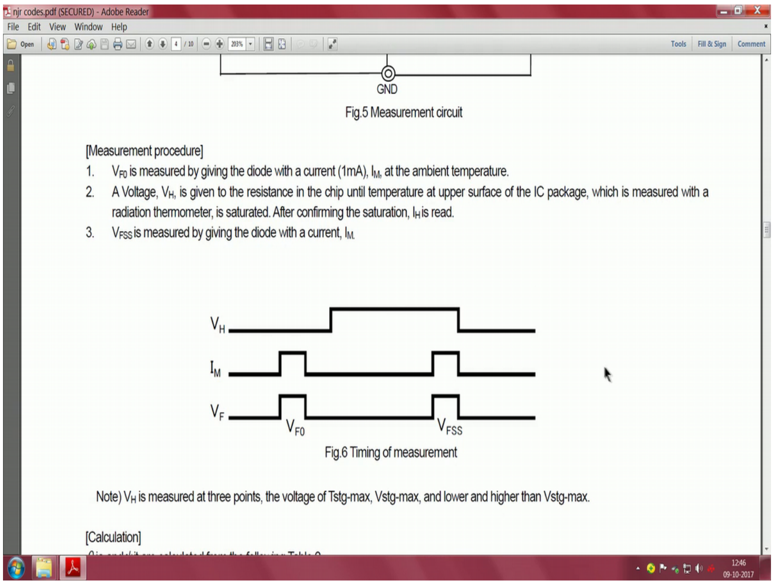

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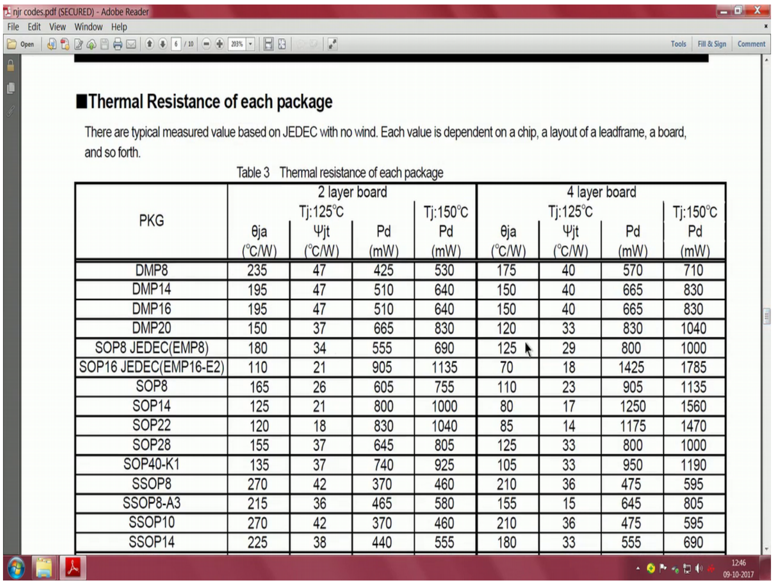

■Thermal Resistance of each package

There are typical measured value based on JEDEC with no wind. Each value is dependent on a chip, a layout of a leadframe, a board, and so forth.

Table 3 Thermal resistance of each package

PKG	2 layer board Tj:125°C θja (°C/W)	2 layer board Tj:125°C Ψjt (°C/W)	2 layer board Tj:125°C Pd (mW)	2 layer board Tj:150°C Pd (mW)	4 layer board Tj:125°C θja (°C/W)	4 layer board Tj:125°C Ψjt (°C/W)	4 layer board Tj:125°C Pd (mW)	4 layer board Tj:150°C Pd (mW)
DMP8	235	47	425	530	175	40	570	710
DMP14	195	47	510	640	150	40	665	830
DMP16	195	47	510	640	150	40	665	830
DMP20	150	37	665	830	120	33	830	1040
SOP8 JEDEC(EMP8)	180	34	555	690	125	29	800	1000
SOP16 JEDEC(EMP16-E2)	110	21	905	1135	70	18	1425	1785
SOP8	165	26	605	755	110	23	905	1135
SOP14	125	21	800	1000	80	17	1250	1560
SOP22	120	18	830	1040	85	14	1175	1470
SOP28	155	37	645	805	125	33	800	1000
SOP40-K1	135	37	740	925	105	33	950	1190
SSOP8	270	42	370	460	210	36	475	595
SSOP8-A3	215	36	465	580	155	15	645	805
SSOP10	270	42	370	460	210	36	475	595
SSOP14	225	38	440	555	180	33	555	690

So, at this point I will. So, we have so many of these things saying, what is the power dissipation on a 2 layer board, 4 layer board, anything you can think of is probably already has been calculated and kept. So, you should be able to search for these things and try to implement then as much as you would like to implement.

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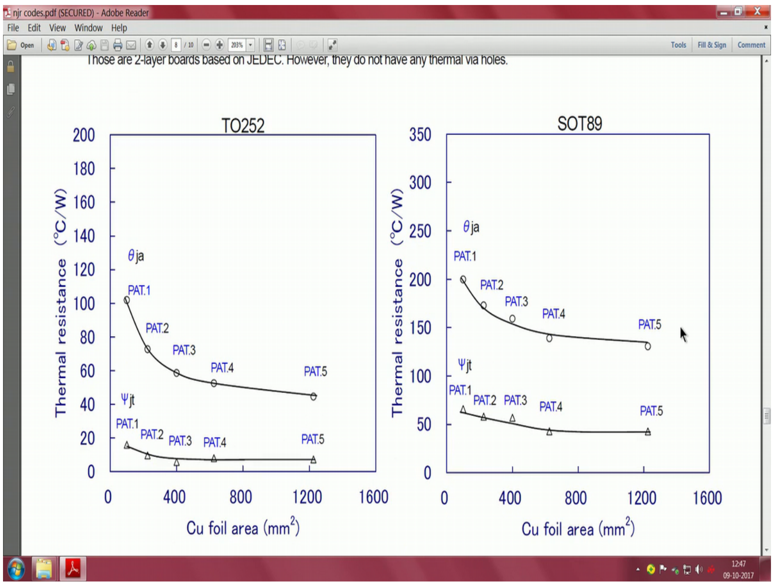

My call also know; locate the retrieve this information directly whenever; see this being recorded in at end of 2017, I expect nothing has really changed in the last 10 years. Maybe the next few more years, these are still valid and then you can start working on it.

So, thank you.