Power Electronics and Distributed Generation
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Lecture - 28
Two leg Single Phase Inverter

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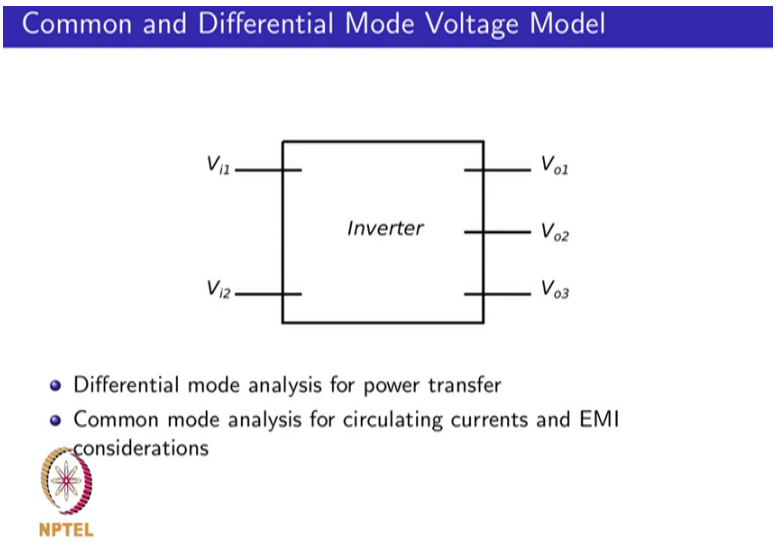

Welcome to class 28 of topics in power electronics and distributed generation. We have been looking at the common mode and differential mode analysis of power converter, and the differential mode signals are quite important, because they are primarily responsible for power transfer. So, the basic purpose for operating the power converter is power transfer. So, the study of the differential mode operation of it is important part. The common mode signals are important, when you are looking at a other perspective, such as circulating possibility for circulating currents in the converter possibility, the EMI characteristics, EMI perspective of the power converter. The other thing we saw in the last class is that the common mode, and differential mode analysis can be performed on a on using both the switching model, and the averaging model, average model. And if you look at single phase inverter.

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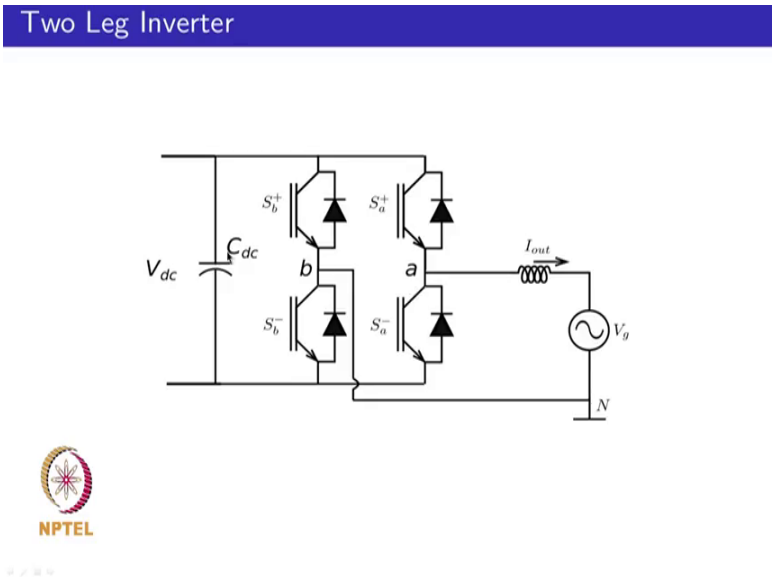

So, this is a single phase 2 leg converter earlier, we had looked at single phase center tap capacitor converter. So, you could look at, it from the common mode and differential mode analysis, and look at what, how these circuits would behave in particular further 2 leg converter. We looked at a modulation method, where you are switching your switching both legs of the power converter, because now you have 2 legs. There are a lot of possibilities for the way in which you could now have p w m on the 2 legs.

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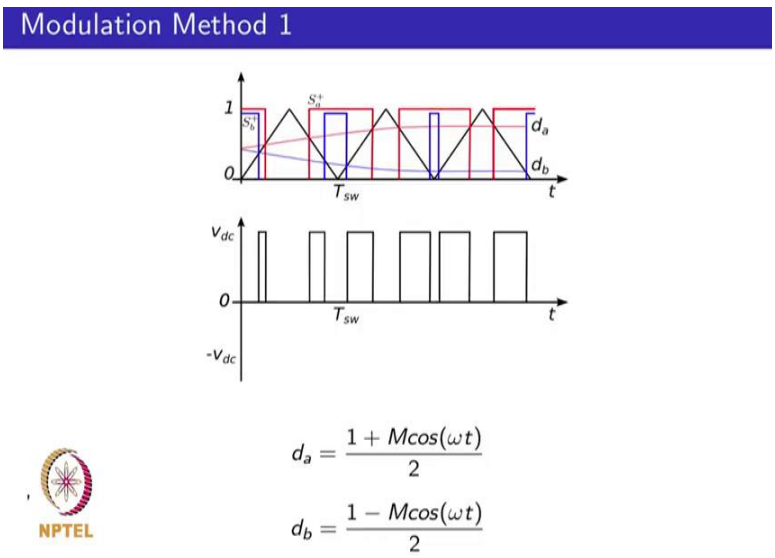

The method that we looked at the modulation method one, where we had a duty cycle for a leg a, and duty cycle for leg b to be symmetric around 0.5. And if you look at the d a and d b, essentially they are symmetric around 0.5, and the characteristics that we saw, is effectively the output frequency is doubled. So, you have two pulses coming in the output for during every switching period, you also have the polarity of the output pulses being in the polarity of the commanded voltage that you would like. So, we called is unique polar modulation, if you have pulses of both polarity coming during the operation that would be a bipolar modulation. We look at couple of other possibilities for the way in which you could modulate the power converter.

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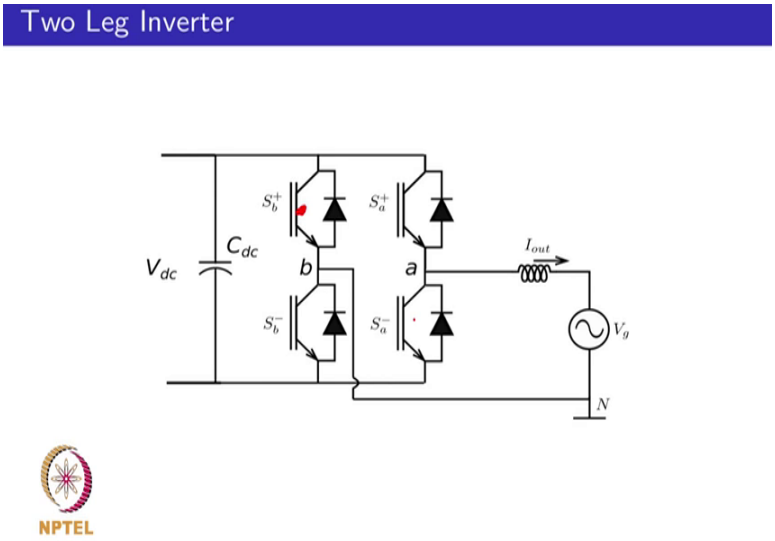

Here, both legs are switching one possible method for modulating. The power converter could be that you could switch say, leg a at high frequencies when you want to get a positive output voltage. You could say, you could, you could turn on say, this particular device. So, if this particular device is on leg b would be connected to the negative d c bus. So, using V d c you could synthesize a positive voltage, if you want to synthesize a negative voltage, you could turn on this particular leg, and switch the leg a, so because now leg b is connected to positive. You have minus V d c and by appropriately switching leg a. You could synthesize a negative polarity output voltage.

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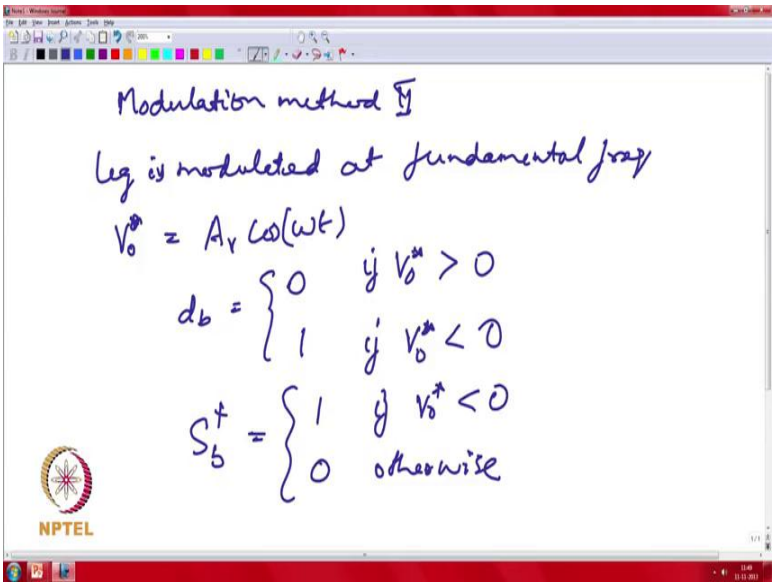

So, you could do this by considering signals. So, will consider a modulation method 2, so if you your leg b is modulated at the fundamental frequency, which is 50 hertz in your case. And if r decide output voltage has a V as of the form A V cos omega t. Then, essentially what you would have is d b could be a signal, which would be 0, if V o star is positive and 1, if V o star is negative. So, if you look at the switching signals, the switching functions for leg by our S b S b plus would be a signal of the form 1, if V o star is less than 0 and 0. Otherwise, so essentially your leg b is switching at fundamental frequency, and leg a is switching at the carryout frequency. So, if you look at the duties cycle signals that are being applied.

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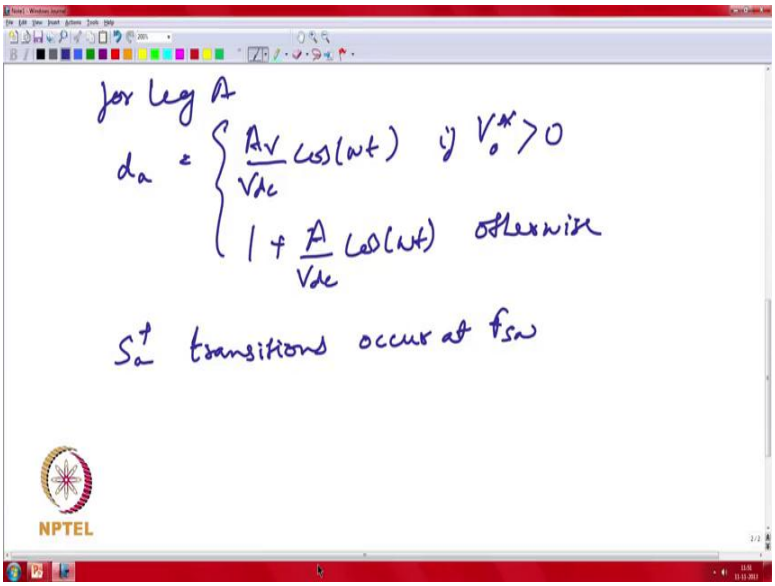

For leg A, We will have d a is equal to, and 1 plus A v by V d c cos omega t. Otherwise, again your leg b, the d b was going between 0 and plus 1 with not taking any values in between, whereas now, d a is having a value, which goes between depending on the polarity of your output voltage that you would like to synthesis takes on signals between, so because your d a's. Now, a continuous a signal between 0 and 1, your S a plus switching formation transitions occur at f s w, if you look at V a b on a differential mode, essentially the output signals will have.

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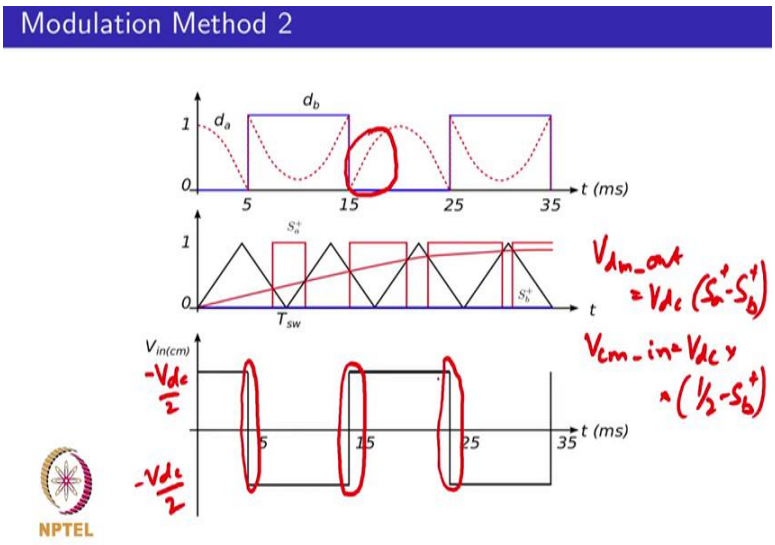

If, you look at your b b, d b is now switching at the fundamental frequency, so this is time in milliseconds. So, it's so one fundamental frequency would correspond to a duration of 20 milliseconds d a, what we had written the expression, would now have a form, which looks like this red dotted line. And the height of this particular d a signal would depend on the amplitude of you are a c signal. That you are trying to synthesis.

So, if you then zoom in to some region of your p w m operation. Say, in this particular between 15 and say 20 milliseconds. You would have wave forms that look like this S b plus is now just staying low, your S a plus would now be switching between plus 0, and plus 1 depending on the amplitude of this d a signal. You can see that your effective output frequency is now f s w. So, you lose the advantage of 2 f s w that you had in the previous modulation case. You have now your effective output switching frequency, which is at f s w rather than 2 f s w, if you.

So, if you can actually write an expression for V differential mode of your output is V d c into S a plus minus S b plus. So, you can see that despites the slightly more complex shape of S a plus and S b plus, your effective output voltage would be the decide sense. So, if you look at your common mode signals that we had we wrote an expression for V common mode of your input, which was V d c in to half minus S b plus. So, you can see that now because your S b plus has a shape, it is 0 in the regions. Say, 0 to 5 seconds, it would be high between 5 and 15, your S b plus function is now switching at the fundamental frequency.

So, if you look at your common mode signal that is coming in your output. You are jumping between plus V d c by 2 and minus V d c by 2 at your fundamental frequency, which is much lower than your switching frequency, which means that your high frequency transition should causes pikes of current to flow into the ground is occurring at a much lower repetition rate. So, your expected problems of E M I that this particular modulation method could be low lower than with the modulation method one that we previously saw discussed. So, it could be easier to build a E M I filter. So, the E M I issues at not just about the topology. Also related to how you are actually conducting the switching operations.

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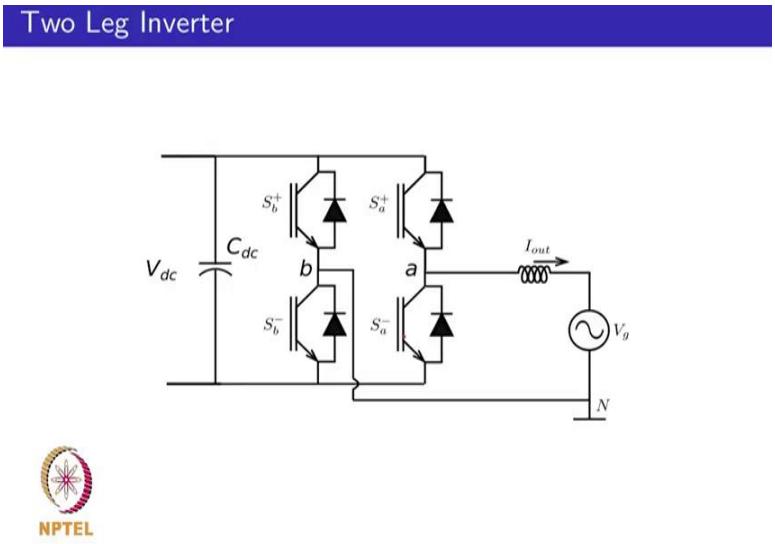

So, if you now you look at the option that we had looked at we are switching leg b at the fundamental frequency, and we switched leg a at high frequency. We could also do take a different alternative approach, where we switch leg b at the switching frequency, and we could switch leg a at the fundamental frequency.

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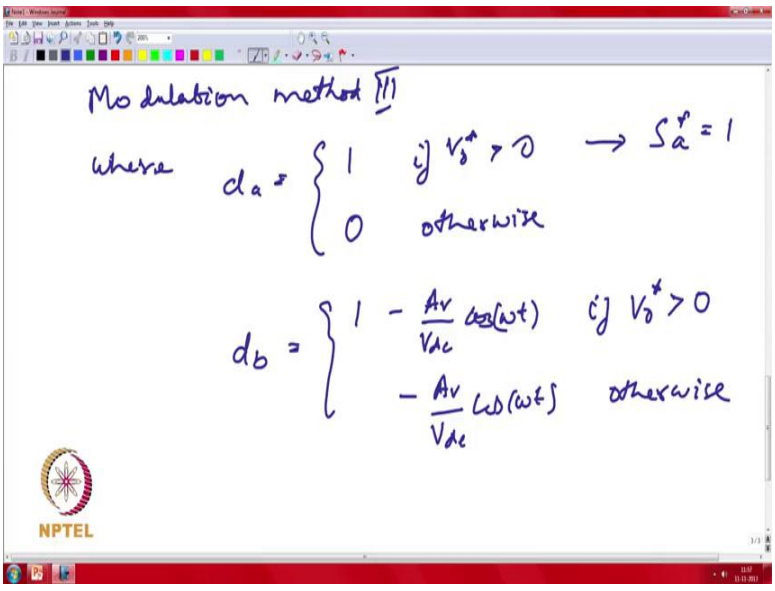

So, we call let modulation method 3, where d a is 1, if V o star is positive. So, this would correspond to S a plus being equal to 1 and 0, otherwise and your d b for the other leg would be 1 minus A v by V d c cos omega t, if V o star positive or minus A v, again you

can see because your o output voltage is V d c into d a minus d b. You get the same differential mode output signal in all the 3 modulation method. So, the differential mode signals would not change, if you look at the shape of the wave forms in the modulation method 3.

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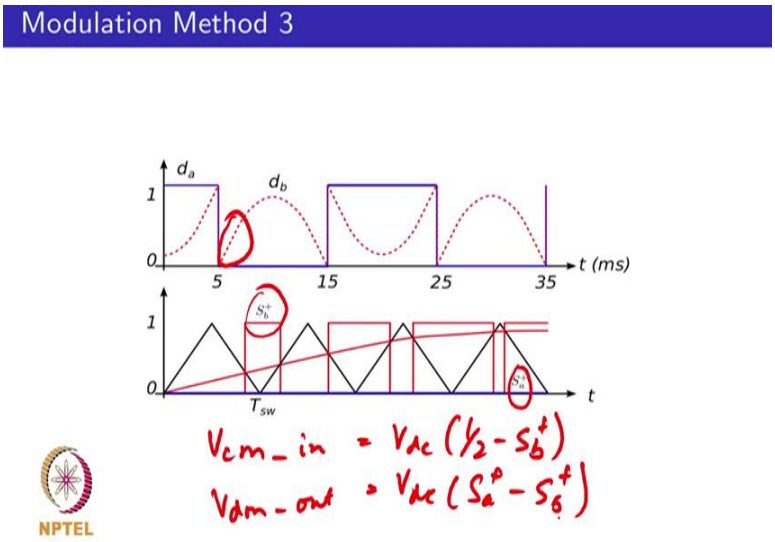

You can see that now d a is switching at the fundamental frequency, and d b a is now having a value, which lies in between 0 and plus 1, which means that d b will be switching at higher frequencies. So, S b plus is the 1, which is switching and say, a plus is now staying at 0. Say, if you are looking at may be a zoomed in region around there it would correspond to wave forms that has been drawn below, if you look at your common mode signal.

In this particular case, we can we have V c m of your input is V d c into half minus S b plus in this case, we can see that the your input would see high frequency on the common mode. So, we have problems with the high frequency on your input side. You also have now only a f s w as your output equivalent switching frequency, which means that we lost the advantage of 2 f s w. So, we can see that this is you your differential mode signals V d m out is to the same V d c into S a plus minus S b plus. So, your output switching frequency is still at f s w.

So, modulation method 3 is poor from both the input and output perspective. So, you by not being careful about which leg you are switching at appropriate rate. You could end

up with beating the problems that you are facing in your power converter without getting any advantage either at the input or at the output.

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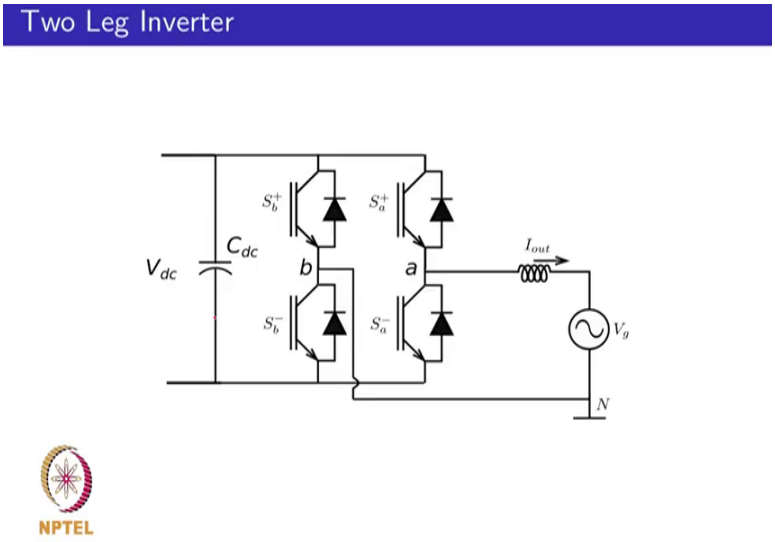

So, one thing that also keep in mind is that we were looking at it at the operation of the power converter from the input and output voltage wave form bases. Another important factor to keep in mind is, how these legs of the power converter would operate on a thermal bases, if you are switching. Say, 1 leg at a S w at the carryout frequency on the other leg at fundamental frequency. It means that 1 leg is having higher losses and the other leg is having lower losses. So, from a thermal loading perspective the temperature rise on 1 leg would be more and the temp compared to the other leg. So, if you are using a h bridge module you may not be fully utilizing your semiconductors.

So, you will have to look at all the factors in mind depending to look at, what are the advantages and disadvantages of one particular topology or one particular method of operating, your switches in a power converter. Now, that we are looked at this 2 leg power converter, we could ask a similar question as we did for our center tapped capacitor topology of, what would be the defined issues behind the d c bus capacitor for this particular topology? How does it compare with the center tapped capacitor topology? So, will look at this design with the same example as what we looked at in for center tapped capacitor.

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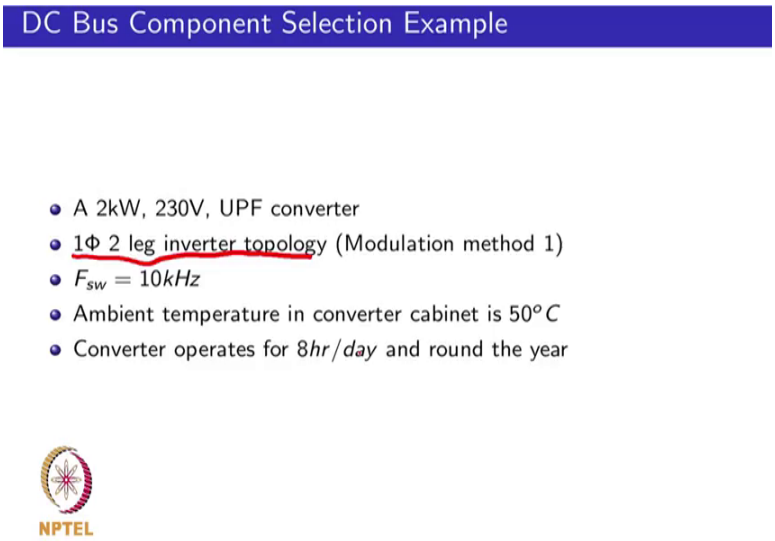

So, we will consider a 2 kilo watt 230 volt unity power factor power converter, but now with a single phase 2 leg inverter topology modulating with method 1. And we will assume that you are your switching frequency is 10 kilo hertz, your carryout frequency is 10 kilo hertz. So, your effective switching frequency seen by a filters would be at 20 kilo hertz the ambient temperature and the operation of the power converter is kept the same.

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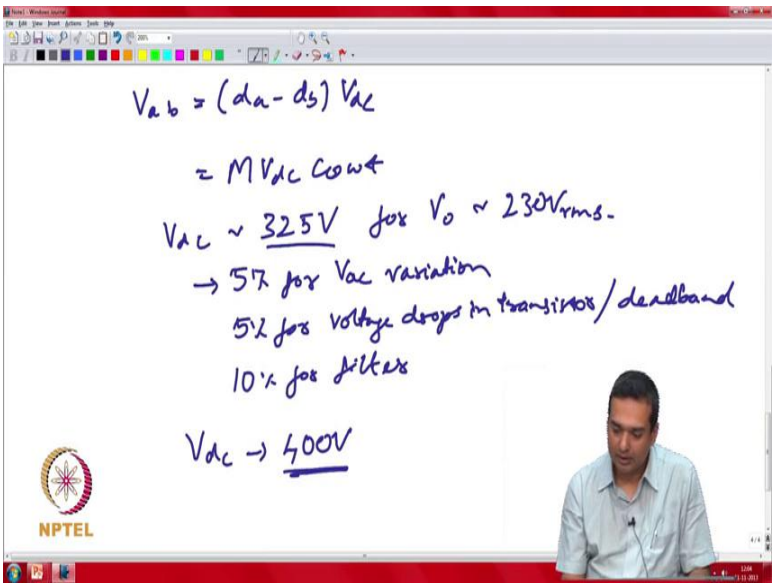

So, we know that from our average model for the power converter V a b is d a minus d b times V d c and d a is half plus M cos omega t by 2 d b s, again symmetric about the 0.5.

So, V a b can be written as m v d c cos omega t, and if we are trying to synthesis a 230 volt a c output. You are talking about V d c of the order of 325 volt for V o is 230 volts r m s. Again we have to consider factors such as the grid voltage variation dead band on state drops in the devices etcetera.

So, will consider 5 percent for V a c variation and dead band effects and 10 percent drop of filtered. So, the actual d c bus voltage that we might need to use would be higher. So, it would be the order of 400 volts rather than 335 volts with ideally, so again for the selection of the capacitors. We are talking about capacitors, which are rated at 4 higher than 400 volts may be 450 volts would be a suitable choice.

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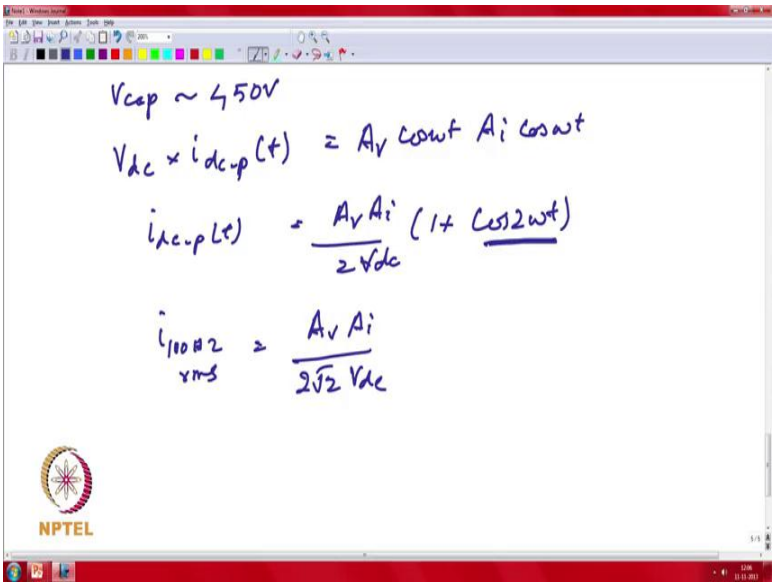

So, we will consider, will so for our analysis we could do a similar analysis for the power converter. We could match the power flow between the input and output of the, of the power converter.

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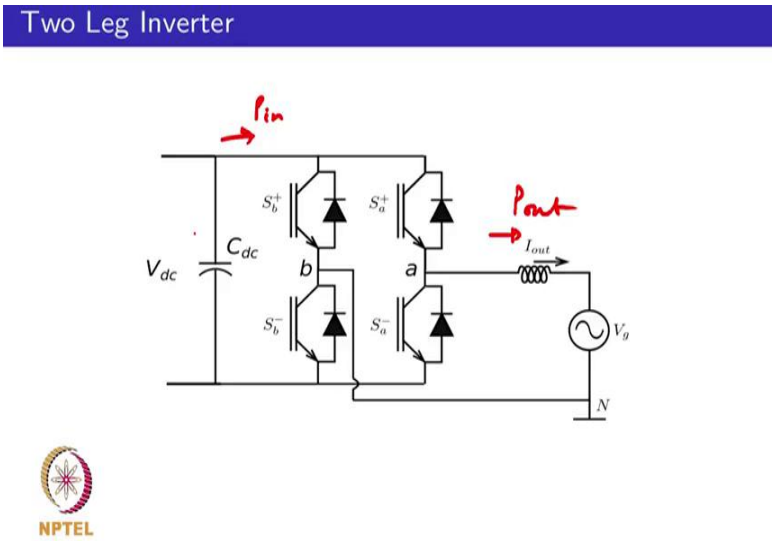

So, if you take a single leg converter, we looked at your p out. And we looked at the power flow into evaluate the d c current and the 100 hertz ripple that would be seen by the d c bus capacitors, we could do a similar analysis to evaluate, what would be the 100 hertz ripple on the d c bus? So, we have V d c times i p of t, which is the positive d c bus current, will call it i d c p?

So, we know you are the a c voltage is 230 volts, we know, the power is 2 kilo watts, so we know, what are a i is? So, you could calculate I d c p. So, the d c current that flows through a, which has a value of a v a i by 2 V d c as there is a 100 hertz components. That is flowing through, which would have a r m s value of a v a I by 2 root 2 V d c. So, the next component that we would, we would like to evaluate for this particular power converter is due to the switching operation, what is the high frequency components that now flow through the d c bus capacitor. And you could evaluate the high frequency components by looking again at the switching functions.

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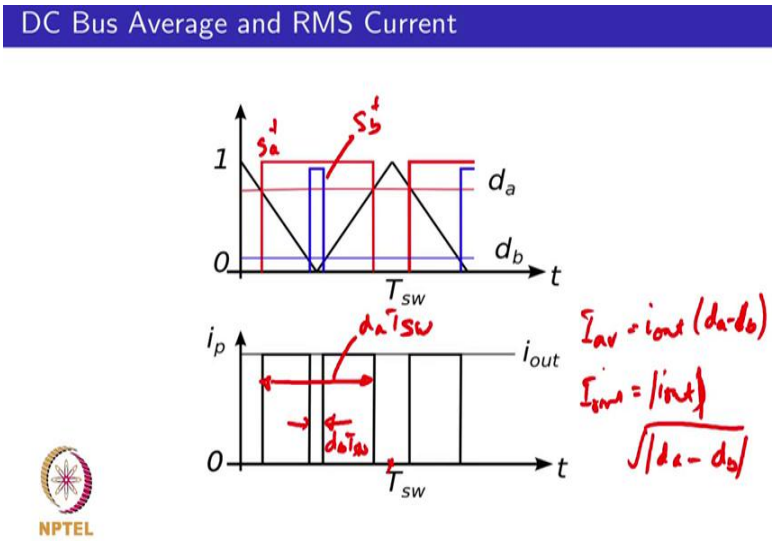

So, if you have S a plus to have a shape such as this and S b plus to have a shape such as this, and you have your i out, when S a plus is wider than S b plus. Then, this particular point this region in between the width of this region would be equal to d a times t s and the width of this particular duration is d b times T s w. Then, you could calculate, what is the average of this particular d c bus positive current, and what is the r m s value? Your average current would then be equal to is i out to d a minus d b again depending on the polarity of diode could be positive or negative. Your r m s quantity on a per switching cycle bases would be magnitude of I out into square root of the magnitude of d a minus d b. So, again this is this gives a r m s value on per switching duration per T s w. You could then submit over all the switching durations in one fundamental cycle.

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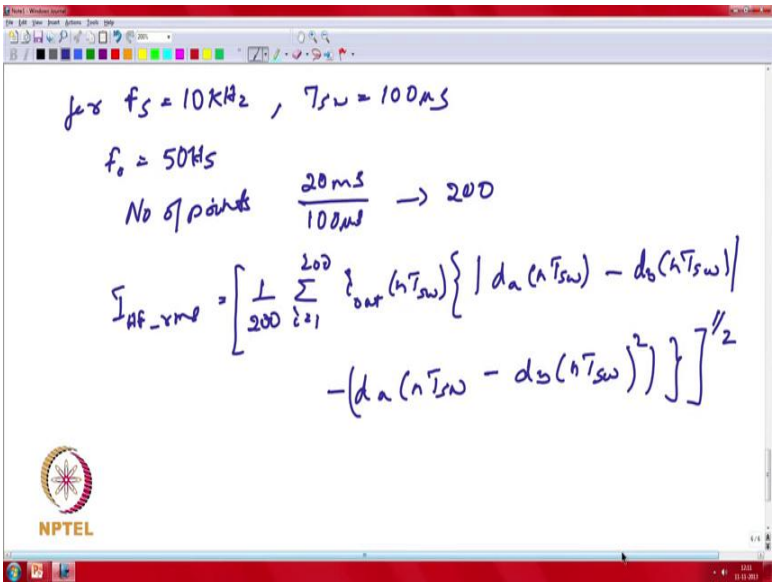

To calculate your high frequency r m s currents or switching frequency of 10 kilo hertz and your T s w is 100 micro seconds, and your fundamental frequency is 50 hertz. So, you have number of points per fundamental is 20 milliseconds by is 100 micro seconds. That is what this would give you 200 points. So, your high frequency current, so this is I out of n T s and the whole thing under square root, will give your r m s currents. So, essentially your summing up the r m s over all the switching T s w's.

So, we could then ask a similar question as what we did for our d c bus capacitor midpoint topology of, what is the r m s current, what would be the voltage ripple? What would be the power dissipation temperature rise the number of capacitors? You need to place in parallel, we could then for the particular, this particular example will consider the same capacitor as what we considered for the, for the previous topology.

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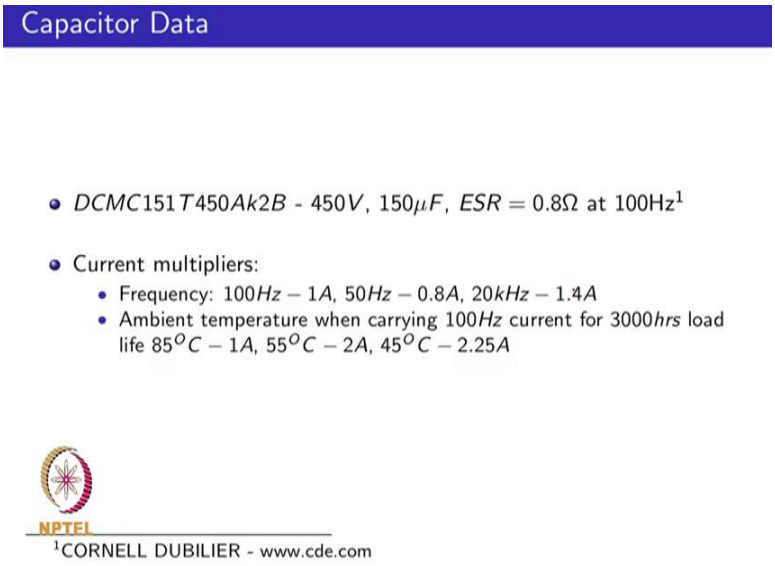

So, we will assume a 450 volt 100 and 50 micro farad capacitor with the given E S R of 0.8 ohms at 100 kilo hertz, will assume the data to be is the same as what we had the previous time, will assume that the high frequency current multiplier is a is 1.4 amps even at 20 kilo hertz. We had taken 1.4 amps at 10 kilo hertz, will assume that it stays flat even at 20 kilo hertz, and the data is same as what we considered for the d c bus capacitor midpoint topology. So, essentially the current multipliers as we saw, give information about the E S R of the capacitor as a function of frequency.

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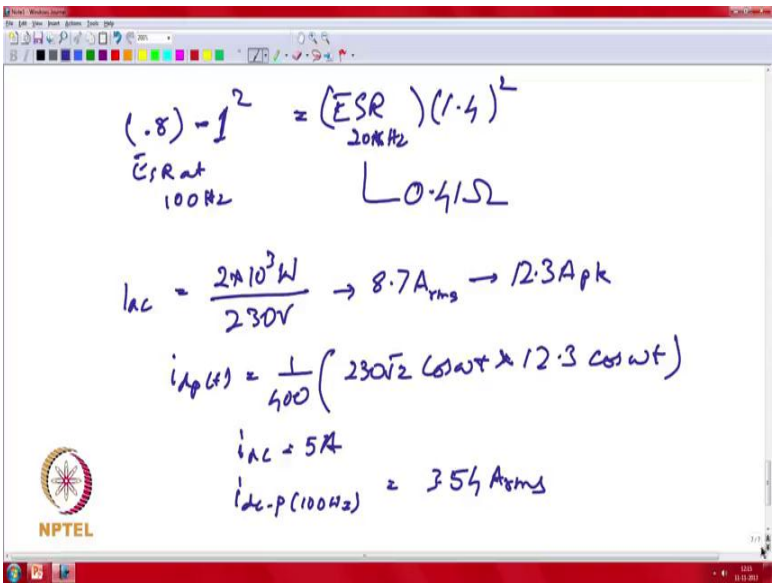

So, if in this particular topology. We know that is 0.8 ohms E S R at 100 hertz and your current at 100 hertz is 1 amp. So, I square r is 1 square into 0.8. So, the E S R at 20 kilo hertz into 1.4 amp square 1 would be able to calculate. The E S R, which, so this turns out to have a value of 0.41 ohms, so for this particular power converter, it is 2 kilo watts 230 volts. So, your current rating I a c is 2 kilo watts 230 volts.

So, this corresponds to 8.7 amps r m. So, r 12.3 amps peak in this topology because the output is not connected to the capacitor through any midpoints. There will be no 50 hertz component, so the low frequency component is the 100 hertz component. So, you are I d c p of t is now 1 by 400, which is your d c bus voltage into 230 root 2 cos omega t into 12.3, which is a current cos omega t assuming unity power factor operation. So, you are i d c average d c current is 5 amps and you are i d c p at 100 hertz is 5 amps peak, which would correspond to 3.54 amps r m s.

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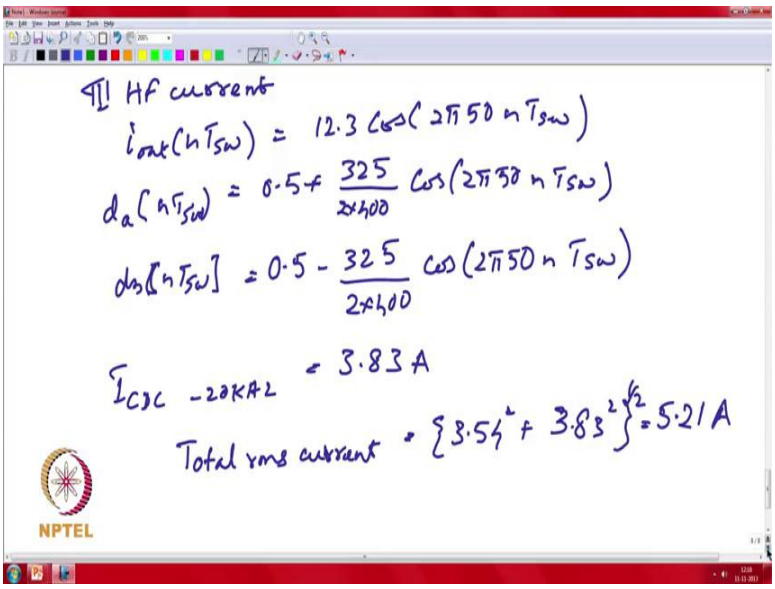

So, to evaluate your high frequency component of the current we will, we can Calculate it in similar manner as what we have just discussed. We know, our I out of at n T s w is 12.3 cos, and we are using modulation method 1. So, d a of n t s is .5 plus your output voltage is having a peak value of 230 root 2. So, this is 325, so you have your duty cycles and your currents based on which you could now calculate, what is your high frequency current flowing in your d c bus? At that current now would be two pulses per

T s w. So, you are having your d c bus current, now at 20 kilo hertz and its side bans and harmonics.

So, based on the expression that we had just written previously could calculate, you are I c d c at 20 kilo hertz is 3.83 amps. So, if you look at your total r m s current flowing through the capacitor, it would now be your 100 hertz component plus your 20 kilo hertz component. So, you have about 5.2 amps flowing through the d c bus capacitor. So, a single capacitor would obviously not be sufficient, and will have to connect multiple capacitors in parallel.

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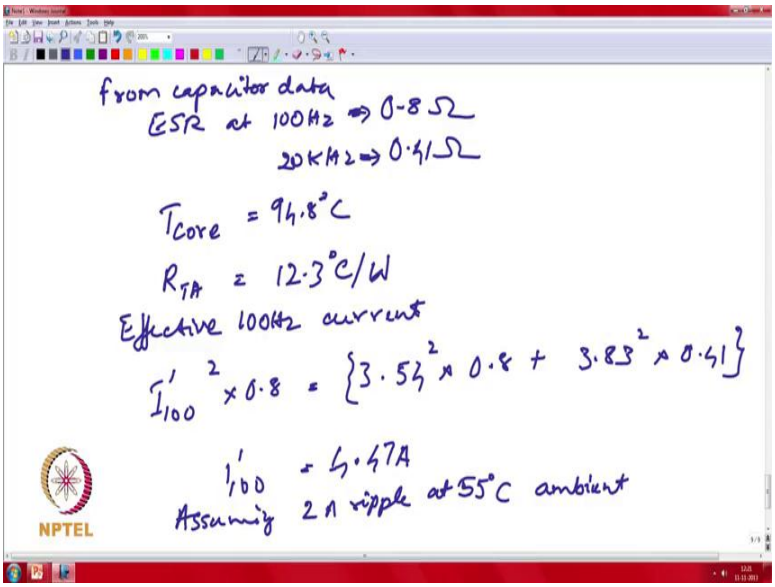

So, if you look at the E S R numbers, the E S R at 100 hertz and at 20 kilo hertz is 0.41 ohms. And based on the calculations from our previous example we saw that the cap capacitor, which was fight for 3000 hours of life would correspond to a core temperature core of 90.8 degree centigrade. And it had thermal impedance from core to ambient of 12.3 degree centigrade per watt.

So, this is from the previous example, so using this E S R numbers we could calculate, what is the effective 100 hertz current that is flowing through the capacitors o effective 100 hertz current? So, 3.54 is the 100 hertz ripple plus 3.83 is the switching frequency ripple. So, you are I 100 is 4.47 amps, so from a thermal perspective, we had seen again from the data sheet that if we have about 2 amps per capacitor. And it's operating at an ambient of 55 degree centigrade, you can expect about 3000 hours of life. So, if we can

make use of this number by taking the 2 amps per capacitor as the as a design guideline we would need, we need.

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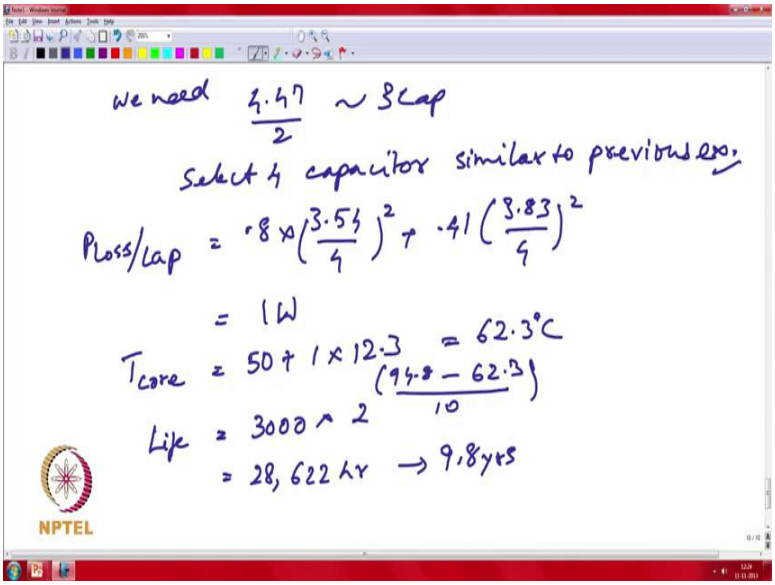

So, you are talking about roughly 3 capacitors. So, last time we did in the previous example in analysis with both 3 and 4 capacitors will consider. Say, for 4 capacitors in this case as being used in the design, so select 4 capacitors example. So, if we could then calculate the power loss per capacitor, so this is 0.8 into. So, it is about 1 watt loss per capacitor, so 4 capacitors in parallel. We are talking about 4 watts loss in the bank your core temperature for the capacitor is 50 into 50 plus 50 is the ambient within the cabinet plus 1 watt loss per capacitor into 12.3, which is the thermal impedance in degrees per watt.

So, you have a core temperature of 62.3 degrees centigrade and again assuming, the simple the r mal lifetime model. You are considering 3000 into, so you are talking about 9.8 years compared to about 4 and half years. For the other in the previous example, we could also calculate the voltage ripple.

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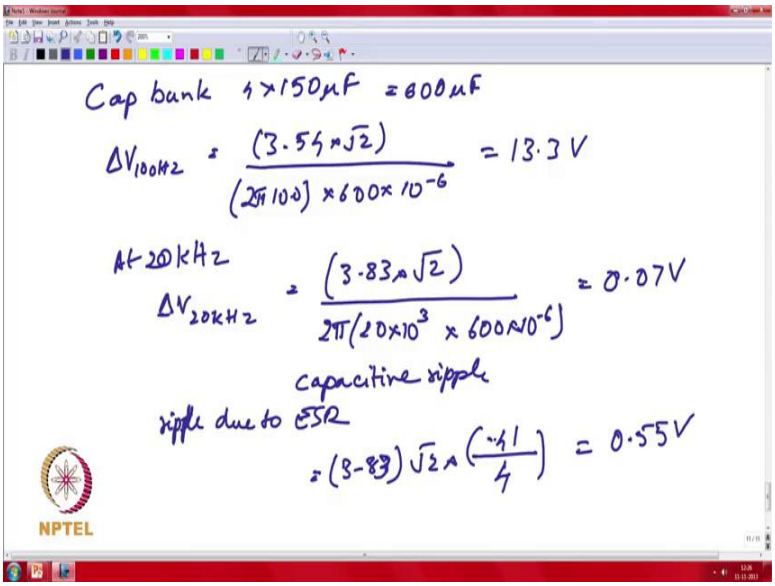

So, your capacitor bank is 4 capacitor sin parallel 150 micro farads. So, this is 600 micro farads. So, your 100 hertz ripple is, so we have about 13.3 volts as your 100 hertz ripple, and then you could look at what is ripple at 20 kilo hertz. So, we had 3.83 amps again will assume that this, it's actually square pulses, but assuming it is sinusoid. You will have 3.3 times root 2. These are all simplifications to get in estimate of what the ripple. So, it is about 70 mille volts, it's almost negligible that rippled at 20 kilo hertz.

It was a capacitive ripple, if you look at the rippled because of the E S R. We are talking about 3.83 root 2 into 0.41 is the E S R at 20 kilo hertz, and the 4 capacitors in parallel. So, we are talking about 0.55 volts. So, you can see at the switching frequency, your capacitor bank is now acting more resistive than capacitive. So, you have the same concerns that you have had in the previous topology, you need to, if you have stay inductances you need. You will have stay inductances and you need to puts rubber capacitors film capacitors in parallel. So, at account for the rapid transitions that would be there in the current wave forms due to the switching of the transistors.

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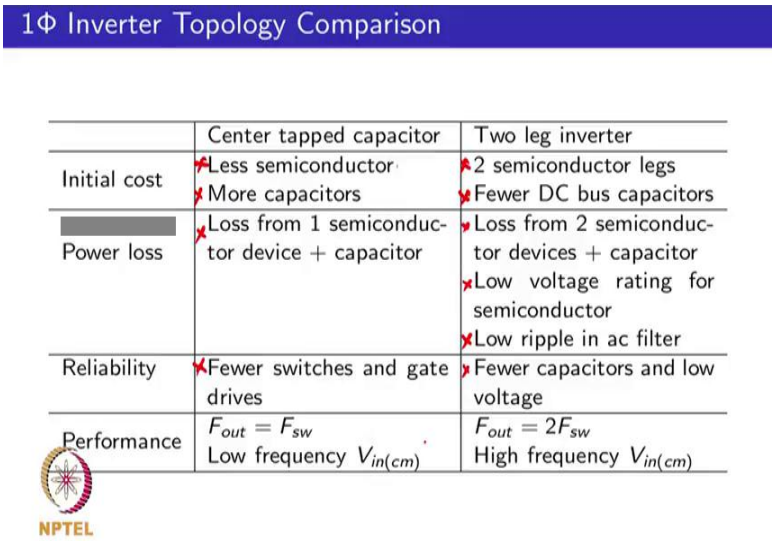

So, we could look at then a comparison of the 2 leg inverter topology with the center tapped capacitor topology. And if you look at the center tapped capacitor topology one thing is you need lesser semiconductor because you have only 1 leg, where as in the 2 leg case you would have 2 legs. So, you have an additional leg semiconductor to consider, but one thing is the semiconductors are rated in this particular case for 1200 volts. And the other case semiconductors might be rated for 600 volts.

So, the voltage rating is not identical in the center tapped case, you have more capacitors that you would need in your capacitor bank. So, depending on the cost of your capacitors versus cost of a additional leg of a semiconductor, you would have different initial cost. In this particular case you have fewer d c bus capacitors, but it is not just the semiconductor leg.

You need to consider, you need to also consider gear drives etcetera that you need for the leg, if you look at the path for the current flow in the center tapped topology. Your current would be flowing through one semiconductor device transistor or a diode, then the written path is so the capacitor. So, you have losses due to the drops in those paths, which could be the conduction drop and the drops in the E S R of the capacitor whereas, if you look at the losses in the case of 2 leg converter you have the drops in 2 semiconductor devices, and the capacitors.

So, you will have to look at from a overall perspective whether the losses would be more in one case or the other it depends to a large extent on, how much more dominant the capacitor E S R values are compared to the on state drops of semiconductor devices. However, the low voltage rating of the semiconductors mean that the semiconductor drops over here would not be identical to the semiconductor drops over in the center tapped topology, if you take a semiconductor device, when you go up in voltage rating the on state resistance will go up for a given current levels. So, a 1200 volt device would have a higher r conduction compared to a 600 volt device.

You can also consider the effect of, say in modulation method; one we saw that the effective output frequency is twice the switching frequency. So, your ripple current in the output filter would be lower because of the higher equivalent frequency, which means that potentially. You could look at, whether there is some energy savings, because of reduced ripple current in your output filter our reliability perspective.

The center tapped topology has fewer semiconductor switches and gate drives. So, if your reliability issues are more semiconductor devices the none with fewer devices would be of advantage whereas, the 2 leg capacitor, 2 leg inverter has fewer capacitors. And the voltage rating is reduced, so your clearance requirement etcetera is actually reduced, so depending on again, which is the item of concern. You have different reliability implications of these 2 topologies also other factors performance factors. We also, we saw that in one case, you have bipolar p w m in 1 k g, you have uni-polar p w m also the switching frequency is effectively doubled in modulation method; one we also saw that in the center tapped topology.

You have low frequency all d c, essentially d c in your input common mode voltage, where a sin modulation method; one we saw that there is high frequency in the common mode input. So, you might need more E M I filtering, so you could actually won a overall system bases look at, what it takes to actually do a comparison. Now, we have looked at essentially single phase two options for single phase power conversion, but we could see that even in this simple example, we could do a very exhaustive analysis of what the implications of each design choice is…

So, to take this further we more detail analysis, we need to actually look at what the implications are, when you are looking at it closely from a semiconductor perspective, and also from a c filter design perspective, which we will discuss later.

Thank you.