An Introduction to Electronics Systems Packaging

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Module No. 05

Lecture No. 22

Demo and examples of layout and routing

Technology file generation from CAD

DFM check list and design rules

Design for Reliability

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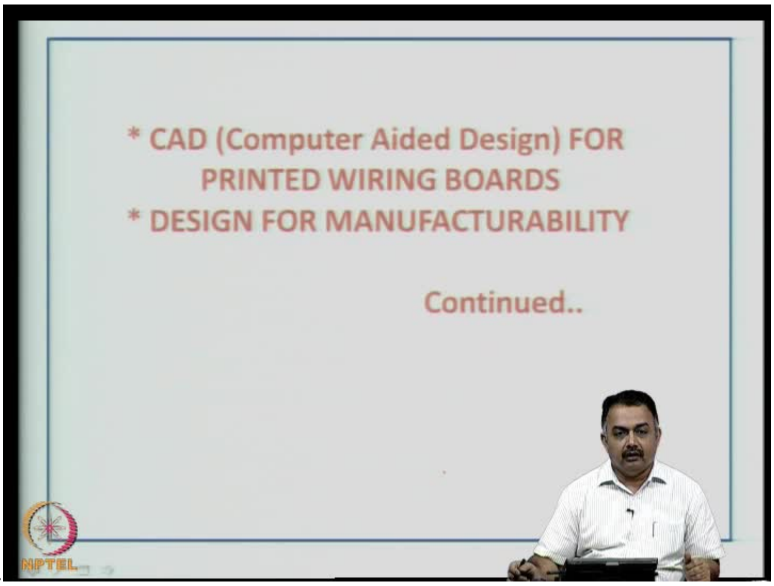

We will continue with this chapter on Computer Aided Design for Printed Wiring Boards. This is the fourth hour that we are spending on this very important topic of CAD for printed wiring boards. We have also dealt on the terms design for manufacturability.

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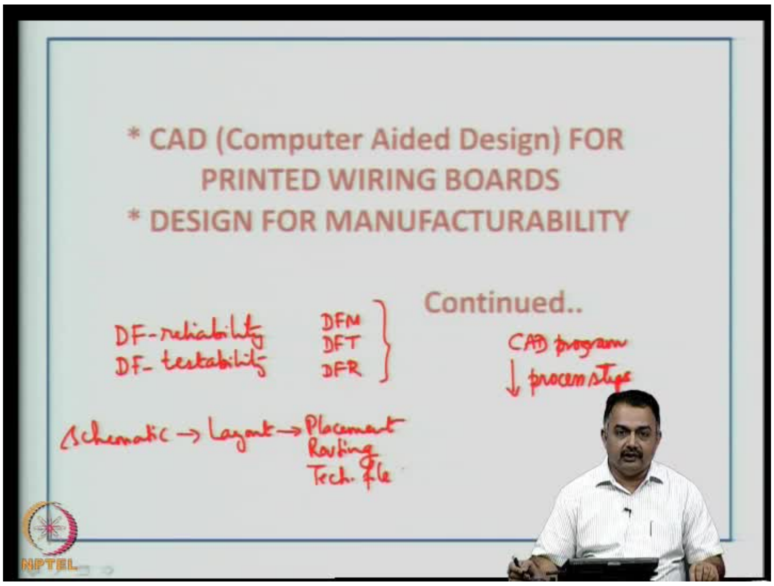

The other term that we have dealt with during this has been design for reliability and also design for testability so we have DFM, DFT and DFR. So, when you read up a lot of papers pertaining to CAD and related to manufacturing, you will come across these terms. It is better to be aware of these terms; what these imply for a designer? Because, as you know, this course is for basically designers, who can do a very good job, if they can understand manufacturing and long term reliability for a particular electronic product.

We have seen in this particular chapter, the process flow for any CAD program or software and we have also seen the process steps. Starting from a schematic to the layout module, and then the layout module contains the placement, then the routing and then the post process files like tech file generation and so on. So, as a designer you have to spend a lot of time in creating these modules for a particular design work. We have seen that the schematics can take up to more than five pages, because if it is a very high dense design, then you have to very carefully split these into pages and you can easily integrate them, because electrically these pages are connected.

So, we will now cover the other aspects in this particular topic. We were looking at the layout module in the last class. So, we will continue from there.

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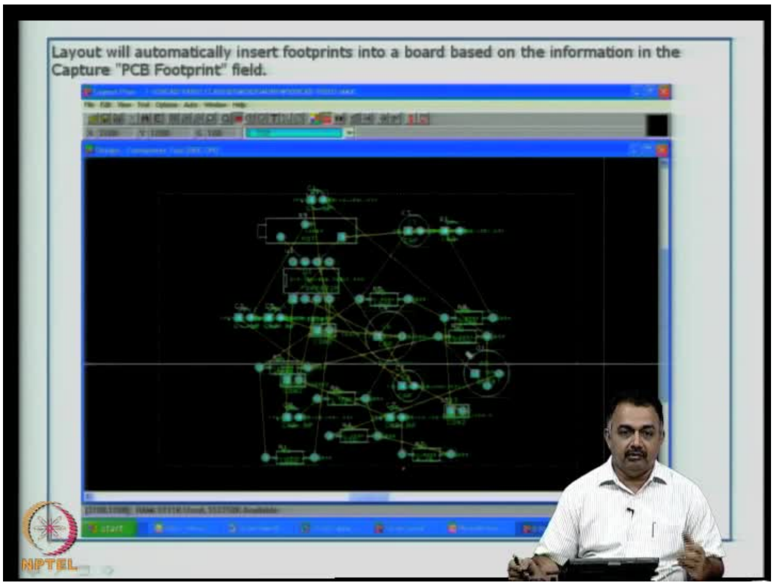

The layout will automatically insert the footprints of all the components that you have used in the board, based on the information that you have given in the schematic section. If you can recollect, when you do a schematic, you are bringing the symbol and then each symbol is actually connected or related to a footprint. This footprint information comes into the layout module, which you are seeing here in this particular figure. What you see here in this figure is that, there is a board outline, as you can see here, (Refer Slide Time: 03:47) this arrow, this is the board outline; this can be tentative. Now, you can see the body outline of various packages. This is a particular package and you can see the pin numbers 1, 2 and 3. This is probably an integrated circuit. There is a body outline and you can see the two rows of pins and then these are all the various components connectors resistors capacitors and so on.

At the first instant, what you see here is that the board outline is probably too large for this particular set of components, but what is more important for you to notice here is that the components come with the interconnections intact. So, these yellow lines that you see between components are the interconnections that you have mentioned in the schematic by means of wires. So, the wiring information is coming along with the packages and the footprints. We call this this particular feature as rats nest in very common terminologies used in CAD because, you can see the connections are intact only in the actual routing of the components need to be done.

And the other feature that you will see here is basically that the footprints are clearly mentioned here the reference designations like C 1, C 2, C 3 for capacitor, U 1, U 2, U 3 for active devices, connectors J 1, J 2, J 3 and so on, resistors R 1, R 2, R 3 and so on and the pin numbering as well as the package names are very clearly mentioned in this particular stage. This is the first thing that you will see when you are exporting your schematic information into the layout module.

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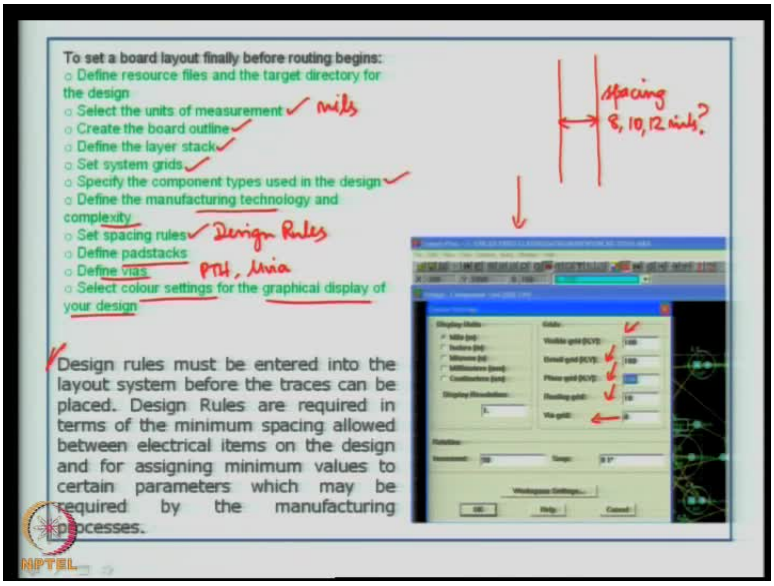

Now, to set a board layout before routing begins, now there are two things that you need to do; define the board outline very clearly, the board outline becomes very important because that is going to be a deciding factor for your product. I mentioned earlier in one of the classes that as a designer you have two challenges when you design a printed wiring board for an electronic product. The first thing is the board sometimes decides the shape and the final size of the product, in some cases the product size is already well defined and you have to work within a restricted board area, to pack all your components, that becomes more difficult.

Now, let us look at the items that you have to be worried about at this particular stage. Define resource files and the target directory for the design in your software tool, select the units of measurement, very important, normally we work with mils; I told you 1 mil is 25.4 microns based on US military standards. Create the board outline define the layer stack layer stack basically means how many number of layers you want to work with and finish your design. Is it going to be a single sided board design? Is it going to be a double sided board design or a four layer, six layers, eight layers and so on. The number of layers always is in even numbers above two layer boards. Then you have to look at system grids, any software will work on a grid pattern, whether it is placement of components or routing of your tracks. We will spend some time on that. Specify the component types used in the design. Now, in a complex design, you might have various types of components. It could be through-hole component, it can be a surface mount device or it can be a mixture of both these and accordingly the manufacturing technology and the complexity increases the assembly complexity also increases. As a designer you should be aware of that.

Set the spacing rules, we are also going to discuss shortly, what do you mean by spacing rules. Basically, here we are worried about the design rules for manufacturing, design rules for testing. So for example, a simple example would be if you have two tracks running close to each other, one of the design rules that you will be worried about is, what is the spacing between these two tracks, is it eight mils, is it ten mils or is it twelve mils. Now that decision as a designer you have to take care based on the density of the board, the pin density of the entire design and the manufacturing complexity that you will be met with in your work area. Define pad stacks. Now, different components have different pad sizes and there are also items like, when you look at the… when you edit a component in the footprint part of it, you will see that lot of information goes into the annular ring information of a pad, drill diameter information of the pad and so on. So, you have to define the pad stack. Then define the number of or the type of vias. Is it going to be a simple platted trough hole via or is it going to be a micro via? If so, in each case what is the size of the vias that you are going to use for different areas in the board. So, it need not be uniform via size across the board. You can vary the via size, let us say for a through-hole via from 600 micron to 200 micron, 0.6 mm to 0.2 mm depending upon the design and the electrical requirement.

Finally setting or selecting the color settings for the graphical display of your design because when you work with multilayer boards for example, you need to differentiate, at least on the screen initially between the different components that you are using in the multilayers. So, as a designer, please remember that design rules must be entered into the layout system before the traces can be placed in your design. They are required very important because editing it finally, would mean a lot of rework. Design rules are required in terms of the minimum spacing allowed between electrical items on the design and for assigning minimum values to certain parameters like space between two tracks or space between two pads which may be required certainly and which will be asked by the manufacturer.

So this screen, what it shows here is for example, displaying the electrical items in mils you are also able to look at the visible grid, the detail grid, the placement grid, the routing grid and the via grid. So, you will have opportunity in your software, in this case it is VORCAD to give these settings initially before the routing begins

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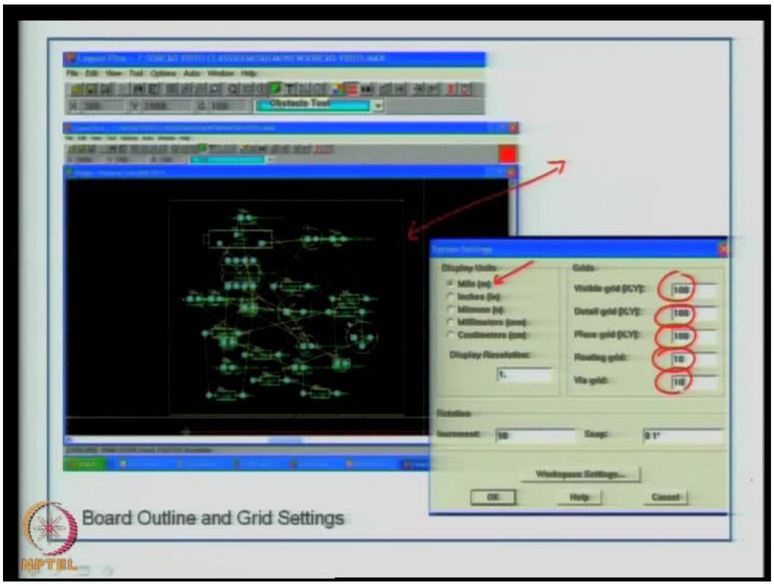

This screen is probably very clear to you. You can see that on the right side picture, you see that the visible grid is set at 100 mils, detailed grid is set at 100 mils, placement 100, routing grid is 10 mils and the via grid is at 10 mils and the display unit here is in mils. So, fixing the board outline compared to the last figure you can see here that the board outline has been reduced, as a measure based on the number of components and the pin density that you have. Look at these settings in your software very clearly and work on it for some time to understand what it means for manufacturing.

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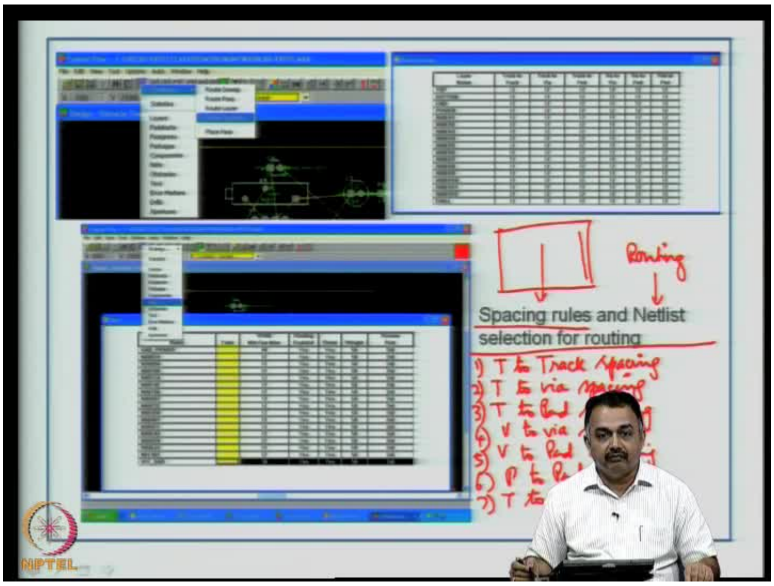

Now, as I mentioned before, spacing rules for a designer are very important and the netlist that you have generated from the schematic, will be the input for your routing that you are going to do. So, netlist is very much important for routing after the placement process is over. You can have different set of spacing rules for different designs. In a particular design itself, you can have spacing rules for different nets. You do not have to have a fixed spacing rule for the entire set of nets in your design. That is the kind of flexibility todays CAD programs have, if you look at it in this particular figure, what you are seeing here is some of the important design rules, which I will write specially here will be, first thing is track to track spacing, T to T would mean track to track spacing. Now can you give 8 mils, 10 mils, 4 mils, 6 mils it depends on your design. Then the next point will be track to via spacing. Then the third thing will be track to pad, the fourth one will be via to via, then the fifth one will be via to a pad the, sixth one will be pad to pad. There is one more important thing that will be, track to edge clearance. That is, if there is a printed wiring board you cannot run a track close to the edge you will have electrical problems and also the finishing problems on the board. So in a board, you please assign all the spacing and the design rules, for an effective design to be completed. This can be a very reliable board and this can be easily tested. So the minimum set of design rules is what we have written here if you dig deep into the complexity of the design at a much later stage I will be able to tell you many other parameters that you can set as a designer for manufacturing.

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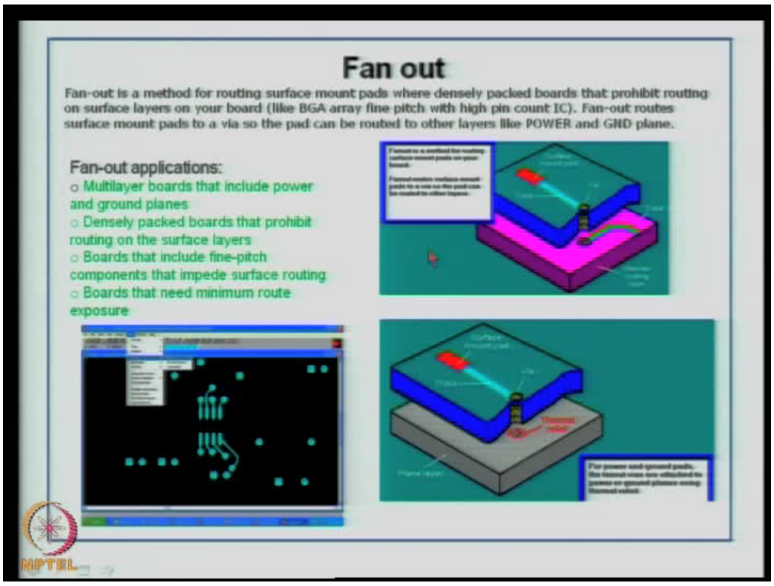

Another important aspect that you will have to look at is what is known as a Fan Out. Fan Out is a method for routing surface mount pads. If you are using surface mount components where densely packed boards that prohibit routing on surface layers on your board like a BGA fine pitch component with a large number of pins high pin count. Therefore, if you look at this figure here, what you see here in the top layer is the surface mount pad on which the component is placed, there is a track that is drawn, it ends in a via structure, this via goes through the next electrical layer that is here in the pink colored surface. It ends here and again it is routed through a track and that goes to may be another pad. That way this particular pad of the surface mount device, the track is actually the pin is actually fanned out, through the via. So it is essential in your design you put a via here and a via can actually go and get connected to a ground plane. This surface can be a ground plane or a power plane depending upon your design. It becomes very flexible to spread your high pin count device into a larger area on the board, so that you can handle the device, you can remove heat and we can also test it.

In the second part, you can see the same structure, surface mount pad. There is a track, it ends in a via, it goes through the next layer and this is a thermal relief that is a power plane and there you have provided what is known as a thermal relief pad. In some cases we will use a thermal relief, which I will mention shortly the difference between the normal pad and the thermal relief pad. (Refer Slide Time: 17:46) Here you get a normal pad; here you are using a thermal relief pad. So, the fan out applications are, when you use multi-layer boards that include power and ground planes, densely packed boards that prohibit routing on the surface layers because you require space, boards which include fine pitch components and that impedes surface routing. When you have a fine pitch component, you cannot fan them out or spread them out on a single layer. So, you slowly move into another layer using a via, boards that need minimum routing exposure, so this is the application, I mean this are the instances where you will use a fan out.

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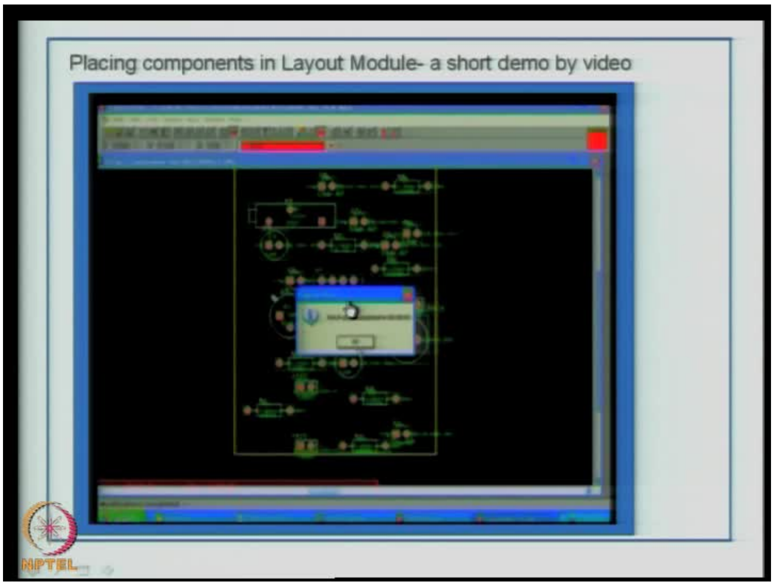

Now we will see a very short demo, which basically describes placing the components in the layout module. So, as this video moves along, I will try to explain what is happening. (Refer Slide Time: 17:46) Here now, you can see that there is a board outline, a tentative one, it could be. You can also always reduce the board size. There is in the corner of the screen in the layout module, the components are just dumped. They are dumped with the interconnections intact like a rats nest. Now, you have to either use the auto placement module or the manual mode and move these components into the board outline area for example, this particular activity shows that we are now moving one component after another and then moving into the board outline area, where exactly you want the component to be placed. As a designer, what I would advise you is that you should always try manual placing first because, in the case of connectors for example, you would like to have connectors at the edges, now if you use a complete placement command you may not get the placement as desired by you. For example, in this particular case you see that the active device needs to be placed in the center of the board outline and all other passives will be built around the active device.

Typically as a good designer, what you have to do is mark the devices that you want in a particular area, in the board, like a connector like or a varistor or a potentiometer that you will access very often after the board is assembled, keep the critical devices at the center and then glue them. So there is a terminology called gluing or fixing the components in your package so you can glue them and then start the autoplacement, which will result in a much better, efficient placement process for your board. So, this is how this video explains to you how effectively you can use a layout module.

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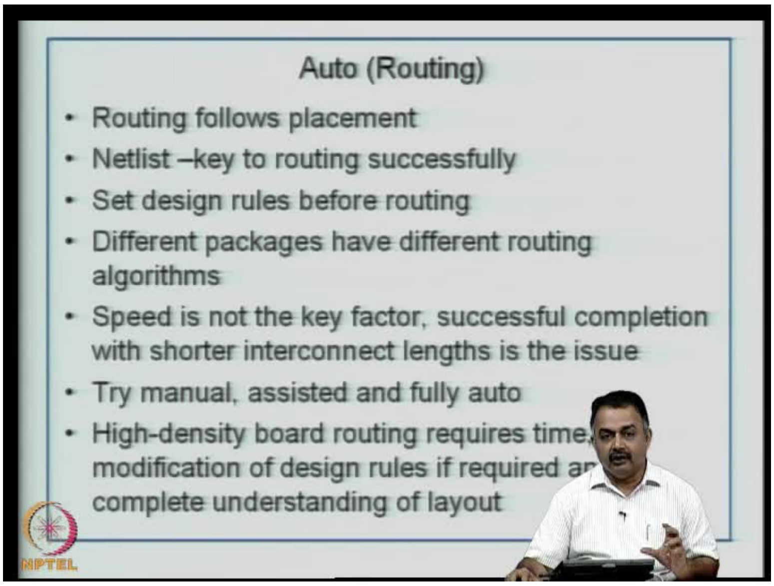

Now after module, obviously you are going to do the routing. You can also do an auto routing or a combined assisted routing but, a typical designer will spend a lot of time using manual routing because you understand exactly where the components are and what typically the net routes have to be, in terms of line width and spacing and so on. So, routing follows placement. Netlist is a key to routing successfully the board. Set design rules before routing. We have seen some of them, different packages have different routing algorithms. So a package A will use some kind of an efficient tool to finish the routing, in a shorter time. Different packages therefore, will have different strategies for routing your boards. Now, in a very dense board you can give at least five to six passes and compare which one is efficient in terms of the design rule that you have set. This is time consuming, if it is a high dense board, which is very normal. Speed is not the key factor, successful completion with shorter interconnect lengths is the issue. So, even in an algorithm, the deciding factor of completing the routes is, shorter interconnects are first finished and the longer nets are kept pending till the end. So, very often you will end up with the longer nets not being completed at all, so you may have to be prepared to that five percent of the routes manually. So, try manual, try assisted and also try fully auto routing independently, so that you understand the power of your tool. High density board routing requires time, modification of design rules in some cases and complete understanding of the entire packages that you have used in your board.

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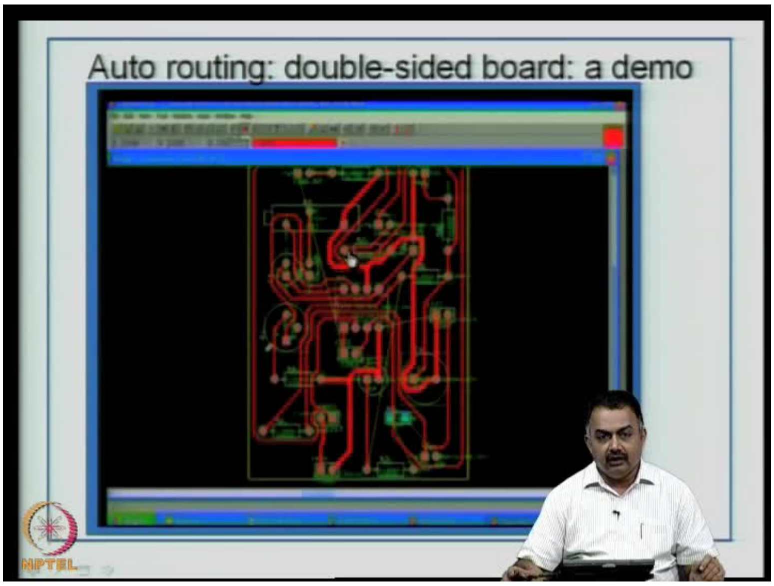

We will now see a demo of a single sided board. Basically, the layout is ready as you can see here. Now, what we are trying to do is every auto router has its own technology, as I said, to provide maximum auto routing power and flexibility. Now in this particular package, you can now try to auto route the board and as you can see here, giving the command of the auto routing for a single sided board, it takes a lot of time because some nets are very lengthy enough. You can also expect a few percentages of nets not being completed at all, because the distances of the components are longer. Some of the nets act as obstacles, some of the packages act as obstacles. So, as you can see here very carefully, some of the nets are not routed for example, (Refer Slide Time: 24:18) this is an unrouted net, this is an unrouted net, now this is an unrouted net. So, you have to now manually do this or the next best alternative is change the placement of the components or rearrange the components in such a way, that you can provide space and also remove those components which act as obstacles for your routing of the single sided board. So, you can move this components as you can see here, the nets will be intact when you move the components, so you do not have to worry about that and if you become an expert designer, by moving these packages you will be able to get an idea that the next pass of auto routing will be rather successful.

Now if required you can also increase the board size, increase the board outline, if you feel that this space is not enough. So, you can spend some time on moving the components effectively to provide less obstacles for your routing. Remember this is a single sided board; so, if the space restriction is there for this particular design, obviously a lot of manual routing will have to be done because you are not allowed to do a double sided board based on the company's requirement let us say. So, after having spent a lot of time on the placement now you go for auto routing and then you will see a different set of routes are being placed and the board is almost completely routed so in some cases you may have to increase the board size for example, in this case there is still a couple of nets unrouted, in that case, you may have to definitely go in for a double sided board. So, you can see in this particular figure, the percentage of routing is around 90 percent. In this particular board area you have difficulty.

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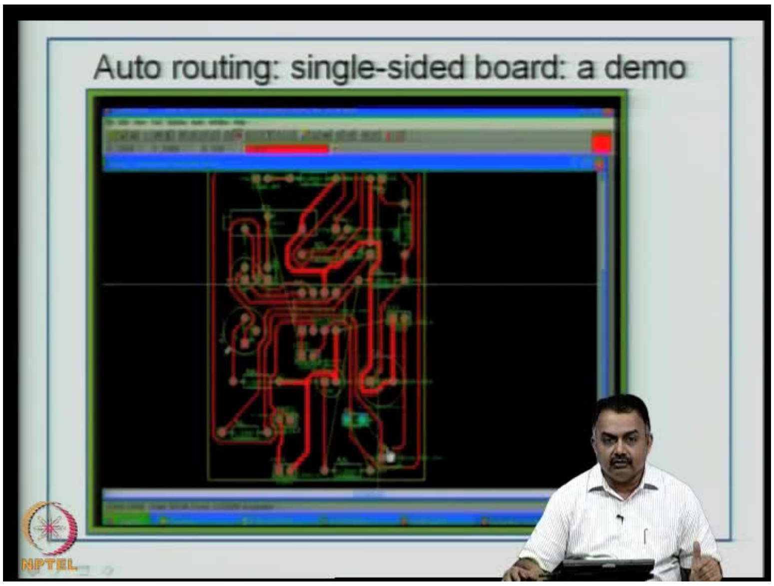

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Now we will try to use the same design and see how we can do a double sided board design where you can achieve 100 percent routing. Now this demo is for a double sided board, the same design is now imported, I mean is now used the first thing that you will do to check a double sided auto routing is that you discard all the nets. So, go to the tool where you will unroute this entire set of nets that you have done on the basis of a single sided routing strategy. Now, you can go and set the parameters, the top layer electrical layer is activated; the bottom electrical layer is again activated. Now the design rules for a double sided board will have to be set and then you start the auto routing. Now you see here, the entire board is complete. The blue lines represent one particular layer and the red lines represent the second layer the two electrical layers.

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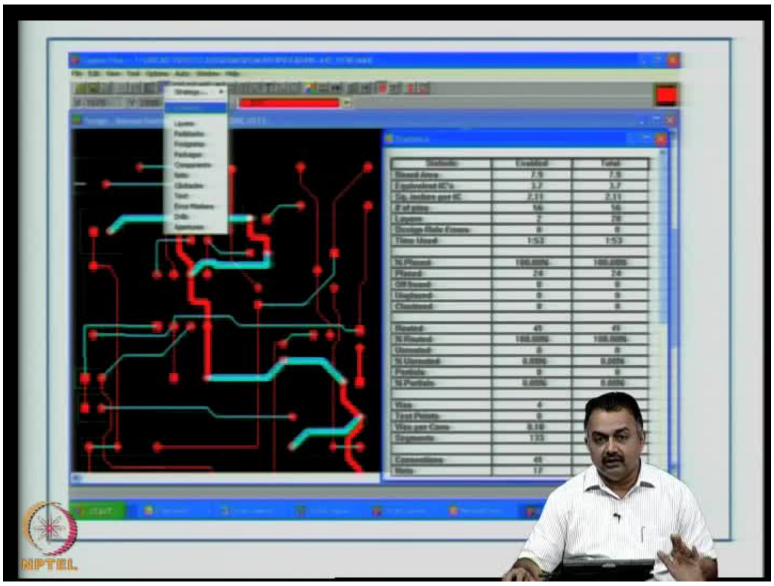

So, by moving from a single sided board design to a double sided board design, here you can see the blue lines represent the one side of the tracks on the board the red represents the other side, where the tracks are placed. So this is copper one and this is copper two. Now the interconnection between copper one and copper two is by means of a via as you can see here (Refer Slide Time: 28:17). So, a via is placed in the printed circuit board, so that you can interconnect or connect layer one to layer two, copper one to copper two. So, the size of the via, you have to very carefully select, depending on the track width that you are having and the space availability and also the manufacturing capability of the manufacturer. At any point of time in your package, you can find statics on your board. What are the statistics? Information like board area, number of ICs used, square inches of IC use that is pin density, number of pins, number of layers, design rule errors, because you have set a design rule, has it worked according to your design rule, time spent, percentage placed, percentage routed and then you can also see number of vias used, test points, vias per connection, segments of nets, total nets used and so on. So this is a very good verification, board status report that any program or software will give.

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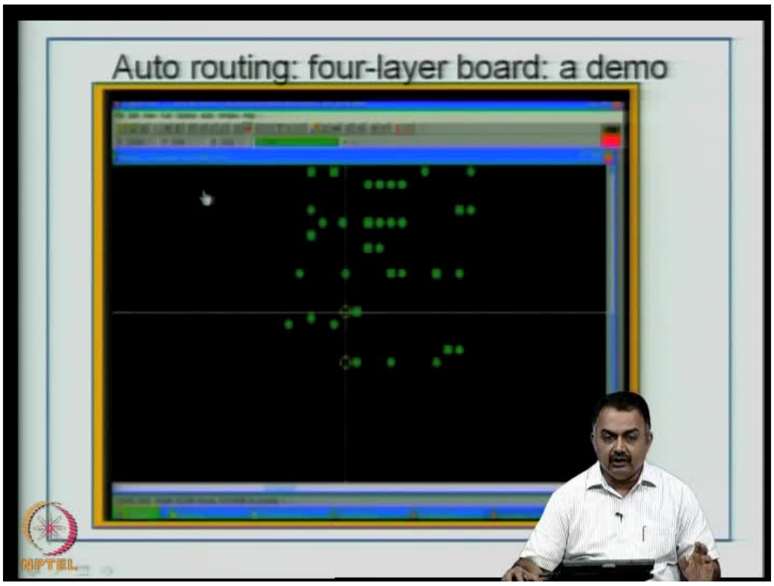

Now, we will look at a four layer board for the same design as a demo. So, the capability of your software is that it can do multi-layer boards provided you set the design rules perfectly. The same design is being used here now; we are converting this board into a four layer board. So, the first thing that you will do is remove the nets that you have generated for this double sided board. Then, the important thing is now you have to visualize a four layer board a top electrical layer, a bottom electrical layer, then you need to have a ground plane, so you activate the ground plane that is required to be inserted and then a power plane which is again not considered an electrical layer. It is considered as a plane layer, so you can also set the design rules that is the line width to be used in those areas and you can also name this particular layer as ground, power and so on. Typically, now with the top, bottom electrical layers, and the ground and the V_{cc} for example, if you want to name it as V_{cc}, you will have four layers. Now the routing will be done for these four layers. Now you can set the design rules for each of these and then you will see that board is complete 100 percent routed. Then you can also visually on the screen look at each of these layers. You can see the two electrical layers on screen; this is the top electrical layer, (Refer Slide Time: 31:21) bottom electrical layer. You can see the inner layer, you can also see the thermal relief pad in yellow, here this is the thermal relief pad and then you can also see the fourth layer so and this is the other layer that you are seeing. So, using the on off switch option, toggle switches and different color codes on your screen, you can view all the components of your four layer board as the case may be. We have seen how we have progressed for a same design from a single sided board to a double sided board and then a four layer board. So, for more complex boards you can use number of layers as the case may be.

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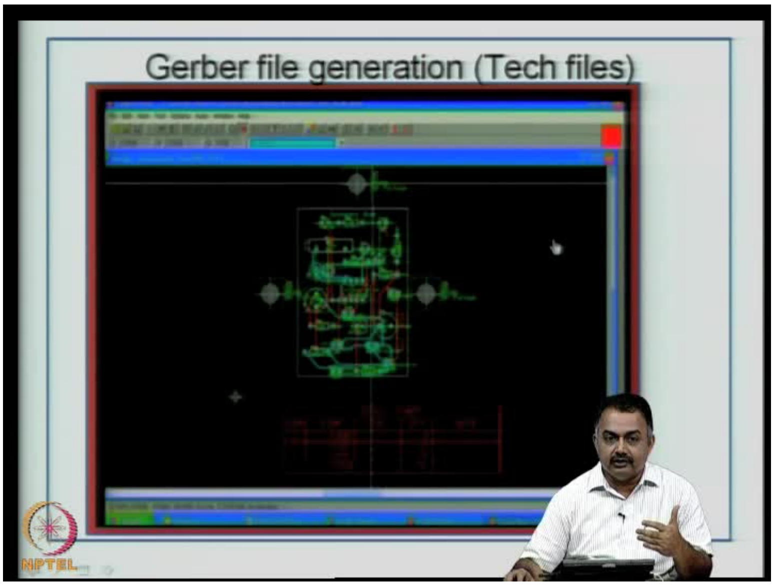

Now finally, after the routing is complete you will have to generate technology files for this particular design. Typically a Gerber file is generated for all the electrical layers, and which is plotted on a silver halide film, which I briefly mentioned. Typically a Gerber file can be created for the top electrical layer, bottom electrical layer, then the ground and power so you have four Gerber files generated. Then you will have other accessories like solder mask on top, solder mask on bottom, silk screen text on top, silk screen text on bottom, if it is a placement on both sides. So, accordingly you have to do this post processing activation, in your particular program. So, that when you start the post processing, all of these set of files are generated. Now, you can also create drill file from this post processing activity. So for example, what you are seeing on screen is the photo plot of a single electrical layer, components side electrical layer which will be sent to the photo plotting person, who will plot this on a silver halide filament giving it to you. Similarly, all of these masks can be created. So, post processing is a very important activity, once you have finished your routing work and the number of sets of tech files that you generate will depend on the number of layers that you have worked with. For example, this is an information that you have where you see that the photo plotting information is perfectly given here it talks about the pad sizes, the track sizes. This is known as decodes.

So the decodes are universal and is accepted by all Gerber based photo plotting machines across the globe. So, you can send the set of information anywhere and get your masks done. Then after this you can also create a drill file. So, drill file is based on excellon format and a drill file typically you will see x, y coordinates of the drill mentioned, the number of drill bits used and the sizes of each of drill bits used, including the vias and the pads and so on. This is a very good documentation that you have to correctly generate before you send it off by electronic means to the manufacturer.

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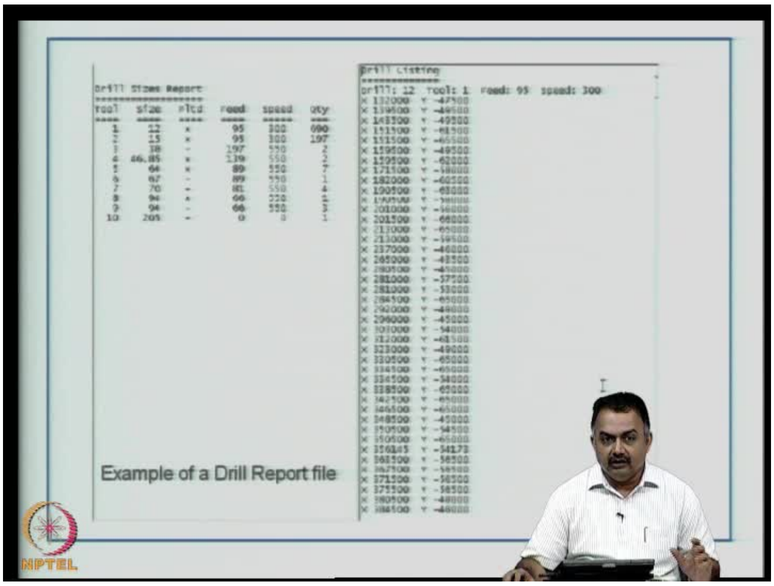

This is an example of a drill report file because the other files are in Gerber format. The drilling information is in an excellon format, what you see here is a drill report. It says the number of tools, the size of the drill bits that is to be used in this particular design, typically the speed is mentioned for the drilling machine for a CNC machine and here it indicates the number of holes totally in your printed circuit board and if you look at the detailed report it will say tool number one for example, if it is 0.6 mm let us say, the x, y coordinates for each of these drill hits that is to be hit or drilled in the surface of the printed circuit board is very clearly mentioned this is the input information for your CNC drilling machine.

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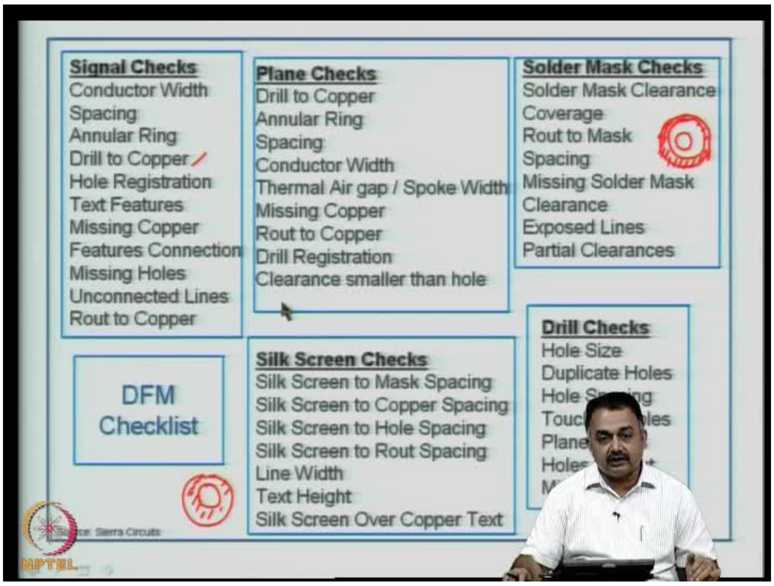

Now the design for manufacturing checklist is what I have presented here. We saw a few design rules, but very carefully if you look at the total activity in your board design. You will have opportunities to look at various parameters that you need to be worried about as a designer. One is the signal checks conducted with spacing. Annular ring information, the annular ring basically means that you have a pad and then a drill pad and this is the annular ring (Refer Slide Time: 36:43). Annular ring information gives you about the total pad size and the copper to be used and then in that what is the drill hole that is to be generated for a through-hole connection. Drill to copper, hole registration, text features, missing copper, features connection, missing holes, unconnected lines, rout to copper. These are the signal checks that you have to do, plane checks, drill to copper, annular ring, spacing between tracks, conductor width thermal, air gap, missing copper, rout to copper, drill registration, clearance smaller than hole. These are the things you can identify as defects during the processing of your boards and this basically means that you have a set of design rules which you have to follow in your manufacturing when you use a solder mask, which is basically used to prevent bridging on the top side and the bottom side of your final board, you have to look at what is known as a solder mask clearance solder mask clearance is usually about 5 mils. So if you have a pad here, and this pad needs to be open finally, this is a drill you will have, a third area which we call as a solder mask clearance, which means the solder mask will not cover the copper area. So, you are trying to give to the manufacturer and the assembly company, maximum copper available for a good assembly process.

So like this you can have various sets of solder mask check, missing solder mask, clearance, exposed lines, partial clearance. There are set of drill checks and there are set of silk screen. Silk screen is basically the text information that you see on a finished board.

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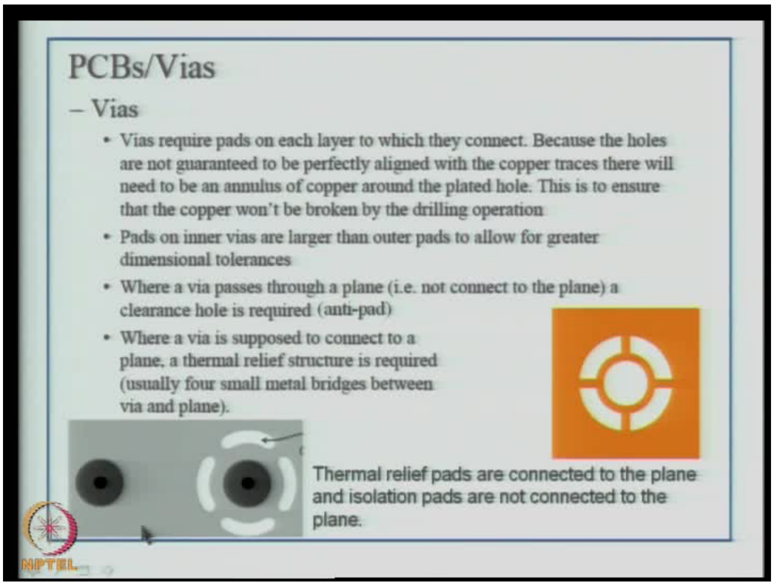

Now I would like to explain what is a thermal relief pad and what is an anti pad information. Basically, if you look at the previous classes I have explained vias are required on every layer; if it is a double sided board you require vias to connect layer one and layer two and multi-layer board you will have different sets of vias connecting different electrical layers on your board. Now, the holes are not guaranteed to be perfectly aligned in a multi-layer board, because the imaging can be varying for different layers and when you stack them on to a multi-layer board there is a good chance that there can be misregistration. That is why we give a annulus of copper area around the platted hole. This is to make sure that copper is not broken away by the drilling operation and you will not end up in a complete open or you will not end up in a situation where you have less copper for soldering process. Pads on the inner via layers are larger than the outer pads because again the dimensional tolerance need to be, will be greater for aligning inner layer boards of a multi-layer board. When a via passes through a plane of copper a clearance whole is required, if you do not want to connect to the plane. That is if you are not intending by electrical design not to connect to the plane then you provide an antipad. This is an antipad what you see here in this figure. So it will totally isolate that pad from the copper plane.

So but, when a via is supposed to connect to a plane a thermal relief structure is given. As you can see here, (Refer Slide Time: 41:00) this is a thermal relief design, this is also a thermal relief design. You can see that the there is a cut off between these kind of short pads with the gap. So, it can actually be a complete copper area but, spacing is provided so that to provide thermal relief. So, thermal relief pads are connected to the plane whereas, isolation pads are not connected to the plane.

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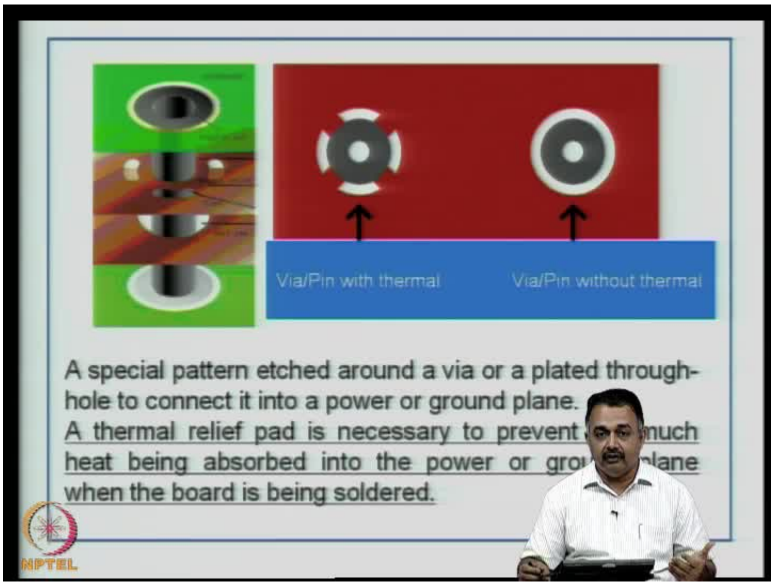

But, why do we require a thermal relief pad before we go into that I would like to explain once again with another picture. See, (Refer Slide Time: 41:34) imagine this is a through-hole, nicely drilled hole, this is the top layer you can see, this is the solder mask, green solder mask, this is the pad and this is the drill area, you can see the annular ring. Now the hole passes through the second layer and here you can see the thermal relief is provided. This is copper, there is no copper here, copper, no copper, copper, no copper and if you can imagine the hole going through the third layer, here there is no copper at all touching the platted through-hole. The copper is here. So, this is an antipad structure and it ends up in the fourth layer. This is a typical via containing a thermal relief pad and containing an antipad structure. In this particular case intentionally you do not want to connect to this plane whereas, here you want to connect but, you provide thermal relief in some cases not all connections to the inner plane need to be through a thermal relief. When do you provide a thermal relief? A thermal relief pad is necessary to prevent too much heat being absorbed into the power of the ground plane in your design when the board is being soldered. So imagine you are placing a component in this through-hole structure and then you are manually soldering it using a soldering iron; now if the heat from the pin passes through this structure through the via and it because there is too much of copper here, the heat will be easily absorbed. Now when the heat is easily absorbed, the solder is not melting at the right temperature, you are now increasing the soldering tip temperature intentionally to make the solder melt but, this is more than that required for actually soldering the component. What happens is that your structure gets damaged, your board gets damaged, your component gets damaged and therefore, to prevent that kind of a situation during manual soldering, you provide this thermal relief. So that, the heat that is absorbed is not too much and heating takes place quickly to melt the solder and enable good soldering and get a wet solder for your component. You do not want to spend too much time on your soldering process. This is the picture that shows a via or pin with thermal relief and this is without thermal relief now you will able to get an idea when to use a thermal relief pad and when not to use a thermal relief pad and also when to use an antipad structure.

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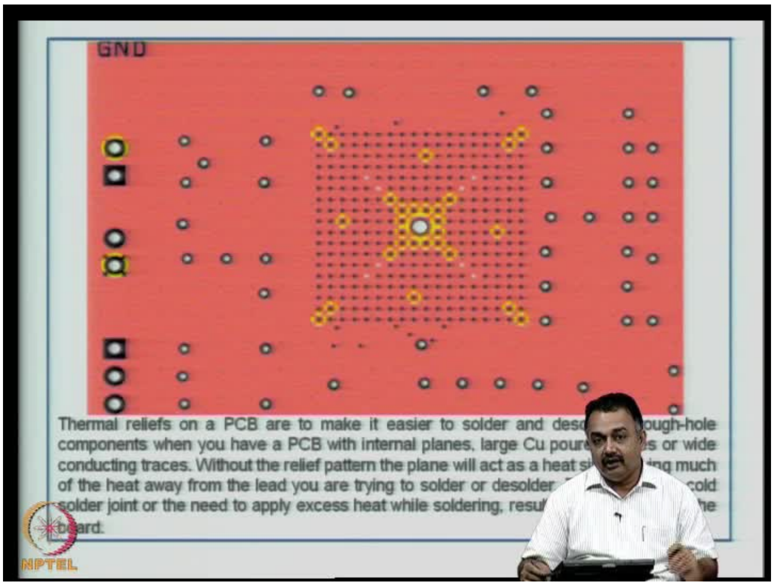

So this is an example again to show you in a board, you can see here this is a BGA structure. This is a pin layout for a BGA and selectively, we have given here thermal relief packs; the yellow one that you see here are the thermal relief pads, based on your component pin configuration. Assembling these kind of large pin count components becomes perfect, when you use a thermal relief.

Without the relief pattern, the plane will act as a heat sink, drawing much of the heat away from the component lead that your trying to solder or desolder; then, it could become a cold solder joint and you try to apply more heat; damaging the board; damaging the pin or the solder ball; or the component itself.

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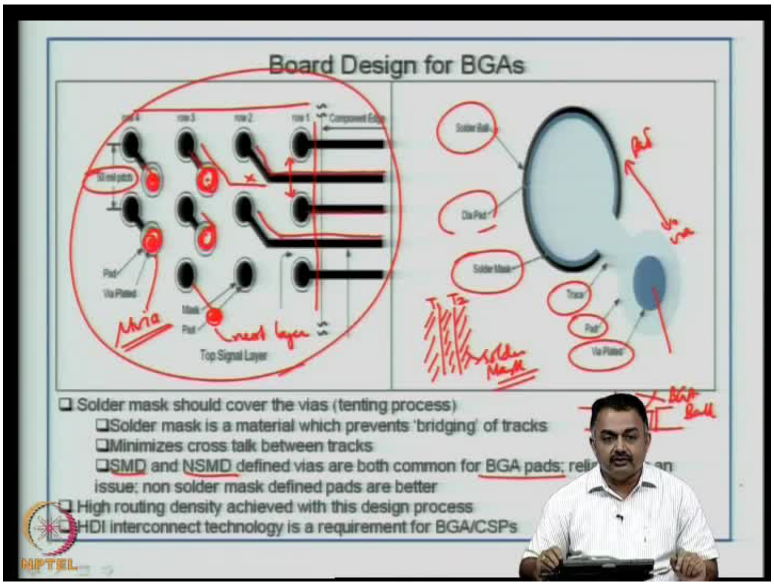

If you look at BGA design, as a designer, doing a through-hole may be relatively easy, because the pin count is small, but for a BGA, you have a matrix of solder balls or pins in this fashion. What you are seeing here, is basically an array; row, then, this is the matrix that you are seeing; in this particular example, you have 4, 3, 2, 1; 4 rows and here again, you have 3 rows or more; Now how are you going to do routing for a BGA?

If you look at the top view; this is row 1, you can easily take a track to the top surface of the board; for the next row, because you cannot extend it directly because there is a row obstacle here, you take a 45 degree bend and then do the tracing; there is space enough space between 2 rows of 2 adjacent pins; typically if you take this as a 50 mil pitch, then you can take 1 track; this is the next one; then the next row pin for this particular BGA, again you can do a parallel structure like this; now, if you come to the third row, you cannot extend the same thing here, because there is no space; so you take it here 45 degrees, create a via and then take it to the next layer; so, the need for using multi layer boards arises when you use BGAs, because of the high pin density; so here, it will go to the next layer; similarly, here, it will go to the next layer and so on. So all these things will go to the next layer.

Then, if you come to the row 4, probably again, this will be the via and you can take it to the immediate next layer; or if there is no space available, it can go to the second layer below. So, that is how the number of layers increase for a BGA design. If the number of pins or solder balls are more in a BGA you can expect, definitely, a 4 or a 6 layer board.

So this is typically a micro via that you can do; it needs a small via, you cannot use a very large via structure here; and for improving the reliability of this design, you want to use a micro via using a SBU technique, which I will explain, when we come to manufacturing; and typically you do not want a through-hole structure.

Now, this is again explaining to you, the typical fan out from the pad to the via. This is the pad and this is the via structure for a BGA design. So, as a designer, you must be aware of the Solder Mask clearance, the diameter of the pad, then the solder ball diameter, the trace width, track width, pad size and the via platting that you require and to which layer it goes. The solder masks should cover the vias; basically it is a tenting process; you can see here, the solder mask covering the vias, because the vias have to be protected and solder mask is a material, epoxy material, which prevents bridging of tracks. It also minimizes the cross talk between tracks. So, if you have 2 tracks running the non-track areas will be covered with the solder mask; so, the 2 tracks are actually protected. So if you take this as T_1 track one, track two; there is also an issue with solder mask defined pads and non solder mask defined pads for a BGA; although this is a very detailed chapter for designers, what I would rather say is that, if there is a landing pad for a BGA, that pad can have solder mask overlapping the pad or not overlapping the pad. So if there is a pad here; and if the BGA landing here, the solder mask can overlap or it can be away with a clearance.

These 2 procedures are adopted by designers today. Reliability is definitely an issue, but by experience what I have seen is that non solder mask defined pads are much better because they give allowances for the stresses that are developed in the BGA balls, otherwise the solder mask will cover a small portion of the copper pad; and the stresses will be built up in the in the BGA ball. High routing density is achieved with this design process, so what we have seeing here is a process to achieve high density; and to manufacture this you have to use HDI interconnect technology.

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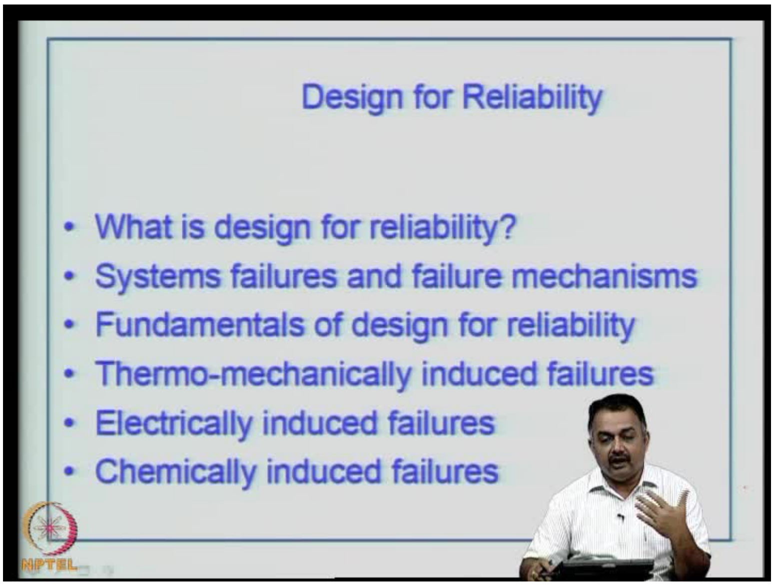

This is, in brief, about the CAD process and as a designer I have given you a large number of tips; there are much more tips, but it comes by practice and experience and interacting with your manufacturer. Finally, I would like to talk about design for reliability; we have talked about design for manufacturing, I will briefly spend some time on design for reliability, which designers need to be aware of.

What is design for reliability? Because at the design stage itself, you must think of reliability. Reliability is not something that after manufacturing, you wait and watch. When a mobile phone is manufactured, they have already calculated the reliability of that product; how much time it will have, shelf life; and that includes the printed circuit board; it includes the components; it includes the solder material; it includes the substrate material and so on. All of this put together, as a designer, you can calculate the mean time to failure or mean time between failures.

System failures and failure mechanisms are very common, but you need to understand what can be expected, if we use a set of materials. Fundamentals of design for reliability - you need to understand, most failures are thermomechanically induced failures; there can be electrically induced failures and chemically induced failures. But all failures, whether it is chemical induced or mechanically induced, it will end up as an electrical failure.

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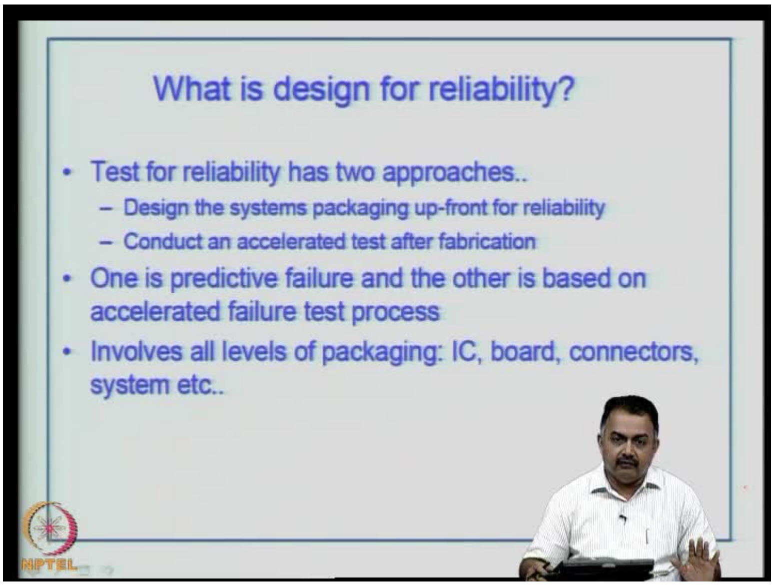

Test for reliability has got two approaches: design the systems packaging up front for reliability; so look at these considerations; if you have some details about materials and processing, do some simulation and try to find out; apart from your electrical simulation, apart from your thermal, you can do some approach, soul searching, to find out if a product can withstand the environmental conditions. Normally what people do is, they conduct an accelerated test, after the board is fabricated; for example, they set room temperature to 125 degree centigrade for 500 hours, 1000 hours and see if there is any failure including tracks, pads, components, substrate, warpage and so on. But you can simulate this beforehand. So, that is what we call as predictive failure. One of the concepts is that, if you do a systematic analysis, you probably do not have to do an experimental verification; on the other hand you have to do an experimental verification and compare; but this involves all level all levels of packaging, whether it is IC board, connectors, system, etcetera.

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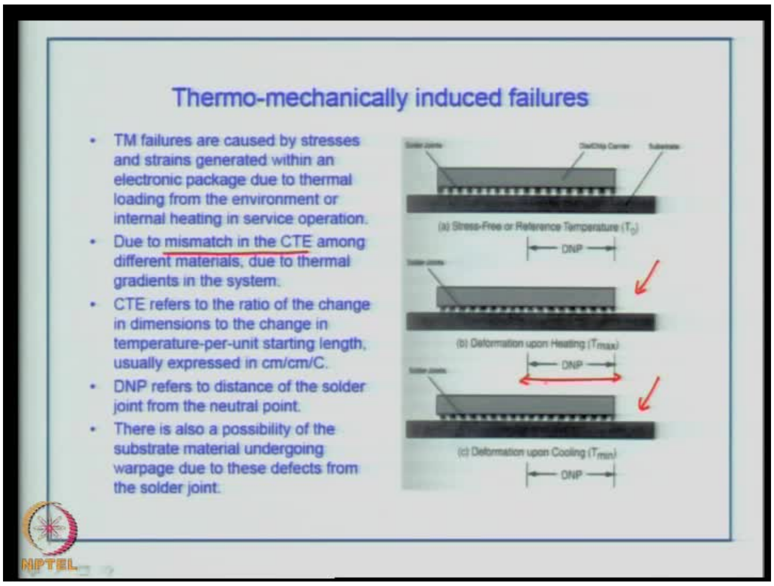

A very common failure that you will see is Thermo-mechanically induced failures. You see here a flip chip, with a solder bump, that is a substrate; and here upon heating and upon cooling, you can see that there is deformation; there are changes; there are stresses built in the system. This is also caused by mismatch in the coefficient of thermal expansion parameter for each material. So you need to understand this CTE value, for all the materials that you are using in your design because there is always this thermal load that is going to affect your design. The CTE refers to the ratio of change in dimensions to the change in temperature per unit starting length, usually expressed in centimeters per degree centigrade; and DNP refers to the distance of the solder joint from the neutral point. So, if this is the central point, you will actually calculate what the deformation that is taking place based on continuous heating and cooling. There is also a possibility of substrate material undergoing warpage, if it is not suited for that system.

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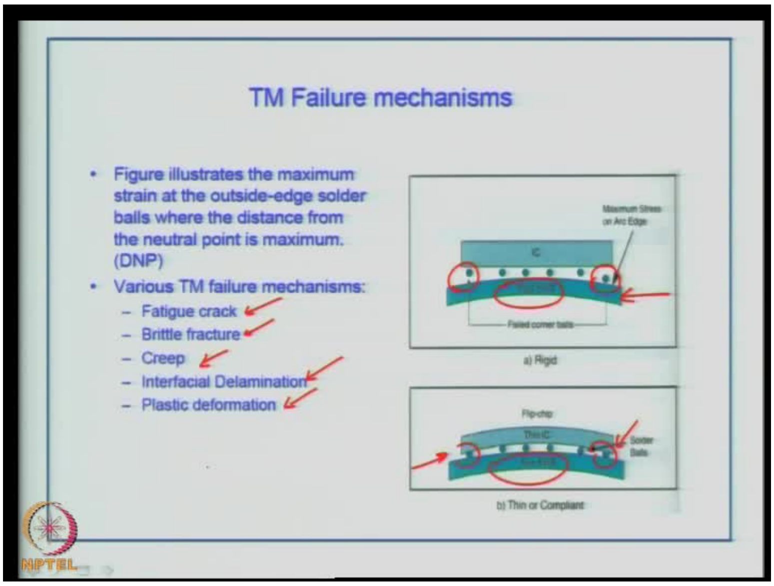

Now, this is a very good example; as you can see here, there is a rigid printed wiring board. This is rigid; and here you have a flex PCB. Now, you are using a flip chip with a solder bump; and if you look at the temperature cycling for this system, you will see upon continuous thermal cycling or thermal load, there is stresses built upon the corner solder balls, and usually they can detach away; but in a flex PCB, you can see, because it is compliant with the thermal load, because the material is thin and flexible, the connections are not lost. So why not use a flex PCB, rather than a rigid PCB? Or even in a in the case of a rigid PCB, why cannot we use smaller thicknesses.

So, the various failures that you can expect as a mechanical engineer can be fatigue crack, brittle fracture, creep, interfacial delamination, plastic deformation - that is from the substrate point of view, and as a designer you need to be aware of this.

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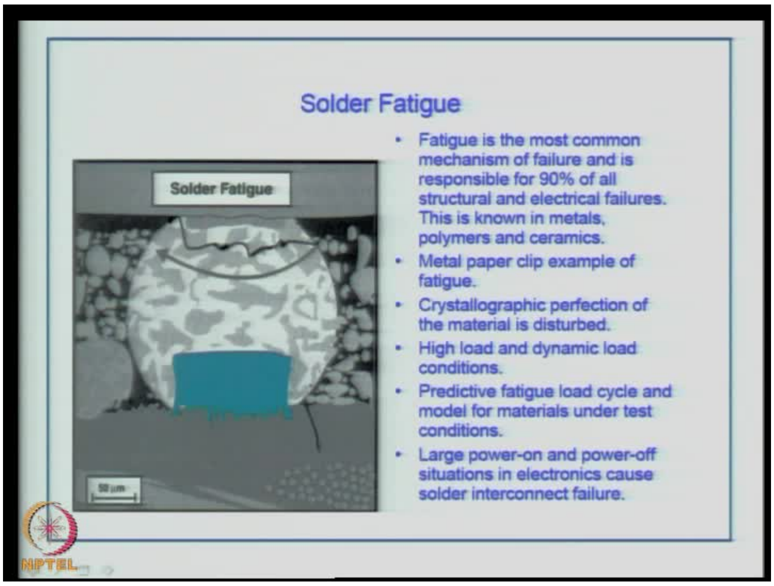

Solder fatigue is very common and fatigue actually takes place upon time. Once the board is fabricated; once the components are assembled; and this is known in metals, polymers and ceramics. Crystallographic perfection of the material is disturbed because of the thermal load and dynamic load conditions. You can also predict these kind of failure, solder fatigue failure, if you know the properties of the materials. You can also design against delamination induced failure, typically, if you look at this structure where a via is built using a built up technology. These are areas where delaminations can occur, at the junction between the polymer and the copper, close to the vias, at the knees, at the junctions. How do you prevent these kind of failures? Understand the kind of material that you are given to use, thickness of copper platting, thickness of planes, thickness of inner layer dielectrics; and assume the load that it will be exhibited or expected to withstand and then try to do a simulation; and design against these kinds of failure.

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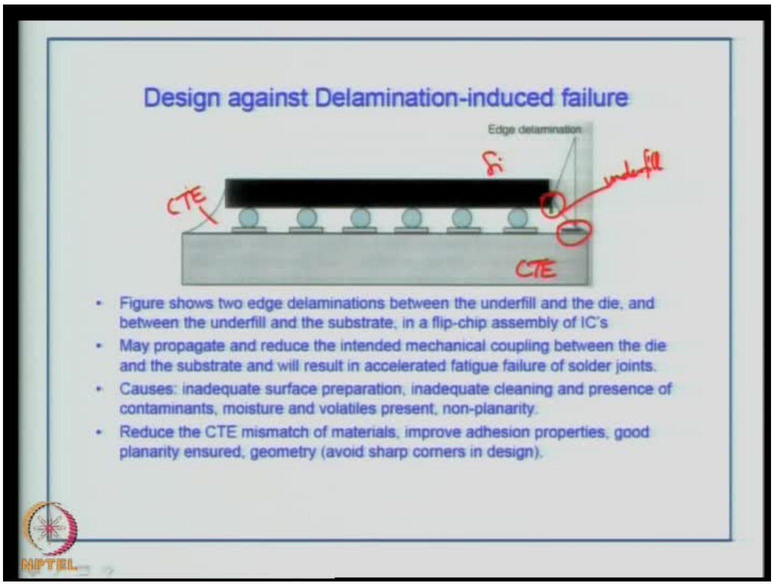

Then, we have design against delamination induced failure. This is very typical of flip chip kind of connection, where an underfill is used; and you can also have cracks in the underfill, close to the edge of the chip, or close to the edge of the PCB. So, the curing conditions are very important; and if you have used a very poor underfill; and if the CTEs between the silicon die; the CTE of this organic material and the CTE of the underfill are grossly misdesigned or ill designed, you can expect delamination induced failures, especially the edge lamination.

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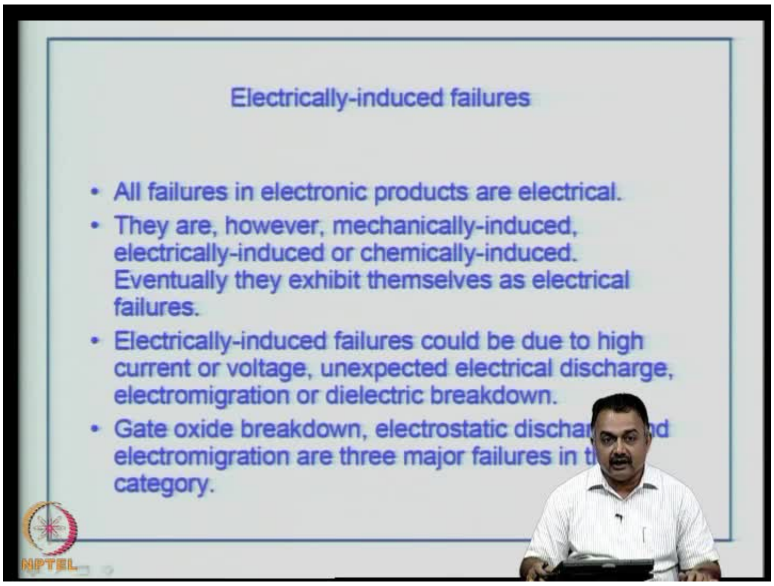

Electrical failures: All failures in electronic products are electrical; they are, however, mechanically-induced electrically-induced or chemically-induced. But they exhibit themselves as electrical failures. You can expect a lot of this kind of failures, especially gate oxide breakdown, electrostatic discharge and electromigration in this category of electrically induced failures.

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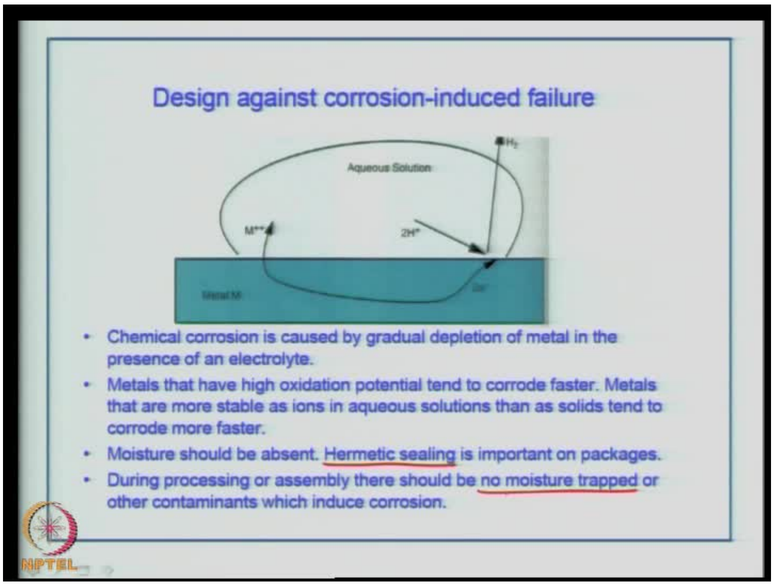

The important thing, which I want to mention is electromigration, especially, if you look at tracks, and if you look at the spacing between tracks, and if you have not protected them well, you can expect a lot of migration. The different current densities that you are using; and the kind of moisture levels; the kind of external debris and process debris, if they are there, these can these can make a situation, where you can have disturbances in the copper, in terms of voids or creating what is known as some kind of a whiskers in tracks, which can lead to a short, due to electromigration, but this is a slow process.

Corrosion is a very typical thing that can happen in the systems, because you are using different materials. Today, components are also absorbing moisture, because of the materials. Hermetic sealing is very important on packages; try to use hermetic sealing; there should be no moisture trapped or other contaminants; during the process, drying is very important; the process needs to be well controlled to remove moisture; even your encapsulants will absorb moisture, but you have to dry it before they are actually used, or during use you have to make sure that it is moisture free. So, these are some of the important things that you have to take care of including intermetallic diffusion, which we see in the solder material.

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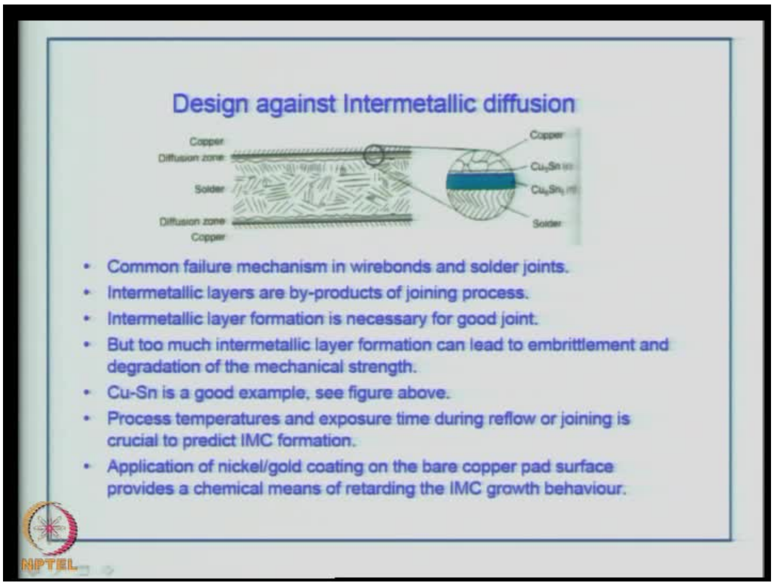

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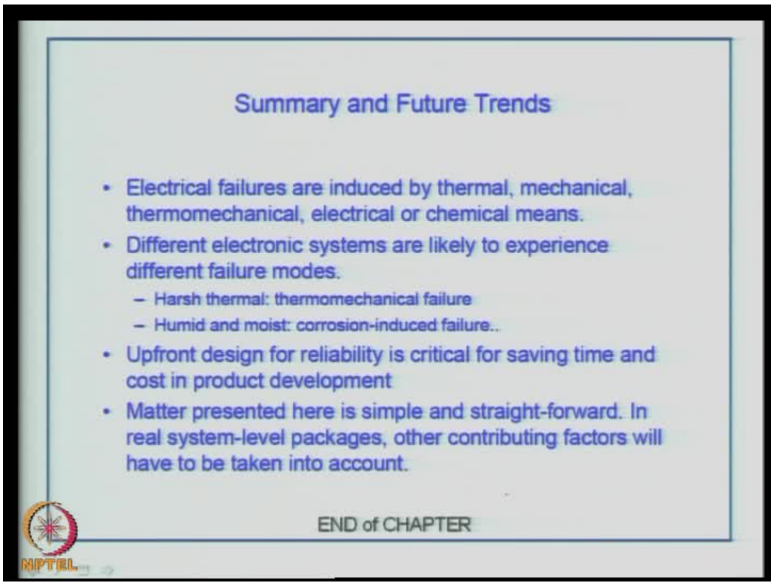

As a summary of this chapter, electrical failures are induced by thermal, mechanical, electrical or chemical means. Harsh thermal environment is one; humid and moist environment can also cause failure. As a designer, apart from your CAD work, or while doing your CAD work, you please look into these aspects, as an issue that can prevent failures in completed systems, but this requires the coordination of designers, manufacturers, assembly people and materials - especially materials that are being used, the people who supply these materials, the data sheet and so on. This will complete the CAD design for manufacturing; design for reliability and design for testability. In the future class, the next class, we will look at the process steps of creating a system level printed wiring board.