CMOS Digital VLSI Design
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Module No # 02
Lecture No # 08
POWER ANALYSIS – I

Hello everybody welcome again to the NPTEL online certification course on CMOS digital VLSI design in our previous lecture we have actually understood what is CMOS inverter how it is works and give your detail 1 and 0. We also seen what is the meaning of propagation delay and noise margin and then how they are related to the device parameter and circuit parameter devices parameter primarily means aspect ratio which is W/L.

And circuit parameters are such as a your capacitances as so on and hence so forth in your previous lecture we had actually stopped at the point were we discussing power dissipation. So this module will be dedicated to understanding what do you mean by power dissipation and what are the methods available as a designer to actually reduce the power dissipation or optimal power dissipation with in the available resources without compromising on it performance analysis.

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So let me give to you an idea about what do you mean by energy so the whole since it is a whole thing is about to power there is no outline slide as such in this case so will we doing first of all the what you be understand by power and energy and then we will see for CMOS inverter is how

its works at. Well energy as you know it is measured in joules or kilo watt hours and it is the ability of a system to do a work or produce a change right.

So as I discuss with you that there is no activity you do not have activity involved and then do not have any power energy dissipated right. So no activity is possible without energy and this is bottle neck for any other inverters because any inverter to work you need to have switching that only produce the energy and the energy will be dissipated across the silicon and they by lower by the has by making it getting heated up more and more.

Let us look the concept of power will it is measured in watts as I discuss with you measured in watts or kilo watts and it is amount of energy required per unit time right. So basically if you are spending larger amount of energy per unit time you have actually dissipating higher power right. So as we move along we will see that either you reduce the total energy output energy or you reduce or you make the time frame which you reduce the power reduce the energy.

So either of this two cases the power will fall down right so that is easier said and done but it is how it is works out now per unit time the average amount of energy consumed is defined is the average is the average power as the simple expression is studied from the basic physics. And therefore we have to very clear but it is the amount of energy which is consumed per unit time is defined as my average power.

In most of the cases throughout this lecture as well as the subsequent lectures we will be referring to the total power for understanding a purposes this total power as I discuss with you in the previous lecture it is the basically the sum of addition of static power, dynamic power and well as leakage power right and our short circuit power what you mean by the instantaneous power?

Because when T tends to 0 we define that to be as instantaneous power which means that for a short plus of import if you are consuming large amount of energy your instantaneous power will be very high right why it is important because in certain cases in certain interconnect in certain junctions if the junction temperature exceeds the particular value even for a very short duration of time the junction will get destroyed right and that makes the whole flow of deign in the

difficult state. And the reliability and heals comes under the question and therefore this motivation is required for this study.

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Let me therefore come to you the basic definitions and energies as you very well know power is basically defined as a voltage into time that means if the voltage drop at the particular point at the particular time multiplied by the current flowing through that as a function of time will be define as my power. So power is equal to vt as i discussed with you.

What you mean by electrical energy electrical what is mean electrical energy it basically means power into time because power was defined as energy per unit time so I get energy equal to power into time and therefore it was nothing but equals to vt multiplied by it multiplied by t which you see in front of you here. So therefore if a power if a energy is held for a longer duration of time you get higher sorry the power get the longer duration of time you get higher energy being generated out of it right.

Well therefore from my from understanding the basic concepts of power and concepts of electrical power you should be aware or you should be aware of fact that we define a very important tern in specially in CMOS circuits that is energy is equal to power into delay. Which means that in a critical path from primary input to primary output of a digital circuits. If you know the power being dissipated and you also know the delay if you simply multiply you get the energy which is as per the definition we learn from here and here.

So therefore if you want to reduce energy either if you reduce delay or you have to reduce power the only problem is the power and delay they do not go they do not get lower down together or they do not get the heightened together. If power is increased power dissipation goes high delay also increases there by reducing a frequency similarly if you reduce your delay you power dissipation is goes high.

So the problem is that you need to find a solution which will optimize this energy rather than power itself right and to optimize it you need to optimize the power and you need to optimize the delay individually in order achieve this result fine. So with this basic third process or basic idea we have understood therefore what do you mean by power and energy as per our definition.

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And let us suppose that your connected generally all your digital electronics or digital VLSI chip design we referred the input power the power supply to be equals to VDD and if nothing is said or assume that the lowest potential is basically your ground. So if nothing is same assume that the lowest potential is ground and highest potential is basically equals to VDD right.

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Power and Energy

- Power is drawn from a voltage source attached to the V_{DD} pin(s) of a chip.

- Instantaneous Power:
$$P(t) = i_{DD}(t)V_{DD}$$

- Energy:
$$E = \int_0^T P(t)dt = \int_0^T i_{DD}(t)V_{DD}dt$$

- Average Power:
$$P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}dt$$

So it is quite interesting the highest potential in a chip will be equal to VDD and lowest potential will be equals to ground right it can also negative value right it can be also less than 0 can be also one of the lowest potential available to you. But typically this is the values which you see and this is known as power rail and this is known as ground rail. So whenever you draw a circuitry this is basically a power rail right and this is a ground rail right which you see.

And between these two rails you will all have your circuits available here right and these are power rails will be added and ground rail is added like this and there will be power rail like this. So this will be the general structure of any system design or basic combinational logic design right with this knowledge the instantaneous power as i discussed with you will be equal to this much.

Which is nothing but the current flowing at the particular time T at which your the time of instantaneous power multiplied by VDD where VDD is applied voltage at that particular point. We define energy as if you remember energy was nothing but if you integrated the power in time determine from 0 to T right that is basically energy. So what I do I take Ptdt and integrate from 0 to t and what I get from here iDD VDD into 0 to t right where 0 is the point at which the current starts to flow and the capital T is the time at which you do have a stoppage of current.

Which means that the current becomes a function of time T and therefore the energy is dissipated per unit time might vary but the total energy will still remain the same that is what you can see

from here right let us discuss what is known as average power? right average power. Average power is energy divided by the total time T right and that is what you see the same expression which see here this expression divided by capital T is my average power right. But for most cases in the whole logic design which we study or combinational logic design when we talk of power we talk of total power right transient when do you a transient we talk about let us say we do a transient analysis.

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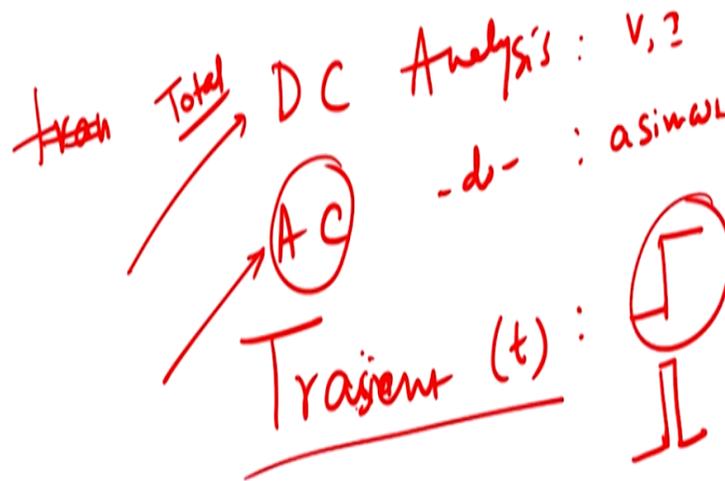
Then when we do a transient so as you remember there the two three analysis as I discussed with you in the earlier cases. We have a DC analysis we were transient analysis right what is DC analysis DC analysis when you have DC bias and you want to find the voltage current under DC bias what is AC? When you input is at AC cycle and for example A sin omega T what is a transient? When you give impulse give a delta function something like this right and because of this you will have a function of time T available to you.

So in most of the cases whenever we doing DC analysis we talk of total power to the total of power available to us what you talk of AC analysis the value is changing or the value of your system in fact if your doing for the example not giving a pulse but you are giving a input signal which in the satisfied in nature then we will discuss AC. And if you giving a pulse you will doing a transient analysis. Now so that is the reason the average power is given by E / T in this cases.

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Power Consumption in CMOS
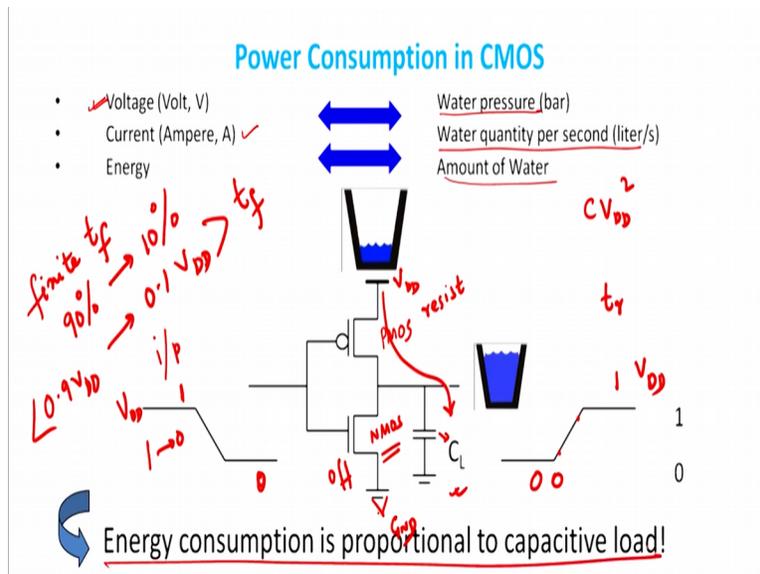
Let me give you a brief idea what are what is the formula here now if you remember in our previous discussion we had seen this was my PMOS right this is my PMOS right and this was my NMOS and I had a load capacitance here CL assume it sorry this is your VDD line and this is your ground. So this is your ground which is the earth this is your ground and you have got assume this power line to be having large amount of water sort of the glass of water in it right and what I do I give you the input side right 1 to 0 transitions.

So this is 1 this is 0 so I do the 1 to 0 transition which the finite fall time available to me so I have a finite fall time finite tf which is fall time. Fall time is defined as the difference the time taken for the signals to go from the 90% of its highest value to 10% of its highest value right. So if you are if you are looking this is VDD then 0.9 VDD to approximately 0.1 VDD is basically the time taken to do this is basically a tf.

So I have a particular TF available to me because of this TF there is a 1 to 0 transition and therefore I would have to except to see my earlier discuss has 0 to 1 transition which is basically 0 to VDD transition right and the will be also a TF attach to it tr in this case will be tr 10% of VDD or 90% of VDD difference is defined as my rise time. So I have a rise time here now let us see what happen?

So let me give an idea so voltage is sort of water pressure so higher the water pressure more will be a voltage a current is basically water quantity flowing per unit time as I discussed with you

and the energy is total amount of water flowing right. So let us see if I do a small thing that I this is what will happen right that your water will in the first off cycle when 1 to 0.When you giving 1 to 0 what was happening in 1 NMOS was ON right.

Now when you go to 0 PMOS gets on so when NMOS it was ON the capacitors are fully discharged because its was connected to the ground and all charges of capacitor moving to the ground now when you go from 1 to 0 NMOS switches OFF and PMOS goes to the resistive state right resistant state was this happen voltage from VDD line starts to charge Cl in this path. As you discuss in the earlier stage which means that whenever you have a 1 to 0 in the transition output there will be energy drawn from VDD and stored were in the Cl in the capacitor block here.

Is it is clear? So how much do you store CVDD square is the energy you stored amount of stored right. Energy consumed therefore is directionally proportional to capacitive load that is simple and straight forward. Why because higher the capacitor load more time it will take by the same amount of current the charged fully of the bring it to values equal to VDD. So if your capacitor lower you can safely thing but the amount of time taken to bring it is the highest value to VDD will be lower therefore your energy consumption will be lower right.
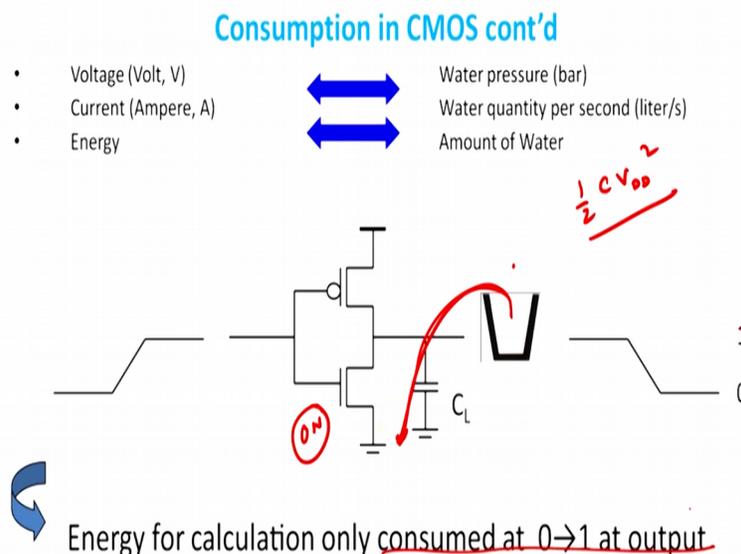
But let us suppose the energy consumption with you see let me see what will happen if I do 1 to 0 transition right. If I do 1 to 0 transmission during 1 your NMOS was ON sorry your NMOS was basically ON and when you go to higher value PMOS gets ON in that case right when

PMOS gets ON this gets the charged. So what was happening in the previous case? I will explain to you what happen in the previous case? In the previous case initially 1 NMOS was ON right if you look very closely here NMOS was ON this is the initial case.

There was no water here and what I do I go from 1 to 0 and this allows to my PMOS to go is ON right and chargers the capacitance to this and therefore this starts to fill up right. Now we have discuss the energy therefore it is proportional to the capacitive load.

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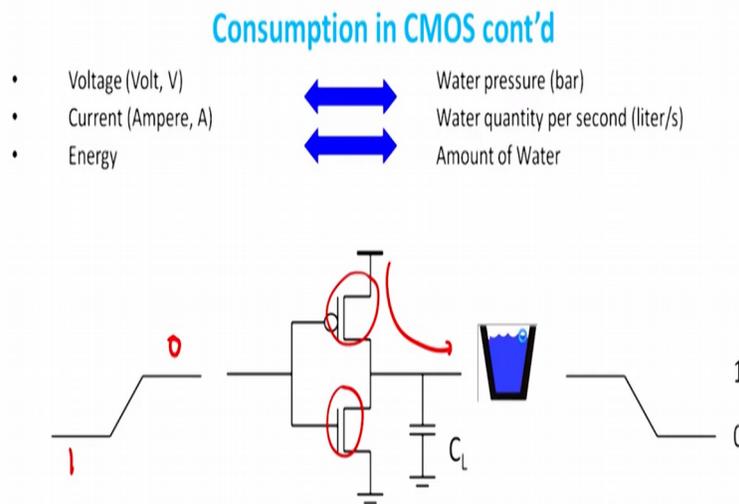
Now if I take a 1 to 0 transition first of all initially it was suppose this is fully charged now. Once it is fully charged and I go from again I make it 1 then what will happen is this well at this instant. This will discharge across at this path agreed why initially it was 0 and going to 1 as it goes to 1 NMOS switch is on and all the charge stored here actually goes to this page and how much it is half CVDD square will in this case right.

So this is what you get that means whenever you go from output goes so the output goes from 1 to 0 your capacitors starts to discharge and therefore energy is consumed only at 0 to 1 output I think I am clear to why is it like that energy is only consumed when you have the 0 to 1 transition in the output side because 0 to 1 in the output corresponds to PMOS getting ON and your consuming the energy from the power rail and you are storing in the capacitor. Where are you dissipating energy when you discharging the charge in the capacitor through the NMOS structure when output is going from1 to 0.
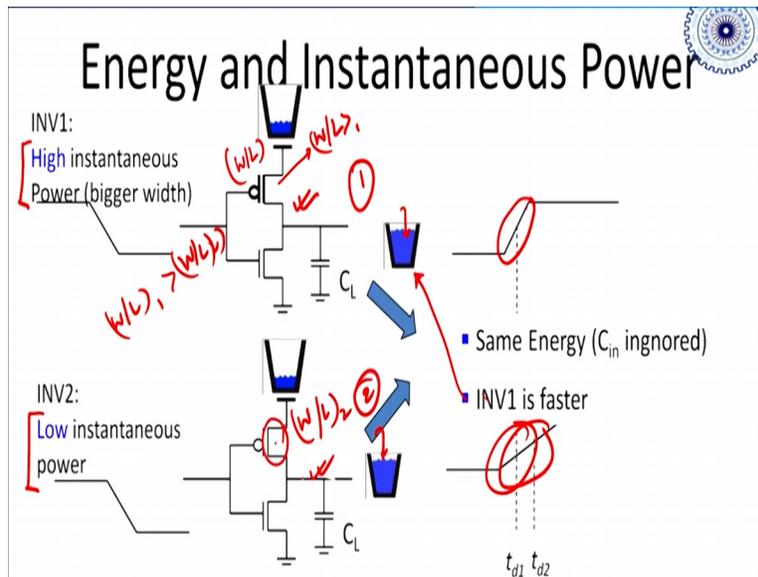
So let me say like this it is happens it is very straight forward and very simple way of looking at it that if let as suppose your W / L ratio of this one PMOS was higher by compare to the W/L ratio of this one so let us suppose this is W/L ratio 2 and this is one and W/L of 1 is greater than 2 then you can safely assume that the current flowing through the circuitry will be this circuitry will be larger as comparing to the current flowing in the circuitry.

Therefore this will be filling up faster compared to this and therefore the rise time will much smaller as compared to this am i clear? I will explain you once again what do I mean to say if I improve or if I make my aspect ratio of this W/L of the of the pull up PMOS to be higher it implies that the current flow through PMOS will also be larger as compared to current flow through this PMOS and as a result the amount of time taken to charge the same value of CL will be smaller incase of the first case which is this one and it will be higher cases in second one.

And therefore the rise time will be faster in the case of the first one right and therefore the rise timer are larger right. So therefore the fast rise this is the slow rise right and therefore inverter 1 is the faster this is faster inverter so how did I receive faster inverter by making the PMOS larger devices as compared to the second inverter PMOS as a result but you understand I am still using the same amount of energy why the same amount of energy? Because CL in both the cases are exactly the same my VDD is exactly the same?
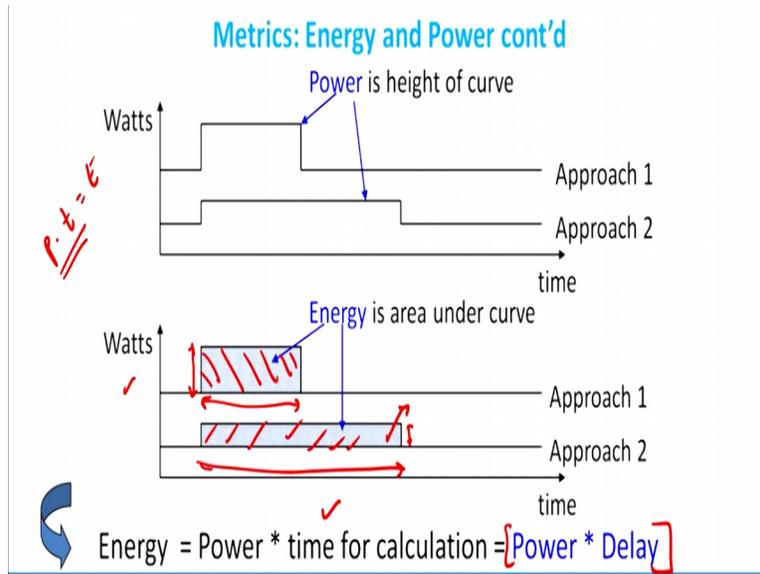
What I am trying to do is the same amount of time I am able to achieve the values in the output side in a much more better manner so therefore I get much high instantaneous power in inverter 1 but I get a low instantaneous power in 2. Why because it is very simple in the second case though your energies are same but the time taken to relive that much amount energy is larger therefore P / T which is P which is actually much lower in the second case how did I do that ?

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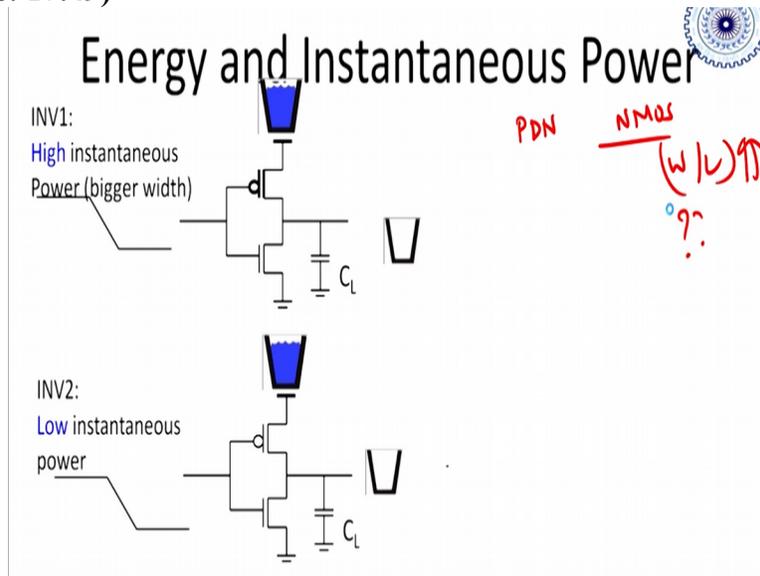
Very simply made the aspect ratio of pull up transistor higher I leave an exercise to you please find out what will happen if your pull down transistor which is basically your NMOS width was higher just think about it right. Just think about it what will happen if the pull down widths are higher it this case fine and should be able to answer this question very easily once you know the relative strengths of PMOS and NMOS and charging and discharging the capacitor.

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Metrics: Energy and Power cont'd

Power is height of curve

Watts ↑ ... Approach 1 ... Approach 2 → time

Energy is area under curve

Watts ↑ ... Approach 1 ... Approach 2 → time

Energy = Power * time for calculation = [Power * Delay]

Let me comes to the therefore the metrics here and first approach is something like that if you come back here I just explain what you mean that now you see as I discuss in the previous discussion if you plot power versus time here. In the first case so power versus time P into T will be equal to E right and therefore you can see so if your power as be made higher but your T is smaller here which is inverter one case in the inverter two case the power is smaller but the time domain is larger.

But the area under the curve P into T is same in the both the cases so the energy consumed is exactly the same but second one is consuming or having an lower instantaneous power is comparing to first one right. So what I am trying to tell you is that by simply change the aspect ratio you can actually have lower power available to you by simply manipulating certain things with in the system.

So this is what I wanted to discuss with you in this case now therefore we define as I discussed with you it is power into delay which is just now found out because this is the power so this is basically your power here right.

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Consumption in CMOS cont'd
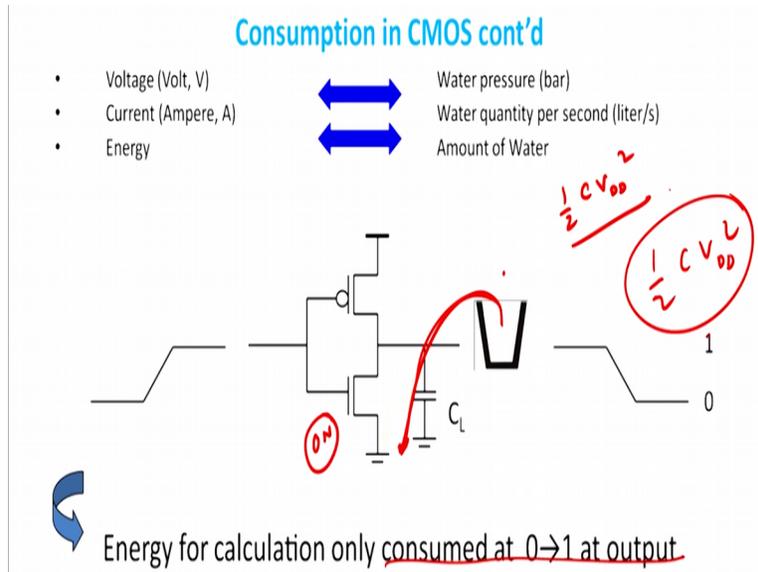
This is your power here and this is the amount time delay 0 to 1 time transition taking place right. 10% to 90% of the VDD is the time taken here that multiplied by P will give you the energy and this much energy was doing what is be absorbed by the devices in this case the capacitance from where from VDD the power rail.

So let me therefore comeback to the initial understanding or initial slides mechanisms here and the mechanisms is therefore that during the off cycle input is going from high to low right. Then you are allowing that capacitor to get the charged and drain in energy = CVDD square during the next half cycle releasing it half CVDD square and therefore for each cycle of propagation half CVDD square is the amount of energy which you are actually dissipating to the environment right is it okay fine.

With this knowledge let us move forward and I explain to you we have discussed the power and energy we have also discussed energy = power into delay and let me therefore give you an idea about some basic issues and then move forward.

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- Energy dissipation
  - Determines battery life in hours
  - Sets packaging limits
- Peak power
  - Determines power ground wiring designs
  - Impacts signal noise margin and reliability analysis

Why energy dissipation is important because lower the energy dissipation low higher will be the battery life typically very important is today's all your handle devices all your PDA's your digital logic should have a very lower energy dissipation. So therefore it will sets the packaging limits also because there are certain issues which the amount of energy releasing is high there are certain packaging issue will limits is energy high.

Because at the end of the day you want to dissipate in the atmosphere right so it can only happen in the convection or conduction right so when conduction is there the material you use for packing interconnects will play a major role in determining how much of energy you are dissipating to the atmosphere to the ambient. Peak power is actually makes our life difficult but we will not be concentrating on this too much but this impacts a signal noise margin.

And it also implies a reliability so if your peak is higher the average power might be low right which means that you are working say at one watt for about 50 days suddenly one day for very few seconds of time you want 50 watts right. That the amount of energy you consume in that period is exactly equals to what you have consumed for last 30 days and as a result you mind sudden drainage of the battery and therefore there will be reliability issues or even the junction temperature is go high. that may destroy the junction temperature so on and hence so forth. So you have to be very careful about what energy we are using? and why we are using those energy right an important criteria.

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Metrics: PDP and EDP

- Power-Delay Product
  - Power P, delay t_p
  - Quality criterion PDP = $P * t_p$ [J]
    - P and t_p have some weight
    - Two designs can have same PDP, even if t_p = 1 year
- Energy-Delay Product
  - EDP = PDP * t_p = $P * t_p^2$
  - Delay t_p has higher weight

$$EDP \propto t_p^2$$

Therefore we define one important product which is again energy here what you known as the power delay product PDP so we always find try to find out the power delay product and we also try to find another important quantity and that is known as energy delay product. Which is nothing but PDP into Tp, Tp is a propagation delay and therefore nothing but P into Tp square which mean if you look very carefully with in EDP right EDP is proportional to Tp square right.

Which means that the propagation delay as got a higher state in determining your EDP so if you able to reduce a Tp propagation delay by half you will be able to your lower your EDP by one fourth that is a bottom line right. Whereas PDP can be half energy can be actually made one fourth right and therefore two designs which is given here can have the same PDP right can have same PDP why? Because one design can have very high power but low Tp and the result can have low power but very high Tp in either two cases PDP remain constant for both the cases.

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Where Does Power Go in CMOS?

- Dynamic Power Consumption
  - Charging and Discharging Capacitors
- Short Circuit Currents
  - Short Circuit Path between Supply Rails during Switching
- Leakage
  - Leaking diodes and transistors

So this is the one of the methods available to us this we have discussed in your previous lectures also. That it is basically your this is dynamic power so the power which you which you have been taken from the VDD rail right the power which can taken from there where does it go actually yes the power goes in the three important consumption it is consumed as dynamic power as I discussed we have short circuit currents we have leakage currents right.

The dynamic power is virtue of charging repeated charging and discharging of capacitors a short circuit is when you have between supply rails and ground if you switch back and forth you have short circuit right and that I discuss later may be I have also discuss in previous discussion and leakages when even when the transistor is off as i discuss with you in the previous discussion you will always have a off currents available to you right these are known as leakage current.

So all this contribute the total power is CMOS inverter let me explain to you what do I mean by dynamic power right. Dynamic power is nothing but the power consumed by the inverter by virtue of constant switching between a high and low state in the output side because every time you go from high to low and vice versa your actually charging and discharging the capacitors respectively right.

So every time you charge the capacitor you store half CVDD square every time you discharge the capacitor you also discharge half CVDD square right and that is how you workout. So o give you a brief idea how it works out?

Dynamic Power Consumption

$$P_{dyn} = C_L * V_{DD}^2 * P_{0 \to 1} * f$$
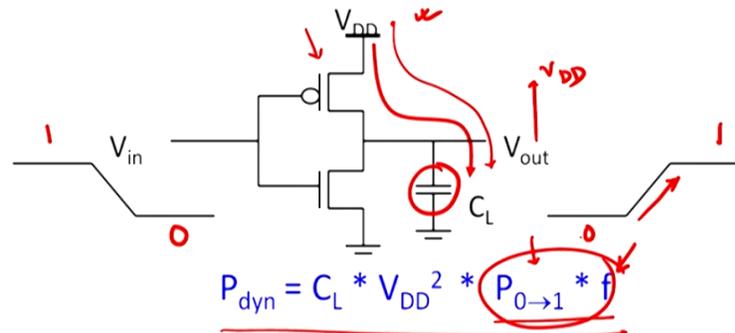
$P_{0 \to 1}$: probability for 0-to-1 switch of output

f : clock frequency

α : activity

When VDD through VDD rail when you try to have a current flow taking place and charging your CL right half CL VDD square is the amount of square energy stored in the capacitor right and the amount of energy given by the VDD rail is CVDD square. So half VDD square again is dissipating through PMOS in that case so we define dynamic power as CL time VDD square right multiplied by P 0 to 1 into f I will explain to you what is term is?

See 0 to 1 transition right is the only power consuming transition right so which transition is 0 to 1 in the output side why I will explain you earlier also. So 0 to 1 in the output primarily means 1 to 0 in the input now 1 to 0 primarily means that your NMOS was initially ON now you are switching on PMOS. So when you are switching on PMOS you are actually consuming current or you are actually getting current from VDD and you are charging the value of CL here.

This is basically a probability for 0 to 1 switch of output you understand why because whenever you will have 0 to 1 switching in the outside side that is time when the capacitor is getting charged by virtue of a connection between the VDD and the output side and this voltage therefore raises to VDD right.

So that is the reason i multiple with probability P 0 into 1 and therefore also multiple the frequency of operation because then I will very well know that mean the 10 clock cycles if there are 10 P0 to 1 the probability is 1 and therefore what you will see is the that the power

dissipation will go up. So what do you get from here is that the probability that is P0 to 1 into F is basically the probability that it is a power consuming cycle and the power consuming cycle will take care of it one or the overall system.

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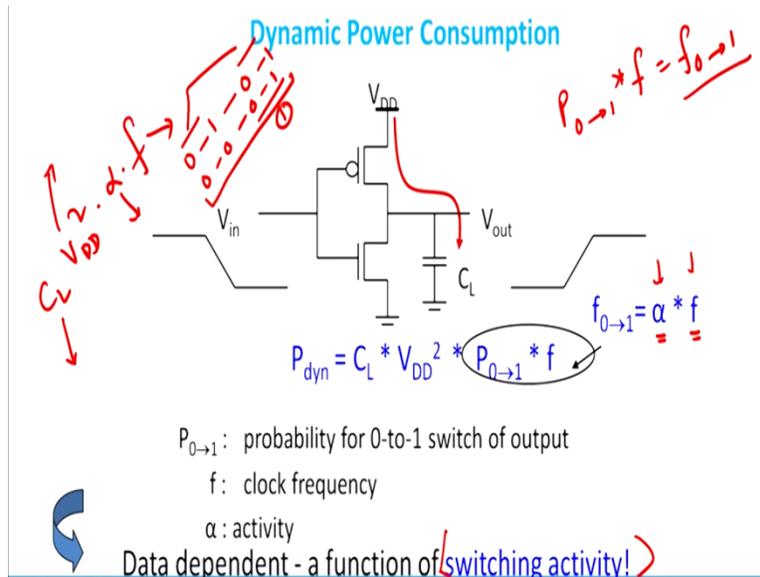
We define very important term here this factor P01 to 1 P0 to 1 into F which is frequency of operation as f of 0 to 1 which is that value of that many number of transition from 0 to 1 which will be always the power consuming transition right and it is also defined as activity factor multiplied by f. I will explain activity factor just now to you and may be in next class explain you what is activity factor? What is that i will explain to you right.

So the final expression is basically CL to VDD square multiplied by alpha into f when f is frequency of operation so I have got CL have got VDD square I have got alpha and I got the F. F is a activity factor f is a frequency operation and CL is the load capacitance and VDD is the power rail voltage available to you. So therefore quite an interesting observation out of all this discussion is that the switching activity the function of switching activity is data dependent.

So if your data is for example let us suppose it is 0, 1 then 0, 1 something like this right and if it is 0, 0, 0, 1 right how many number of 0 in transition in the output side 1, 2 and how many here only 1 so in the cycle of 4 clock cycles I will have two transition of power consuming whereas only one in the second case.

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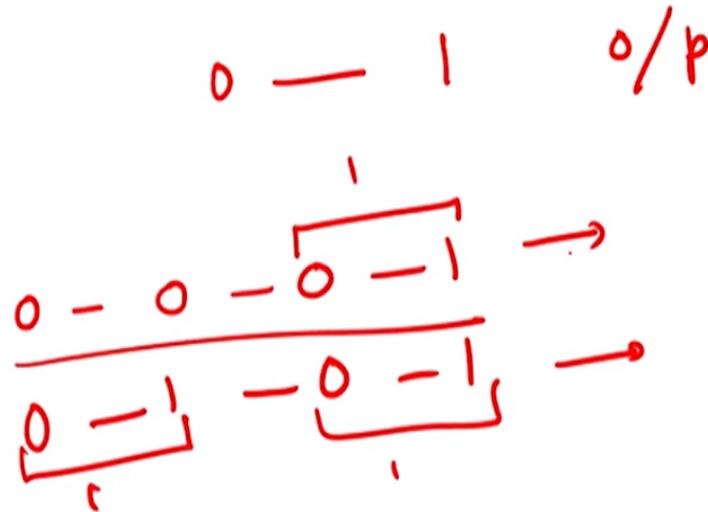
So am I clear the idea is that I told to you 0 to 1 in the output is my power consuming cycle so let us suppose I have a output data which as 0, 0, 0, 1 in 4 clock cycle or four types it has come and I have another case which is 0 to 1 and it is 0 to 1 then you see this case you are having only one transition 0 to 1 whereas in this case you have one transition and two transitions so 1 and 1 and only 1 here so obviously this will be more power consuming as compared to this. So switching activity is therefore data depended what type of data you getting is basically depend on the switching activity depends on the data to a larger extent.

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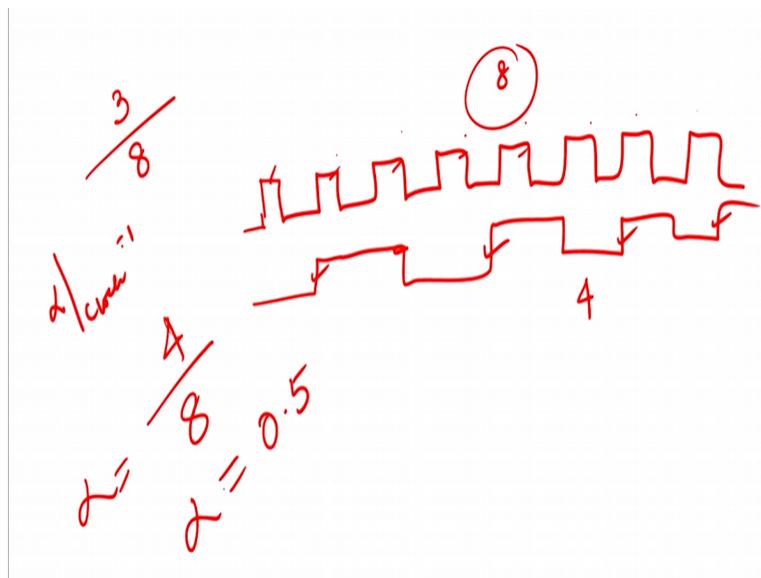
Let us suppose that there are 1, 2, 3, 4, 5, 6, 7, 8 clock cycles so 1, 2, 3, 4, 5, 6, 7, 8 clock cycles are there and in the output side let me say because of some reason because of some complexity

you have say like this 1, 2, 3 so on and hence so forth. So there are 8 clock cycles 1, 2, 3, 4, 5 ,6, 7, 8 and how many 0 to 1 transitions 1, 2, 3 when we define as a activity factor to be equal to 3/8 which means that activity the maximum activity factor is one which of clock.

Because in clock for every clock cycle you will have at least 1 to 0 transition available to you and therefore alpha for clock its always equals to 1 but alpha for some other combinational logical block for other thing might be like this and therefore there might be only 3 or 4 let us suppose something like this that you had a out of this is 1 right and then 2 and let us say 3, let us suppose 4 so I have got 0 to 1 here I have 0 to 1 here.

So in the 8 clock cycle pluses I have to 4 to 0 transition so 4/8 is a alpha which is nothing but 0.5 so 8 times the clock have past only I get 0.5 so what I do my power dissipation dynamic power dissipation is 0.5 into this thing and the reason you can understand why is it like that right but I can be also a high made higher and higher fine so this is the basic idea which i wanted to discuss in this case we will be therefore discussing about short circuit power dissipation in the next class thank you very much.