

NPTEL Video Lecture Topic List - Created by LinuXpert Systems, Chennai

NPTEL Video Course - Electrical Engineering - NOC:VLSI Design Flow: RTL to GDS

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Co-ordinating Institute - IIIT - Delhi

Sub-Titles - Available / Unavailable | MP3 Audio Lectures - Available / Unavailable

Lecture 1 - Basic Concepts of Integrated Circuit - I
Lecture 2 - Basic Concepts of Integrated Circuit - II
Lecture 3 - Overview of VLSI Design Flow - I
Lecture 4 - Overview of VLSI Design Flow - II
Lecture 5 - Tutorial 1
Lecture 6 - Overview of VLSI Design Flow - III
Lecture 7 - Overview of VLSI Design Flow - IV
Lecture 8 - Overview of VLSI Design Flow - V
Lecture 9 - Overview of VLSI Design Flow - VI
Lecture 10 - Introduction to TCL
Lecture 11 - Hardware Modeling: Introduction to Verilog - I
Lecture 12 - Hardware Modeling: Introduction to Verilog - II
Lecture 13 - Functional Verification using Simulation
Lecture 14 - High-level synthesis using Bambu - Tutorial 3
Lecture 15 - RTL Synthesis - Part I
Lecture 16 - RTL Synthesis - Part II
Lecture 17 - Logic Optimization - Part I
Lecture 18 - Simulation-based Verification using Icarus
Lecture 19 - Logic Optimization - Part II
Lecture 20 - Logic Optimization - Part III
Lecture 21 - Formal Verification - I
Lecture 22 - Logic Synthesis using Yosys
Lecture 23 - Formal Verification - II
Lecture 24 - Formal Verification - III
Lecture 25 - Formal Verification - IV
Lecture 26 - Technology Library
Lecture 27 - Logic Optimization using Yosys
Lecture 28 - Static Timing Analysis - I
Lecture 29 - Static Timing Analysis - II

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- Lecture 30 - Static Timing Analysis - III
- Lecture 31 - Static Timing Analysis using OpenSTA
- Lecture 32 - Constraints - I
- Lecture 33 - Constraints - II
- Lecture 34 - Technology Mapping
- Lecture 35 - Timing-driven Optimization
- Lecture 36 - Technology Library and Constraints
- Lecture 37 - Power Analysis
- Lecture 38 - Power Optimization
- Lecture 39 - Basic Concepts of DFT
- Lecture 40 - Scan Design Flow
- Lecture 41 - Power Analysis using OpenSTA
- Lecture 42 - Automatic Test Pattern Generation (ATPG)
- Lecture 43 - Built-in Self Test (BIST)
- Lecture 44 - Basic Concepts for Physical Design - I
- Lecture 45 - Basic Concepts for Physical Design - II
- Lecture 46 - Installation of OpenRoad
- Lecture 47 - Chip Planning - I
- Lecture 48 - Chip Planning - II
- Lecture 49 - Placement
- Lecture 50 - Chip Planning and Placement
- Lecture 51 - Clock Tree Synthesis (CTS)
- Lecture 52 - Routing
- Lecture 53 - Post-layout Verification and Signoff
- Lecture 54 - Clock Tree Synthesis (CTS) and Routing