

Power Management Integrated Circuits
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Lecture – 71

**Designing a Zero-Cross Comparator, Inverter-Based Auto-Zeroed Comparator,
Simulation Demo**

Zero-Cross Comparator Requirements:

1. Since voltages drop across NFET is low (due to low $R_{ds,on}$), a very high gain and low offset comparator is required to detect the inductor reverse current.

For example, assuming $R_{ds,on}$ of 100 m Ω and when you have a 1 A current, then 1 mV error may cause error of 10 mA in zero current detection.

2. Comparator delay should be minimized as it may also introduce error.

Assume your comparator has zero offset. But because of the delay in the comparator, you can't turn off the bottom FET right away. Until that time your inductor will be having a reverse current and again the same problem will happen. So, this delay should be minimized, and this becomes even more challenging if you are switching at higher frequencies.

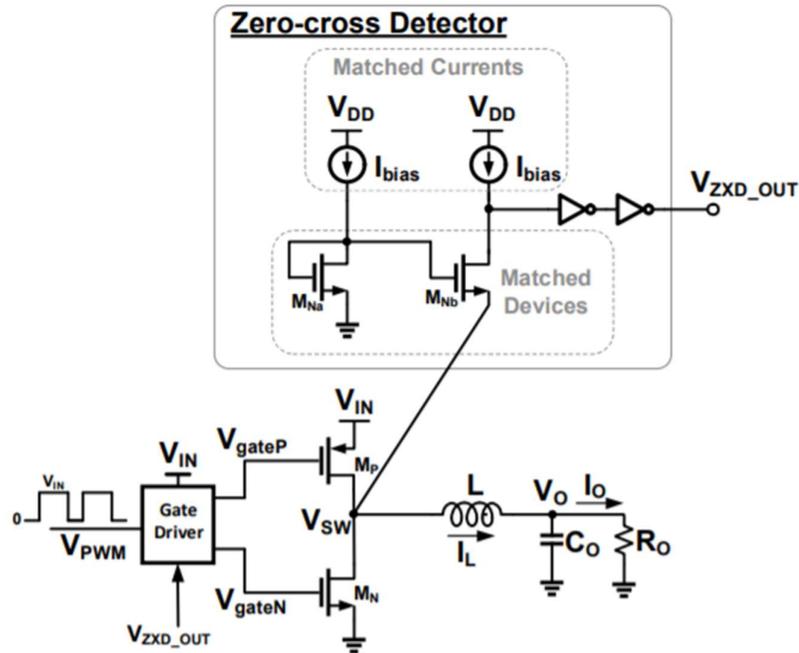
Zero-Cross Comparator Topologies:

There are different topologies you can use. Conventional two stage comparator is not suitable for zero current detection mainly due to large delay. Because more stages mean more delay.

So, high speed comparator with offset cancellation is usually required to minimize the error. And most of the time we try to use a current comparator to minimize the delay.

Current Based Zero-Cross Detector:

The circuit diagram is shown in below figure.



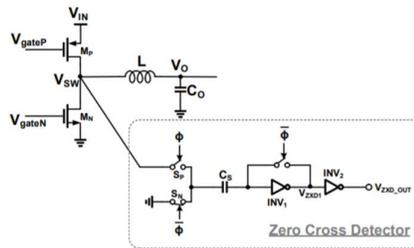
We need to detect when V_{sw} is going from negative to positive. So, when V_{sw} is negative then you are applying more V_{gs} to M_{Nb} . So, M_{Nb} will become stronger and the drain voltage of M_{Nb} will be pulled low. Now, if V_{sw} is going from negative to positive then you are reducing the V_{gs} to M_{Nb} and making it weaker and the drain voltage of M_{Nb} will be pulled high. Thus, it will detect the zero-cross. And we kept these two inverters to make the output rail to rail.

But the problem with this is you need perfect current matching and device matching. You can do a very good layout, but still there are chances of mismatch and we know that a small mismatch may introduce a large error in zero-cross detection.

So, we will go for some better topologies to do the same thing.

Inverter Based Auto-Zeroed Comparator

- When $V_{gateN}=0$, C_S is pre-charged to V_{trip} of INV_1
- When $V_{gateN}=1$, C_S samples V_{SW} node
- $V_{zxd_out}=0$ if $V_{SW} < 0$ and $V_{zxd_out}=1$ if $V_{SW} > 0$
- Any static offset is automatically cancelled
- Any variation in V_{DD} of inverter INV_1 during V_{SW} sampling introduces error



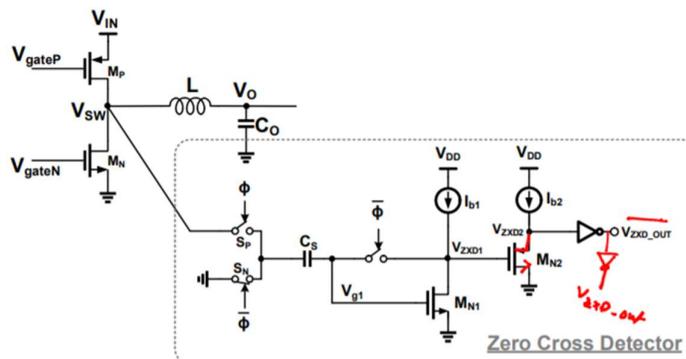
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So, Inverter can be used as comparator as shown in above figure. Φ and $\bar{\Phi}$ are non-overlap clocks. Φ is generated from V_{gateN} and $\bar{\Phi}$ is generated from V_{gateP} . So, you can say that Φ is in synchronous with V_{gateN} and $\bar{\Phi}$ is in synchronous with V_{gateP} .

The problem with the above circuit is that any variation in V_{DD} of inverter INV_1 during V_{SW} sampling introduces error. So, the circuit can be modified to get dynamic offset cancellation.

Improved Inverter Based Auto-Zeroed Comparator

- Power supply rejection is improved by using current biased inverter (I_{b1} and M_{N1}).
- Any variation in V_{DD} during V_{SW} sampling is blocked by I_{b1} hence does not affect output \rightarrow dynamic offset cancellation



Stephen W. Bryson, Using auto-zero comparator techniques to improve PWM performance, *etimes* article, 2008



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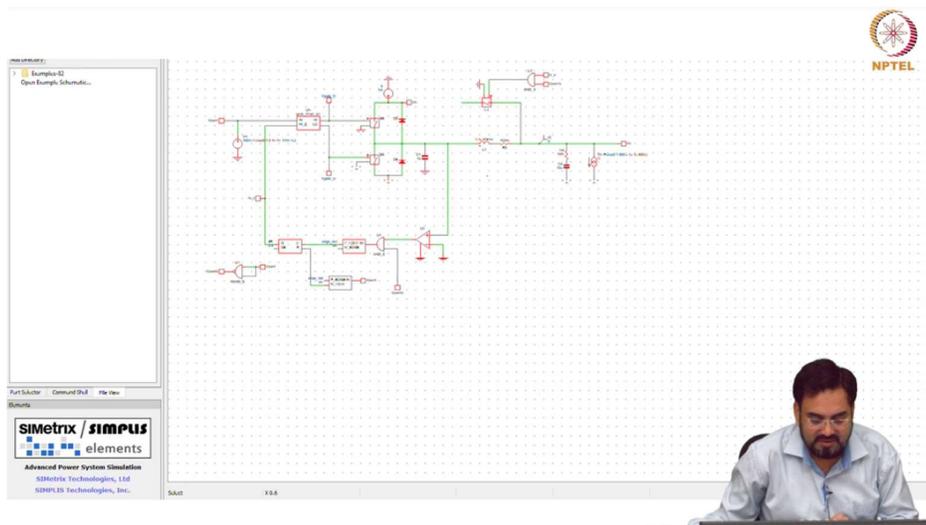
Any variation in V_{DD} during V_{SW} sampling is blocked by I_{b1} . Hence it does not affect output.

The only sensitivity will be through your R_{ds} . Since I_{b1} is in saturation, R_{ds} will be much larger. That's why for most of the current mirror circuits we use a very large channel length to reduce the channel length modulation. Or if you use a cascode, then you can make it very insensitive to V_{dd} .

So, these are some techniques to design a zero-cross comparator. And if you know any other topologies which can work with a very low offset and high speed then you can use that. But this is simpler, and another advantage is that the delay is minimized here because you have only two transistors here. But if you are using a two-stage comparator then you will have more number of transistors and every transistor will have its parasitic capacitance and increase your delay.

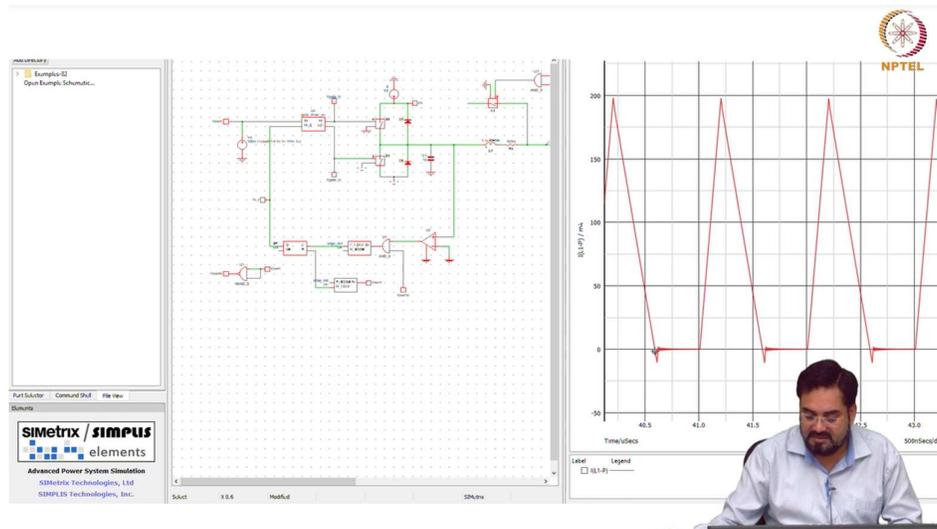
So, this zero-cross detection is the most important part of your DCM operation and you can use this zero-cross detector output to enter the DCM. In fact, you can use this output to enter PFM or PSM also.

This is a simple implementation I have to show you the DCM operation.

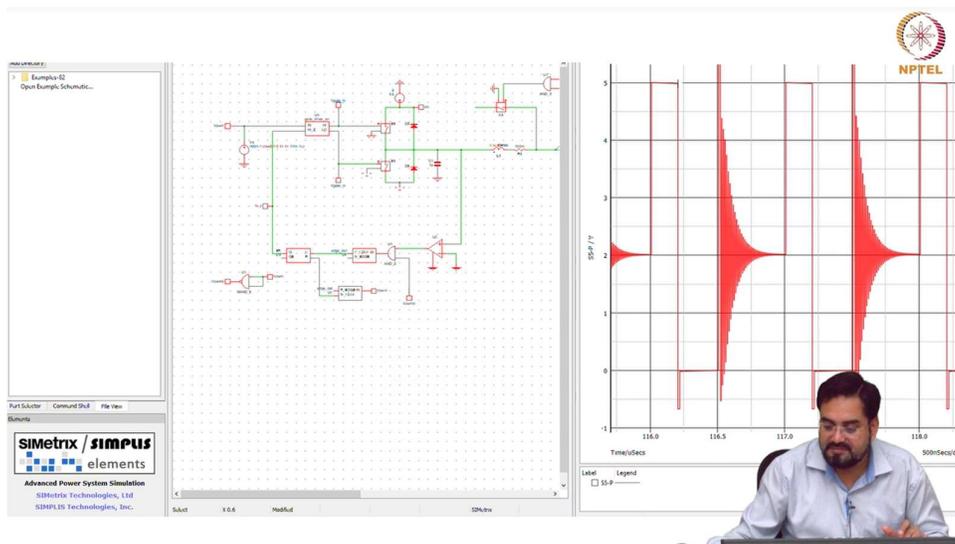


You have some parasitic capacitance at V_{sw} node, because this is connecting the drain of the two devices. So, it will have some parasitic capacitance. So, I am putting a 1 pF here. When I put this V_{sw} node at high-Z, the current will start flowing into this parasitic capacitance. And you have a LC network here. So, any LC network will have a resonance.

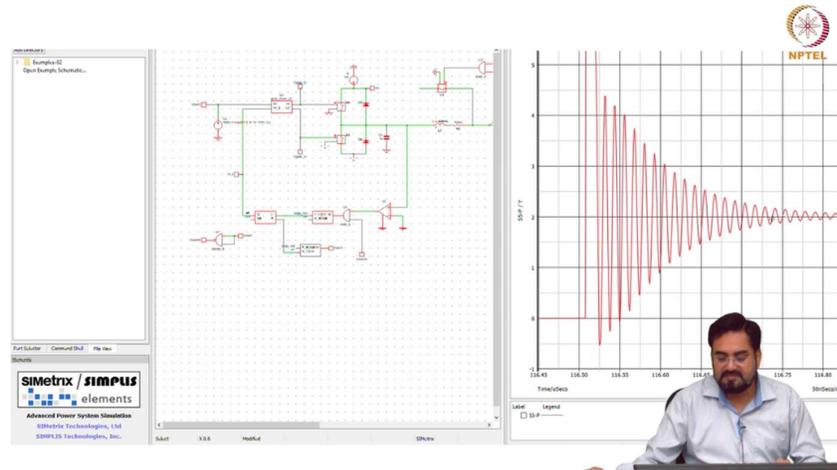
If you do not have this parasitic cap, then it will not resonate. But the moment you connect a capacitor with the inductor it has to resonate. And we know that the DCR of this inductor is not that high. So, Q will be very high, and you will see a lot of ringing at V_{sw} node. And that may cause some EMI issues.



This is my inductor current waveform and you can see that it is stopping at zero. Which means my zero-cross detector is working fine.



This is V_{sw} node waveform and your V_{sw} node has to return to the output voltage when it's a high-Z. But before it settles to the output it is ringing a lot as shown in above figure.



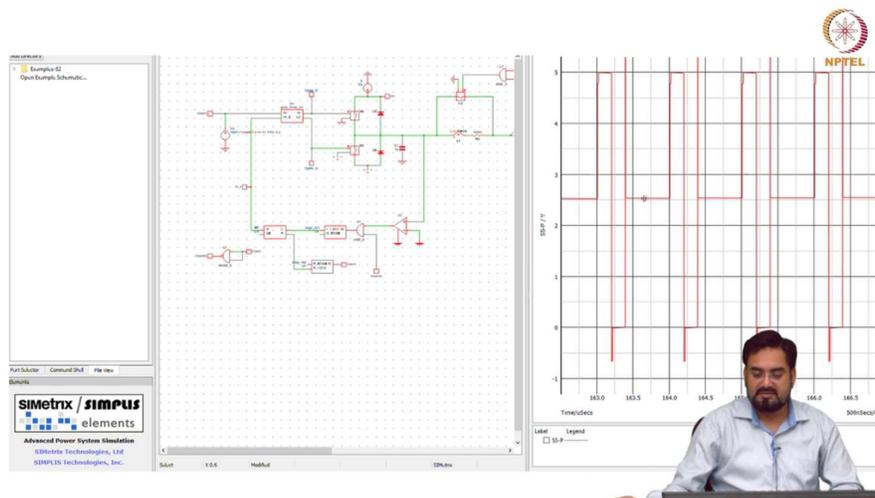
This is a zoomed version of ringing at V_{sw} . By the way, why do these LC networks resonate? Intuitively if you want to explain to anybody, the reason is inductor has stored the current and even though you turn off this bottom FET, this stored current has to be dissipated somewhere and that is dissipating in this parasitic cap and causing the resonance. And we know that as long as inductor maintains the voltage difference, the current will keep flowing through the inductor.

When the current gets reversed, this V_{sw} is at high-Z and it will try to charge to a very high voltage. When this voltage goes high then the voltage across the inductor goes positive and the inductor current will get forward and then it will try to discharge this V_{sw} node. Then again, the inductor current will try to get reversed. That is what happens actually, charging and discharging of this V_{sw} node will keep happening until your whole energy is dissipated and the voltage across inductor goes to zero.

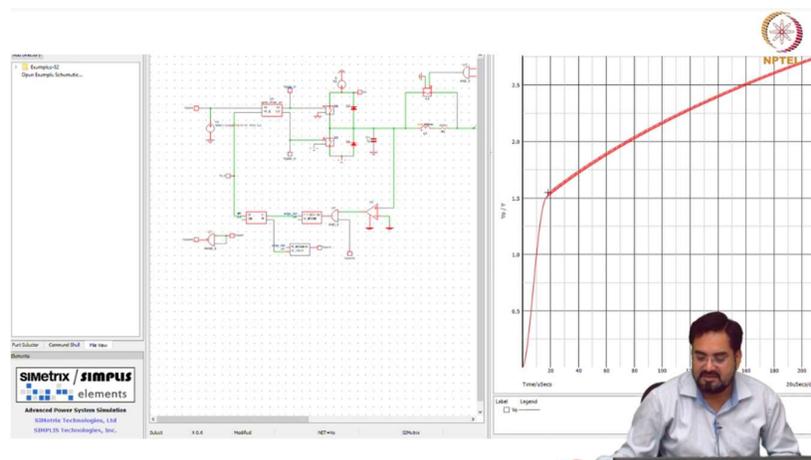
But who will limit this V_{sw} voltage? This can go anywhere because it's a high-Z. It may go even Kilo Volt. Bu the body diodes will limit this voltage. If this V_{sw} goes below -0.7 V, then this NMOS body diode will conduct and if this goes above $V_{dd} + 0.7$ V then this PMOS body diode will conduct. These body diodes will protect this V_{sw} node, and clamp this voltage between -0.7 V to $V_{dd} + 0.7$ V.

We know that when the voltage across the inductor goes zero then the energy will be zero and it will not resonate. So, if I can force the voltage across the inductor to zero then I can get rid of this ringing. If I connect a switch in parallel to the inductor it will do the same thing. The moment I detect the zero-cross, I will turn off the bottom FET and to avoid the ringing I will turn on this switch also.

So, it will short the two ends of the inductor and you are fully discharging the inductor. By the way, the name for this particular switch is “freewheeling switch.”



The simulation with freewheeling switch is shown in above figure. And we can see that no ringing at V_{sw} node and output is settled to 2.5 V. Do not think that output voltage was 2 V in the previous case, because there your output is not settled. You are operating in DCM and it will take very long time to settle the output.



You can see, output is still not settled as shown in above figure. I am looking at different time instances that is why it is still rising. In DCM it will take very long time to settle the output.

For RF applications this high frequency ringing is very bad. Even though it will not appear at the output; because it is a very high frequency ringing and your LC filter will completely filter out that. So, you may not see this at the output but at V_{sw} node you have traces and all those, which may behave like an antenna and radiate energy. So, that may cause EMI issues.