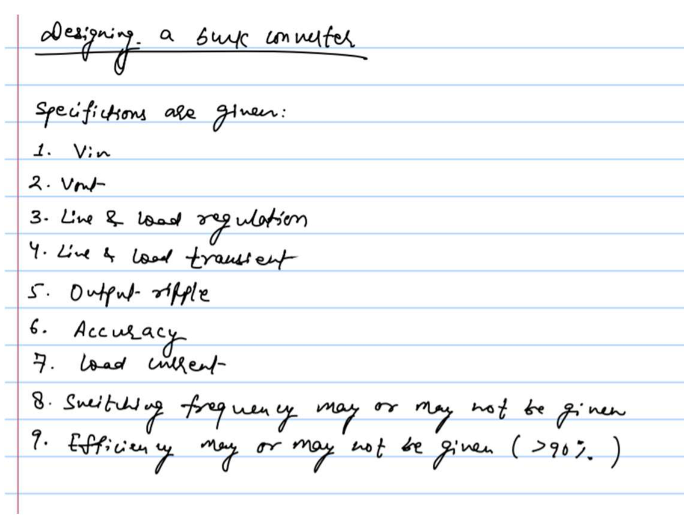
Power Management Integrated Circuits
Dr. Qadeer Ahmad Khan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture – 61
Designing a Buck Converter, Power Loss Budgeting

The way you start with designing a buck converter is first take the specifications. And then you use the ideal components for each block, and do your loop gain analysis and find all the parameters like for compensation if you are using opamp-RC, what values of R and C will require, what gain for op-amp, what kind of bandwidth you will require. And then what sort of V_m you will be looking for your ramp generator for the given range of V_{in} . And then feedback factor (β) also will come into picture if you are using g_mC compensation. Once you have finished with that, you have to start replacing each block one by one using transistor level.

There are two possibilities in a converter design. One way is like range of V_{in} and V_{out} will be given and you have to decide everything else. Other way could be like if there is already a converter design and you are looking for a replacement for the same in a different technology. In that case you can take the switching frequency, L, C values and everything from the existing design and simply port. But that is not like designing from scratch. But if you are designing from scratch then you have to decide your switching frequency, you have to decide the value of L and C before even you go into designing each block at the transistor level.

So, in this design flow we are going to learn; how you decide your switching frequency, how you choose your L and C values and after that how you start designing each block one by one based on the given specification.



So, these are the few specifications which you will be given, and you have to design DC-DC converter for those specifications. Switching frequency may or may not be given. If it is given, then it is straight forward based on the ripple voltage you choose L and C values. But if it is not given then you have to do a little bit more exercise to find out what will be the optimum switching frequency for the given voltage and the load current.

And efficiency also may or may not be given. If it is given then you size your transistors and choose the inductor with the DCR values based on the efficiency. Otherwise we usually target 90% and above.

If switching frequency is given then it is fine, if it is not given then the first thing you do is to find the optimum switching frequency. Since L and C is coupled to switching frequency, we decide L and C while finding the switching frequency. To find the switching frequency, the first thing is you need to look at the efficiency spec. If your switching losses are high, you cannot arbitrarily choose 100 MHz. Let's say at 100 MHz your switching losses are 10% and 10% you are losing in the conduction loss. So, 20% is lost and your efficiency will be 80%. In this case you can never meet 90% efficiency target, if you choose very high frequency.

These switching losses will dominate at light load and we are looking at 90% efficiency at full load. Which means out of 10% loss, theses witching losses should be negligible. So, at high load currents, you should try to keep switching losses less than 1% or so. If I am targeting efficiency greater than 90% means total loss is approximately 10%.

Let's say I am designing for V_{in} equal to 1.8 V, V_{out} equal to1.2 V and $I_{load,max}$ equal to 1 A. Which means the losses you have to calculate is at full load because I know that conduction losses (I^2R) will be maximum at 1 A.

To get 90% efficiency total loss in converter is approximately is 120 mW. It would not be exactly 120 mW; I am just calculating the 10% of the output power. The formula to get exact total loss (P_{loss}) is given by

$$P_{loss} = P_{out} \text{ x } \left(\frac{1}{\eta} - 1\right) = 1.2 \text{ x } 1 \text{ x } \left(\frac{1}{0.9} - 1\right) = 133 \text{ mW}$$

133 mW is the total loss you can incur in your converter. And this should include all losses: conduction losses, switching losses, magnetic losses and quiescent loss.

$P_{loss-total} = P_{loss-cond} + P_{loss-sw} + P_{loss-magnetic} + P_{loss-Q}$

At higher load currents.

$P_{loss-cond}$ should be dominant.

$P_{loss-cond} \geq 90\%$ of total loss.

$P_{loss-cond} \approx 120\ mW$

$P_{loss-total} - P_{loss-cond} \approx 12\ mW$

When I say switching loss ($P_{loss-sw}$), it includes all the switching losses: Gate driver loss, dead-time loss and hard switching loss.

Usually hard switching losses are dominant if you are using external powerFET because their gate cap is order of nanofarads. So, they have a larger delay. But when you are using on-chip transistors, then their delay is quite negligible.

Since we are using 180nm process for this, the delay associated with these on-chip MOSFETs is not that large. But when you use external FET, those FETs are rated for like 50 V or 60 V. So, these hard switching losses are more dominant if you are using a discrete power electronics kind of implementation, but in on-chip implementation usually those losses are not that high.

So, conduction loss ($P_{loss-cond}$) should be 90% of total loss. So, 90% of 133 mW is approximately 120 mW and left over 13 mW should include all other losses.