Lecture – 23
Output Impedance of PMOS LDO

- Two-Pole Model used to find the Output Impedance:
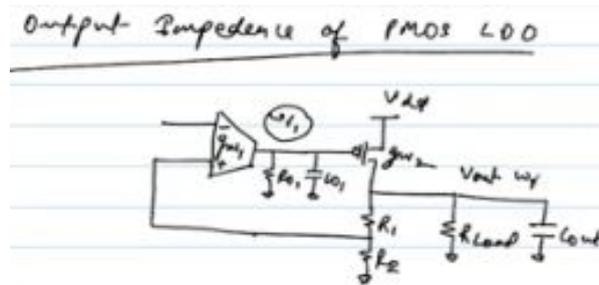
- Approximate expression of Z_{out} (s) at frequencies $\omega < \omega_{ugb}$ and the corresponding magnitude plot (error amplifier pole ω_{p1} is dominant):
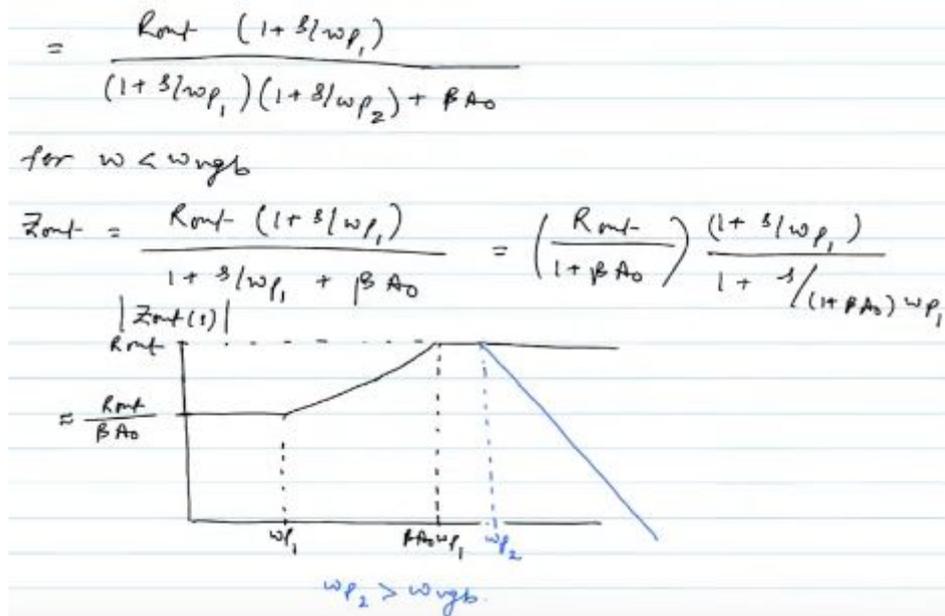
  - The output impedance of the LDO is R_{out} divided by one plus the DC loop gain at frequencies $\omega < \omega_{p1}$.
  - Beyond ω_{p1}, the impedance of C_{o1} begins to decrease until it becomes a short-circuit to ground at $\omega_u = \beta A_0 \omega_{p1}$.
  - Beyond ω_u or ω_{ugb}, there is no feedback and the loop is dead (i.e. the loop gain is negligible) so the output impedance is R_{out} itself. (Feedback at frequencies less than ω_{ugb} helps to reduce the output impedance.)
  - Beyond ω_{p2}, the impedance of C_{out} begins to decrease, so Z_{out} falls as well.

- When the error amplifier pole is dominant, the only way to improve the load transient response is to push the peaking near ω_u to higher frequencies, i.e. to increase the bandwidth by increasing g_m, which comes at the cost of burning a higher quiescent current I_Q.

- The output impedance of the LDO at DC is known as its load regulation and is given by $R_{out}/(1 + DC\_loop\_gain)$. This means that increasing the DC loop gain improves the load regulation.

- Magnitude plot of $Z_{out}(s)$ when the output pole ω_{p2} is dominant:
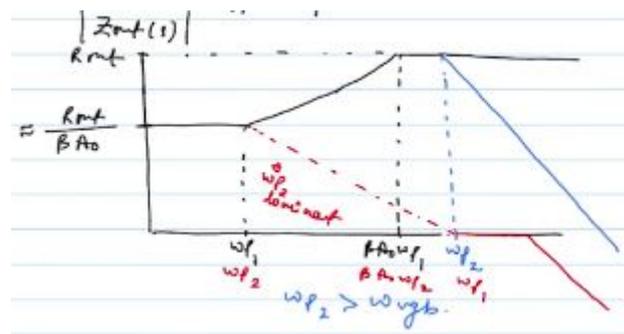
- The output impedance of the LDO is the load regulation (R_{out} divided by one plus the DC loop gain) at frequencies $\omega < \beta A_0 \omega_{p2}$, i.e. at frequencies $\omega < \omega_u$.
- The zero at ω_{p1} cancels with the non-dominant error amplifier pole ω_{p1}.
- Beyond ω_u, there is no feedback and the loop is dead but Z_{out} still falls in the absence of feedback because the impedance of C_{out} begins to decrease beyond ω_{p2}.
- Thus, when the output pole is dominant, the LDO output impedance is always non-increasing, i.e. it never increases beyond the load regulation $R_{out}/(1 + DC\_loop\_gain)$ as is the case when the error amplifier pole is dominant.
- The response to load transients is very good when the output pole is dominant since Z_{out} is low at all frequencies. The PSRR is better as well, when the output pole is dominant.
- Increasing C_{out} will reduce the bandwidth ω_u but it will improve the load transient response when the output pole is dominant because Z_{out} will begin falling off at lower frequencies (the output capacitor C_{out} would sink/source fast transient currents).
- However, increasing C_{out} does not improve the load transient response when the error amplifier pole is dominant, since it does not increase the bandwidth.