

Digital IC Design
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Lecture – 36
Logic Gate Capacitance

So, now let us move on to the idea of estimating the delay of these gates right. I want to ultimately use this gate to either again charge a capacitance or discharge a capacitance like I have told you many times that is the only purpose of this course; how fast can I charge how fast can I discharge. So, we have to estimate these delays given that we are now had different kinds of sizing that is happening there right. So, for that first we have to estimate the capacitance on these arbitrary gates ok.

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CAPACITANCE

ALL CAPS SCALE AS $\propto W$

$C_{gn} = C_{gp}$

ASSUMPTIONS:

- 1) LUMP ALL CAPS.
- 2) ALL CAPS TO AC GND
- 3) ALL CAPS ARE EQUAL

C → GATE CAP OF A UNIT NMOS DEVICE

So, let us look at the capacitance. Let us start with our inverters maybe I should draw this bigger because I need to put lot of caps there ok. I am let me also draw the body node this is connected to V_{DD} , this is connected to ground.

Now, what are the capacitances for this inverter? Yeah. So, basically from gate to source there is one capacitance, right this is the C_{gsn} , then from gate to drain there is one more capacitance C_{gdn} right, then there is one capacitance like this C_{dbn} right, C_{sdn} right and then there is also a C_{gdn} .

Similarly, I have capacitances on my PMOS transistor as well; same number of capacitances ok. The only difference is because this is size 1 and this is size 2, the capacitance now will become twice; remember, all the capacitances that we derived scale linearly with W , that was our primary conclusion from that module right.

So, let me put that down explicitly all caps scale as proportional to W . Therefore, you will have if the unit capacitance for a PMOS transistor that is a PMOS transistor with width 1 is C_{gsp} then this will be $2C_{gsp}$ right and actually there is nothing to choose between these two between the NMOS and PMOS.

So, all if the C_{gs} is C_g C_{gs} for the NMOS, then if the same width I use for the PMOS and that is also C_g . There is no big difference there if you remember; just because there are holes there the capacitances do not change right. So, let me just write that down this is $2C_{gdp}$ right then I have this C_g no C_{dbp} and C_{sdp} twice all this should be twice and yeah?

Student: (Refer Time: 04:37).

Correct, you are right. I am just saying I have just called C_{gsp} I will now say C_{gsn} equals C_{gsp} right. I am just marking it differently. So, the first thing to do is these capacitances there are too many capacitances here right. So, for our first order back of the envelope calculations we do not need these many capacitances there. In the sense I am not worried if

the value of C_{gd} and C_{db} are slightly different. The fact is both of them scale linearly with W .

So, first assumption I am going to make is assumption 1; I will lump all caps first what I mean is this C_{gd} right, I can I am simply going to make it a single gate capacitance. Ideally you have to break it up as a miller capacitance part here part there and all that you can add all of them I am saying break everything and simply get a capacitance like this on the NMOS transistor. Similarly, for the PMOS transistor I am going to get one capacitance I will put the values there now right.

This C_{sb} is useless because it is connected between ground and ground. So, I can neglect that capacitance, similarly I can neglect this capacitance right. Now, this C_{sbp} is going to V_{DD} , but that is like an ac ground right. So, therefore, I am going to bring all the capacitances to ground all caps to AC ground. So, what happens is my NMOS transistor now has one capacitance, similarly the PMOS transistor has another capacitance.

Now, we are going to make the biggest assumption which will make you question why we did all those calculations in module 1. We are going to assume that the C_g , C_{gd} and C_{db} are basically of equal magnitude. You go back and look at the calculations that you did the capacitances are lot of by lot.

So, third assumption is all caps are equal which implies this is C , this is also C . Of course, this is size 1, this is size 2; therefore, this is $2C$ and this is $2C$ ok. Go back and check your calculations the drain to body capacitance would not be very very different from the gate capacitance, net gate capacitance that we got right. And, the primary point is since all of them scaled with W my error is not cascading. It is not like I have a larger error if I do larger W right they all scale well and it is reasonably accurate there.

In reality of course, if you run it in a simulator you will get a slight difference, but that is not for us to worry in this the theory part because the inferences we are going to make from this

calculations that we are going to do will still be consistent with the assumptions that we are making here.

So, net thing I can do is take an inverter and simply write it as a sum of two capacitances this is $3C$ (Refer Time: 09:00) all right I want to put a capacitance, $3C$ and this is also $3C$ where C is basically the gate capacitance of a unit transistors NMOS transistor. This is C net gate capacitances of a unit NMOS transistors that is what the C is ok. And, of course, which also equal to drain capacitance by this assumption clear ok.

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UNCONTACTED SHARED DIFFUSION
=> DO NOT DOUBLE COUNT CAP

Question - Why did you neglect the capacitance of the bottom NMOS transistor at the source but consider it for the top transistor?

Now, I want to take this understanding and identify what the capacitances are for a NAND2 gate ok. So, let us look at this Y right. So, what do I have at the gate of each transistor? I have a capacitance, at the drain of each transistor I would have a capacitance right and maybe at the

source also depending on whether resources grounded or not I will have to put a capacitance there as well.

So, let us now go ahead and mark these capacitances. I have a cap here right; I have a cap here, then I have a cap between the drain and ground for the PMOS. I have the cap between this drain and ground for this PMOS. So, sizes by the way are 2, 2, 2 right. So, what are the capacitance is now in terms of C ? All of them are $2C$. So, this is $2C$, $2C$, $2C$ and $2C$ ok.

I will now draw this NMOS stack separately so that it becomes clear output Y this is 2, 2. So, what is my gate capacitance? Yeah? $2C$. What is this capacitance? $2C$, right. Now, I am going to put one gate capacitance drain capacitance here $2c$, right. The source of let me call it N_1 , N_2 right there is sizes. The source of N_2 is going to have a capacitance of yeah $2C$ again right wherever you have a node you got a put a capacitance and scale it by the width. The drain of N_1 will have a capacitance of $2C$.

So, what is the net capacitance here? Yeah? No, Not forget the PMOS I am talking only of the NMOS $2C$ right. What is the net capacitance here? $4C$ and I have $2C$, $2C$ ok. Now, here is a slight trick that we will use from the layout wherein this intermediate capacitance is not going to be $4C$, it will actually be only $2C$ ok. I will tell you why and this will also help you do the layout for your NAND gate that is your part of the assignment ok. I was asked not to use this green right? Green is not visible from behind, is it? Magenta is not? Ok I will use blue ok? What about this green? Yeah, is this visible? Ok good. So, yes let me ok.

So, what I am going to do is I am going to now go to the layout of these two of this NAND gate ok. So, I have a width of $2W$ here and I have two gates right. These are my two NMOS transistors which are in series. So, this will basically be my (Refer Time: 14:23) I should just put a metal 1 here ground and I will connect this to ground ok. There are appropriate contacts and all that. So, this is basically nothing, but my series stack from the output Y to ground. So, these are my inputs A and B . So, the gates are going to be connected to inputs A and B ; A , B .

Similarly, I have a PMOS this thing, but now this PMOS is going to be in parallel right. So, sorry, I got it yeah. So, what do I do I am going to simply extend this gate all the way and if

you remember it is not possible to bring these two transistors PMOS and NMOS very close because there is a well spacing problem right. Remember, this PMOS is actually sitting in a N well and the NMOS is sitting in a P well right, this is my N well.

So, now I have my V DD line which is sitting here V DD. So, now, what am I; what am I going to do I am going to construct this parallel PMOS stack right and take it up to V DD right. So, what do I do? I am going to simply connect this guy to V DD, this guy to V DD, this intermediate node that is there is going to become my output node Y. This diffusion is actually this particular diffusion here right. This thing is actually my output Y and this is my output Y right. If this is node X, then this is my node X right.

So, then I have to do something else I have to basically now draw metals and short my output like this. This is how you have to do the layout for your assignment also on similar lines, clear?

So, now we will look at the capacitance terms that are coming right. If I had this guy as two separate transistors what would I have done? I would have basically made it one NMOS transistor, another NMOS transistor right, then and I would have put two gate here and I would have put two metals, sorry I would have connected it through a metal M 1. This is what I would have done if I wanted to keep these as two separate transistors, but now these transistors share a diffusion. Diffusion is basically my n plus right they share that diffusion and also there is no contact on that.

What do I mean by contact? It means that this node X is not available to the outside world. You can access Y, you can access A and B, you cannot access X from outside which means there is no contact that is made and therefore, I do not need to give any minimum spacing between these two diffusions. I can pull the transistors very very very close right. Therefore, this distance I can simply remove this whole metal thing right and move the transistor as sorry move the transistor as close as I can to it and draw my gate ok.

Remember, that when we spoke about the things that we just undo this so that we can use the previous. Remember that when we derived the capacitance of the drain and source we were

actually looking at this cross-sectional area and that is why we got a C we got a capacitance of C from here, a capacitance of C from here and if it is of course, W is higher than it is 2 into C and therefore, we said it has to be $4C$ in that diagram. But, now if I bring these two diffusions so close it is effectively like just one diffusion, you get it? That is the idea that we are using.

So, if you look at the picture of the transistor itself, it would be something like this N plus N plus my gate, this N plus will be shared. So, my other N plus will come here and this will be my gate. So, instead of having 4 N plus diffusions for 2 transistors I will have only 3 diffusions for 2 transistors. The reason is it is not just that it is shared the diffusion is also uncontacted.

For example, I can ask you even the PMOS the diffusion is shared right. If you look at this thing the diffusion is shorted the diffusion is shorted here the difference is I need to put a metal contact here because I need to put a metal contact I need spacing and therefore, I have to keep the transistors far apart and therefore, the capacitance is like each transistor will contribute to its capacitance.

So, the golden rule is if it is an uncontacted shared diffusion then you do not double count the capacitance right. So, here this is a an uncontact contacted shared diffusion and therefore, implies do not double count cap.

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Question - Isn't there capacitance between the GATE and DRAIN terminals?

Therefore, I will redraw my NAND gate with the net capacitances is as follows. Inputs are shorted, I have one capacitance between A and ground other capacitance between B and ground. How much is the net capacitance on A and B gate? On each input what is the total capacitance? Yeah? $4C$ right, each transistor gave me $2C$ because the widths are 2 each net capacitance is $4C$, ok.

On this output node what is my total capacitance PMOS plus NMOS $6C$ right because it is $2C$ from each PMOS transistor because it is a shared diffusion, but a contacted diffusion and therefore, it is $2C$ from each PMOS transistor and $2C$ from the top NMOS transistor, so this is $6C$. And what is the intermediate capacitance? It is $2C$ ok. Any questions here?

This if you do not look at the layout and the physical picture you will not get this idea of uncontacted contacted shared diffusion ok, but luckily you are going to do it in your

assignment now, you will see it for yourself. You can try it and see right you just see for the PMOS transistor how much space you need, you have to keep it far apart. Therefore, the diffusion will be large it will be like two diffusions NMOS you can bring it really close without any DRC violation, that is the idea right.

Any questions here? No, where? Oh yeah. See for the inverter the bottom transistor source was shorted to the body, both are connected to ground. See the reason is if you look at this NMOS stack here this guys body is grounded; this guys body is grounded, but the source is not. Therefore, I have to bring in that capacitance there. Only because in an inverter source and body will ground it I could remove that capacitance out of the picture there is a capacitance yeah. So, that is what I told you. So, that becomes like a capacitance between the input and output now that you have to do miller capacitance and split it as you know this thing.

So, I am saying you lump all of them. Effectively it is like one C here and the drain also has the same C. Correct, yeah. Any other questions? Yeah there is you can bring it as close as you can, effectively it will be like one diffusion that is all. You see you try it in the layout and see you know. So, then we will stop here, we will continue on Monday.

Thank you.