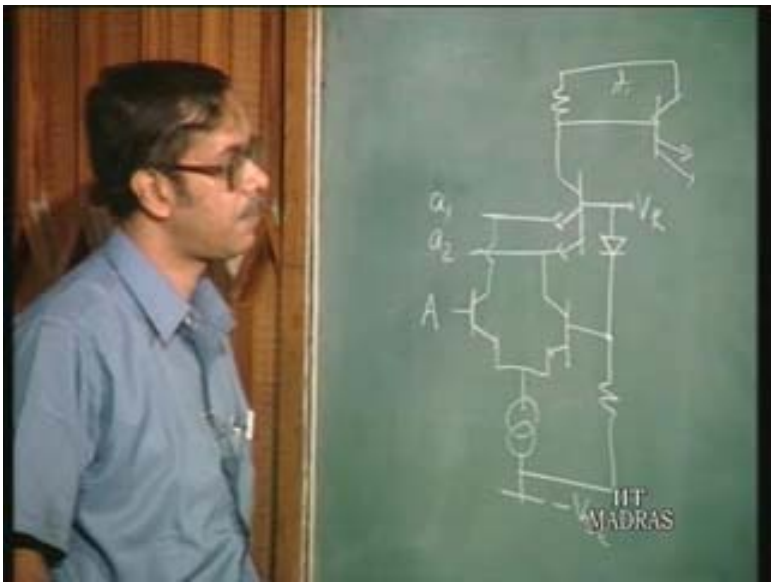
Digital Integrated Circuits
Dr. Amitava Dasgupta
Department of Electrical Engineering
Indian Institute of Technology, Madras
Lecture - 21
Emitter function logic;
Low power ECL;
Current mirror control logic

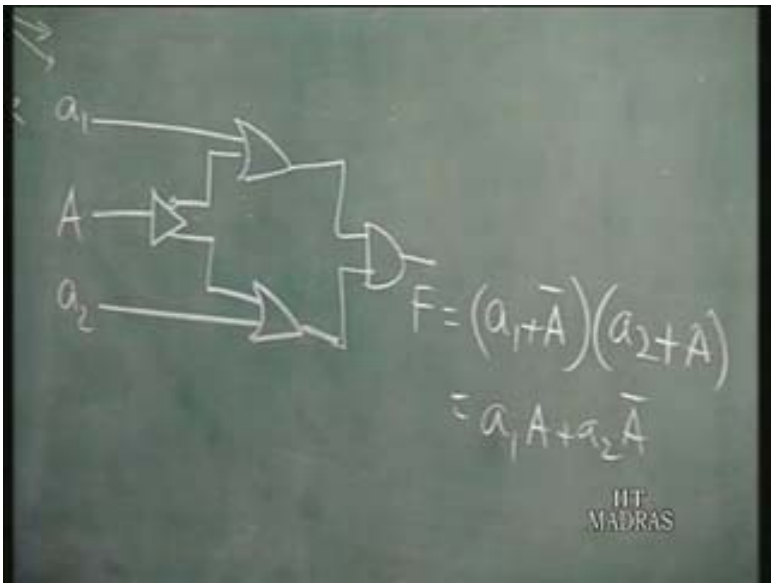
Last class we were discussing the emitter function logic which is a variation of the emitter coupled logic and we have seen that the functionality is tremendously over the emitter coupled logic in the sense that with the same power dissipation, you can realize logic circuits of much greater complexity. So effectively you are reducing the power dissipation. So we shall continue our discussion on the emitter function logic and we will take up again the basic circuit of the emitter function logic which is something like this.

(Refer Slide Time: 00:02:35)



You have multi emitter transistor, the output side and then you have the emitter coupled structure here, the current source, this is minus V_{EE}, this is ground and here this is V_R then you have a level shifting arrangement. So this is V_R - V_{on} and you have the inputs, this is A and this is small a_1 and small a_2. The capital a is actually called the control input, these inputs here at the base of this transistor is called the control input whereas these inputs small a_1 and a_2 are called the direct inputs. That is the name of this and the circuit configuration is like this. So you have the control input here, you have the OR gate, you have a_1, a_2 and like this. (Refer Slide Time: 00:03:02). So f is equal to a_1 plus a bar a_2 plus a which can be written as a_1 a plus a_2 a bar.

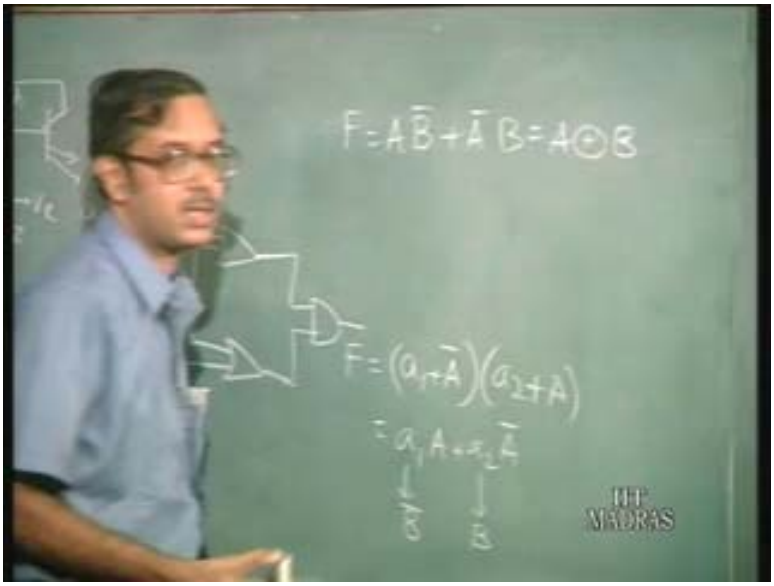
(Refer Slide Time: 00:03:16)



So we have seen this and so this is the logic we achieve and we have also seen that we can increase that complexity by instead of having an inverter structure here, you can have a nor structure that is if you have more transistors in parallel that is more number of control inputs, you can increase the complexity that way.

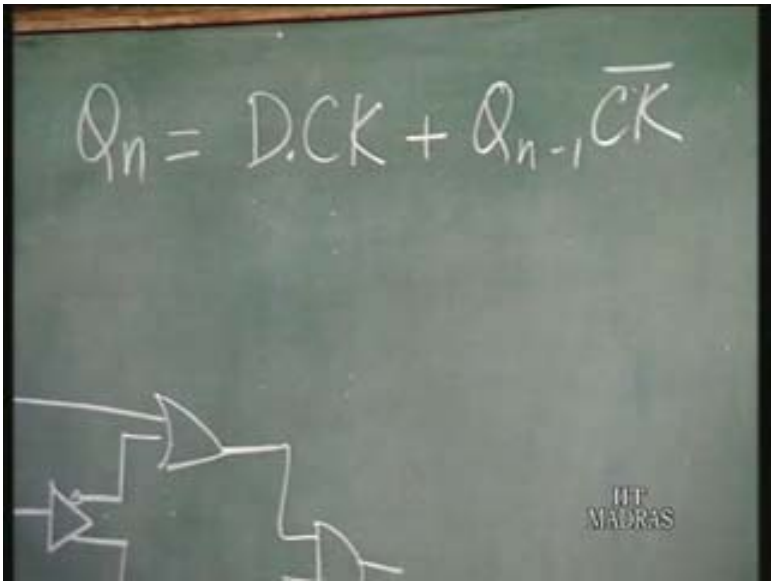
Now let us see we will just take up a few examples of circuits. One is the exclusive or which I think we have already discussed in the last class. That is if a_1 input is taken as b bar and a_2 input is taken as b, when you get the f as a b bar plus a bar b which is the exclusive OR gate.

(Refer Slide Time: 00:04:24)



So you can realize the exclusive or gate by providing b bar at the a_1 input here and b at the a input. The next thing which we can take up is the d flip flop which is a very important circuit when we go for any synchronous logic circuits, you have to have flip flop. So let us see how you can realize a d flip flop. What is a function of a D flip flop? The D flip flop function is that when the clock is high whatever is the value at d should be passed on to the output and when the clock is low whatever was the previous output should be retained. So we can write like this Q_n is equal to D into clock plus Q_{n-1} clock bar.

(Refer Slide Time: 00:05:09)

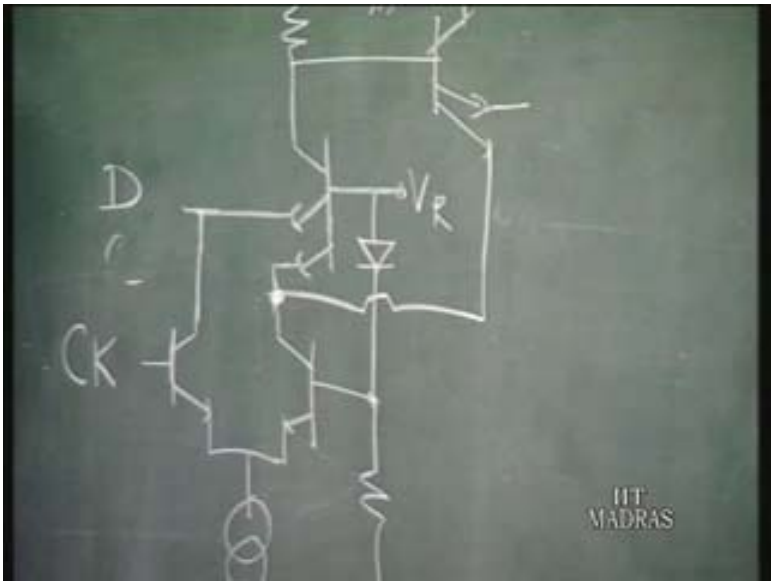


That is when the clock is high that is clock is 1, clock bar is obviously 0. So when clock is high Q_n is equal to D so whatever is the D input is the same as Q_n and when

clock is low that is this clock is 0, clock bar is high then whatever is the Q_{n-1} is the same, the Q_n is equal to Q_{n-1}. That the previous output is retained basically Q_{n-1} is equal to Q_n. Now when you compare this with the standard function which is realized in a D flip flop, you see it is quiet similar. So what you have to do is the clock input must come as the control input here, a should become the clock and in one case the small a_1 can be D and the other one should be Q_{n-1}. So if you do that you will realize the d flip flop.

So I shall just draw the circuit or I can just modify the circuit here maybe on the blackboard. Come back to this circuit, so here instead of A you have clock and then small a one is going to be D. When clock is high, Q_n is d and when clock is low that is the output is equal to Q_n bar, the previous value of Q_n.

(Refer Slide Time: 00:07:41)



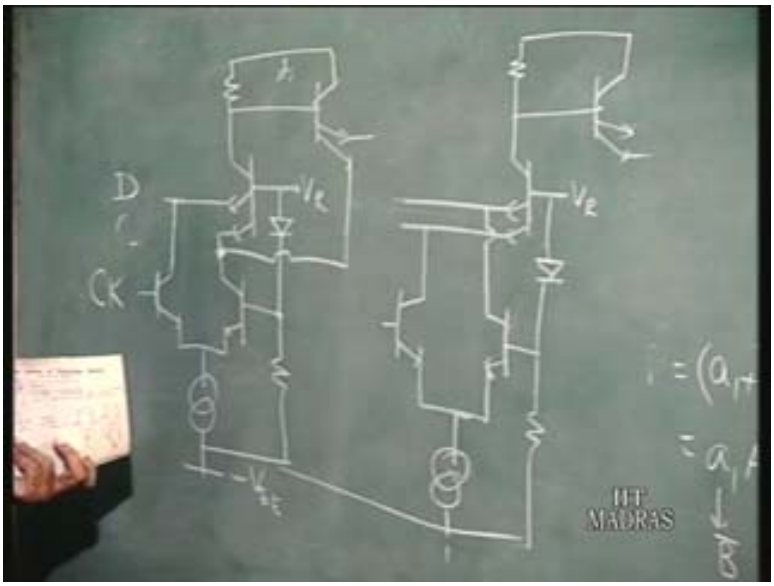
So here for small a_2 you must feed the previous value of the Q_n. So what you do, you take the one output here and it must be fed back here. There is always a feedback in a flip flop, so this is the feedback. So the output comes from here, whatever is the previous output is fed here. So when clock is low then the next output is going to be the same as the previous output. So this completes the D flip flop.

So you see that this is the circuit of a D flip flop then again the power dissipation corresponds to that of a single gate. You have a single current source here and of

course you can realize a master slave D flip flop. How do you do that? You have to have a similar gate, I will just draw it because it gives completeness. So you have a similar gate, I am just drawing a similar gate, this minus V_{EE} is drawn here, this is V_R and then you have this. Now here is the output so you have a similar gate means but the only difference being that the clock is going to be inverted. So what you do is this V_R for this first gate. So basically the clock what I should do now is I think I will remove this.

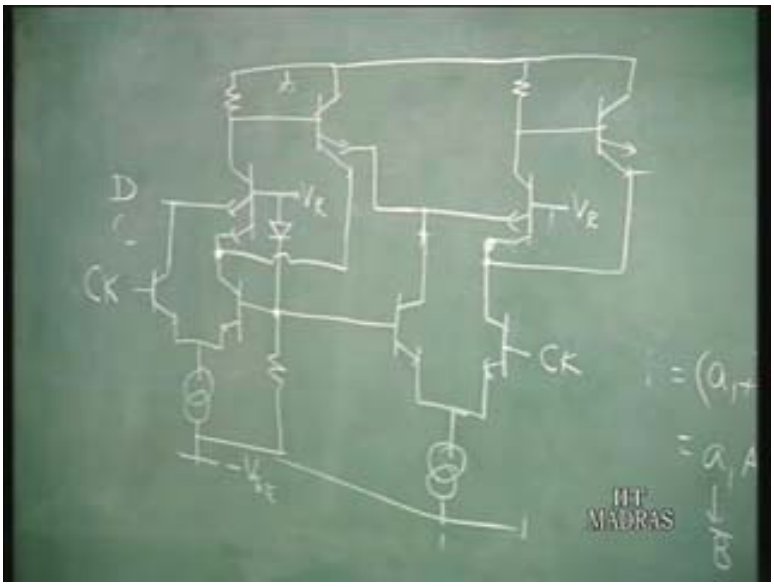
This clock, this V_R should be fed here and the clock should come here, the same clock. So basically I have inverted that position of the clock and V_R, so this V_R comes here same and the clock. So now here you have the D input as in the previous case. So this goes the D input and here you have... so this is the circuit (refer slide time: 00:09:54). So this completes the circuit for a master slave D flip flop.

(Refer Slide Time: 00:08:41)



So we have two stages and the difference between the two stages is that in the second stage the position of the clock and the reference voltage is reversed. So this is the circuit of a master slave D flip flop. So you see that again what is important here is that we have achieved it with lot of saving in power supply in power dissipation.

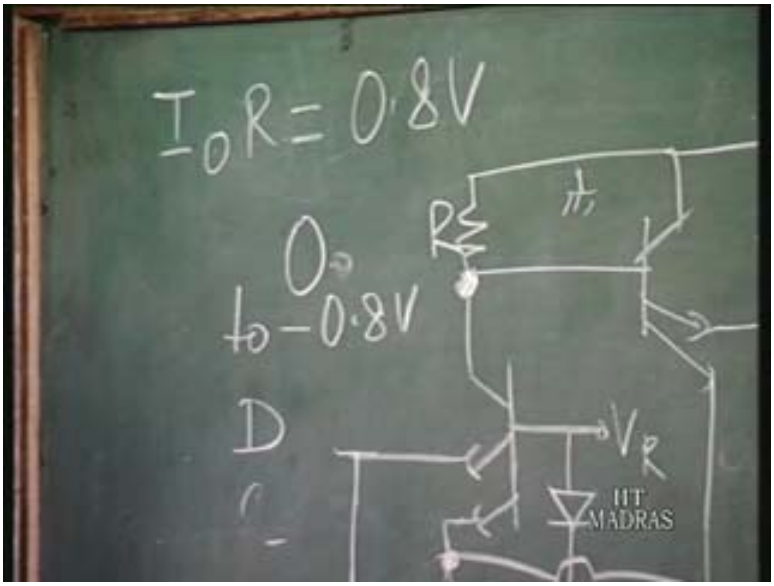
(Refer Slide Time: 00:09:59)



Now after this only one issue which we have not really taken up is that we have to see whether this particular circuit satisfies the voltage compatibility requirement that is what is the voltages, what is the reference voltage? So we have seen for ECL gate that reference voltage must be equal to minus 3 by 2 V_{on} or so on and so forth. So what is it going to be here and whether it satisfies the requirements? So now let us assume for example that I_0 into R is equal to 0.8 volt. That is the current source value I_0 into the resistance R is equal to 0.8 volts.

So the voltage here at this node can either be 0 volts if this transistor is not conducting or it can be minus 0.8 volts. So here it can either be 0 or the voltage variation is we shall write 0 to minus 0.8 volts. This voltage variation at this particular node. What is the output voltage variation, what is the output voltage drop?

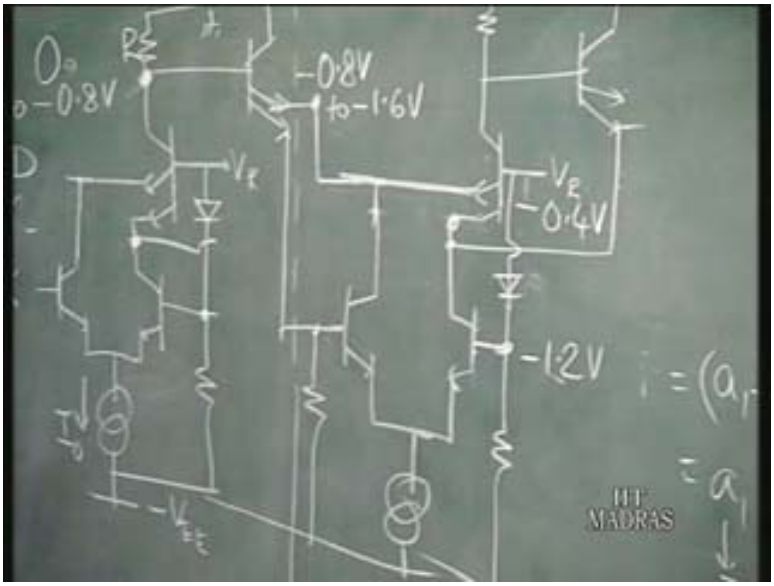
(Refer Slide Time: 00:12:06)



So if we assume that the v_{BE} of this transistor is 0.8 volts so the output voltage varies from minus 0.8 to minus 1.6 volts. Now the v_R of this circuit let us choose it to be minus 0.4 volts and so v_R - v_{on} is going to be again minus 1.2 volts. For the lower part of the stack say here let us draw, suppose I think we will take a different circuit. Let us have the normal configuration. Here you have a diode drop and the resistance. This reference voltage is going to be minus 1.2 volts.

Let us say that the output of the first stage is going to be fed, it can be fed either as input here as a control input, as a direct input or as a control input. So let us see if the voltage requirements are satisfied. When the output of a particular gate so this is the gate one is fed as a direct input here what happens? Now you have again an emitter coupled structure here. This transistor that is the output transistor of gate one and this transistor form an emitter coupled structure.

(Refer Slide Time: 00:15:27)



The emitters are shorted here and this input here is minus 0.4 volts and the input at the base of this transistor is varying from 0 to minus 0.8 volts. What we are having is a variation of this $v_{R.}$ plus minus 0.4 volts at the base here. If this voltage here you see is 0 volts, what happens? This transistor is on and this transistor is off. We have said already that if the input is high then this transistor is off. So between this, there is a perfect voltage compatibility. You can feed this output directly as a direct input here without any level shifting necessary because this voltage varies about the reference voltage here and suppose we have another input and you feed it directly here.

Actually you must have a resistance connected here at the base (Refer Slide Time: 15:31). Now suppose you feed it here directly at the base, now what happens? You see this voltage here is minus 1.2 volts. So this again is an emitter coupled structure, this transistor and these two transistors say $t_{1.}$ and $t_{2.}$ they form an emitter coupled structure. The base of $t_{1.}$ is minus 1.2 volts and what is at the base of $t_{1.}$? The variation is minus 0.8 to minus 1.6. So if this is minus 0.8, $t_{1.}$ will be on. If it is minus 1.6 $t_{2.}$ will be on.

So again you see that there is perfect voltage compatibility that is what you want to say is that the output of an EFL gate from this multi emitter transistor can be fed directly either as direct input here or as a control input here without the need for any level shifting. There is no level shifting required that you can feed it either to this level or to this level because they are perfectly compatible. They form emitter coupled structures here as one can see or one can see where the input here at the base of one transistor swings about the reference voltage. If this input is high, this $t_{1.}$ is on. If this input is low, $t_{2.}$ is off.

Similarly if here this emitter coupled structure, if this is high that is 0 volts then this one is on which means automatically this one is off and if this goes to minus 0.8 then this one is off and this one turns on.

So you see that there is no problem from the voltage compatibility point of view. So EFL circuit does not require any level shifting, although you have a stack structure as you know here that is the important thing because level shifting again would mean that you require additional circuitry. So we have gone through this emitter functional logic which again as repeat, a variation of the emitter coupled logic and the advantage is greater functionality and you can achieve more complicated functions to the same power dissipation. That is one of the circuits which have been proposed in fact this was proposed way back in early seventies. Then that is also been a lot of work going on even further because the problem is ECL gate is a very high speed circuit. It is in fact offers the highest speed but it is still difficult to make large scale integration because it is still very much power intensive. there is lot of power dissipation and so you cannot make very large very highly dense circuits and so even with these concepts it is still power dissipation is high and so people have tried to work out more advanced circuit concepts to reduce the power dissipation.

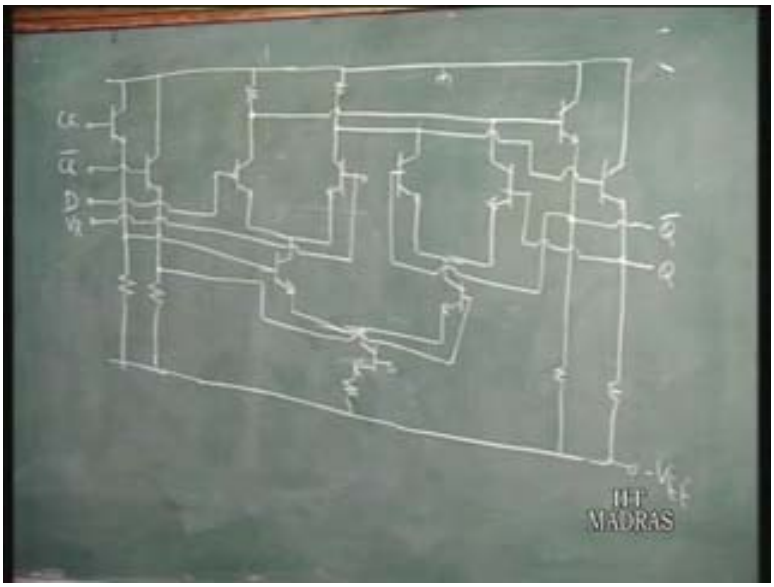
The one aspect people have been working on is to reduce the power supply voltage that is another advantage. See if you reduce the power supply voltage, you automatically reduce power dissipation and in today's world there is also been drive to achieve lower and lower power dissipation also because of the fact maybe you want lot of handed equipment which can operate with standard battery cells and all so on and so forth. Maybe 1.5 volts people are talking of, all circuits should work with that voltage.

Anyway so there has been a drive to reduce the power supply voltage with which automatically means you reduce the power dissipation. I shall take a one more variation of the ECL family which has been proposed very recently in fact, it was first published in 1997. In fact claims that it provides the lowest power delay product, if among circuits working in the gigahertz range.

So I shall just slowly introduce that particular concept. So I shall draw the circuits in fact which I had drawn last class that is the standard ECL D flip flop circuit and we shall see how one can actually go ahead and see the difference. So this is the standard D flip flop circuit using stacked ECL gates. So you have two sets of emitter coupled transistors and here you have in the lowest stack another emitter coupled structure and here you have a current source and here are the clock inputs, clock and clock bar and so here you have one is the D input and the other is the reference voltage V_R.

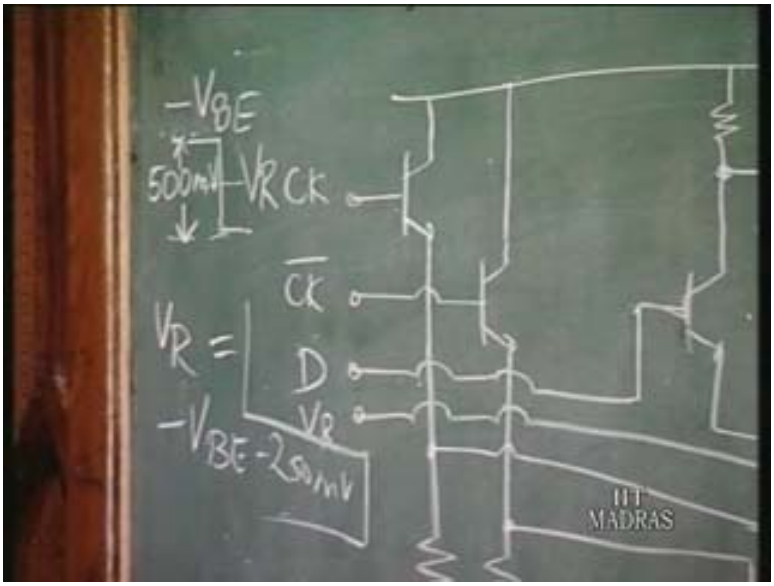
One of the inputs goes here and the other input goes here clock bar. So here clock and other is clock bar, here you have D and V_R reference voltage and here you have say this one going here, this one going here and then these outputs again go to emitter follower and you have one more emitter follower here. This is minus V_{EE} supply voltage and so this is D, this is Q bar and so this you have is Q bar, this is Q and the Q bar input should come here and the Q input goes here. So this is the circuit which we have already discussed, the D flip flop circuit here. So now let us see what is the power

supply requirement for this circuit? In this standard circuit, the input voltage variation between say clock or any of the inputs it varies from minus v_{BE} that is the high value here and say suppose you have the voltage swing say 500 millivolts.
(Refer Slide Time: 00:23:25)

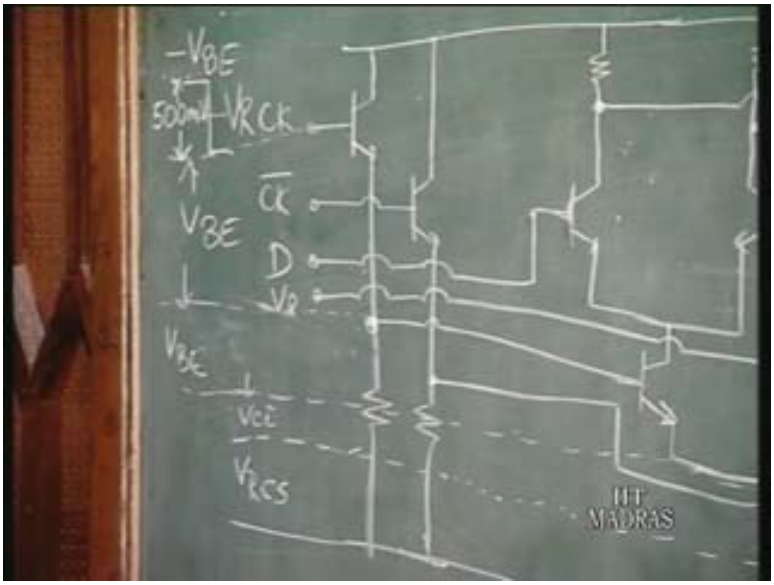


So usually in high speed circuits, the voltage swing will be limited. So it's not full von, so its 500 millivolts, you know that the power delay product will depend on the logic swing. So we limit it to say 500 millivolts. So this is 500 millivolts so input as well as the output voltage should vary from minus v_{BE} to minus 500 millivolts and the reference voltage is centered about that variation. That is v_R will be in this case minus v_{BE} minus 250 millivolts. So this v_R is equal to minus v_{BE} minus 250 millivolts.

(Refer Slide Time: 00:24:57)



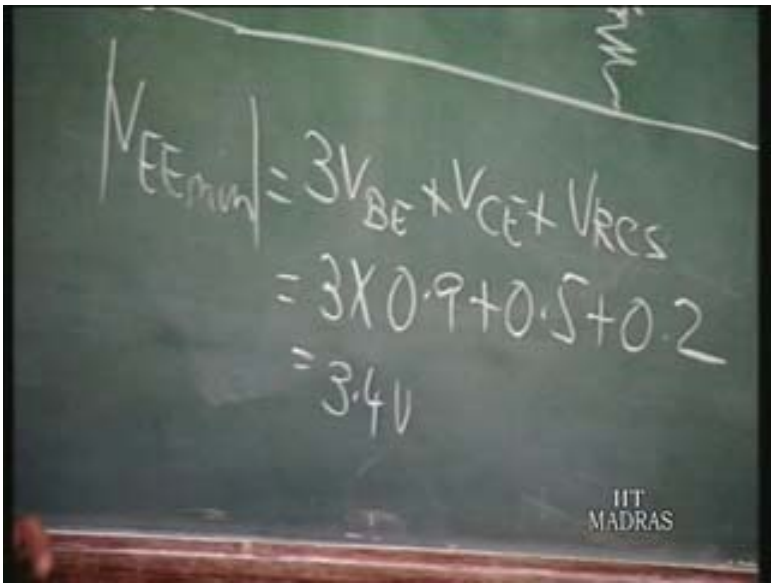
Now let us see what is the power supply requirement, what is the maximum or we should say what is the minimum value of v_{EE}, one requires for the circuit to operate?
(Refer Slide Time: 00:26:38)



Here you have a current source, let us see the drop across these resistances is one drop so let us call this v_R across the resistance for the current source then you have the v_{CE} of this transistor, this is v_{CE}. Then you have the v_{BE} of this transistor. From here this is v_{RCS} then you have v_{CE}, from here to here you have v_{BE}, another v_{BE}. I think another v_{BE} will be there, I just remove this now (Refer Slide Time: 26:25). So this is v_{BE} and then from this point to this input point here you have another v_{BE}. So this is another v_{BE} and so this value, this must be at least minus v_{BE} here, so there is another v_{BE} again

here at the base. Here it is minus v_{BE} to minus v_{BE} minus 500 so there should be at least another v_{BE} here.

(Refer Slide Time: 00:29:19)



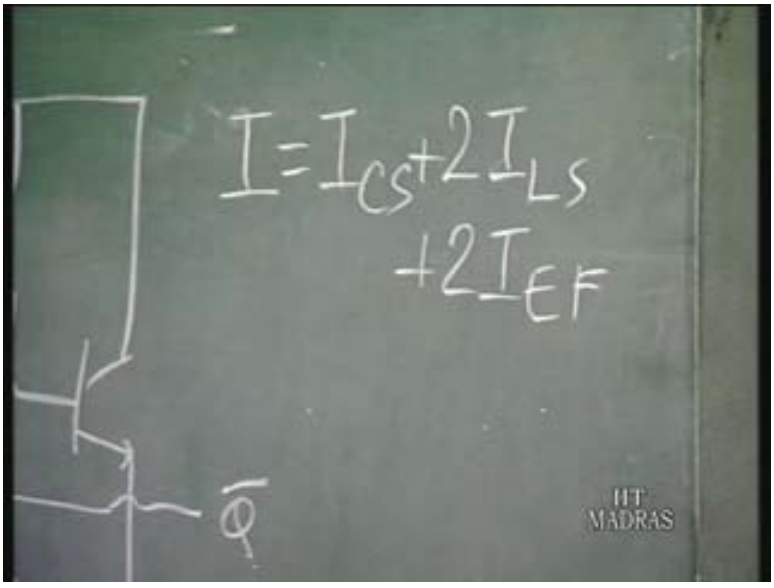
So totally you have 3 v_{BE} plus v_{CE} plus v_{RCS}, so v_{EE} minimum is equal to 3 v_{BE} plus v_{CE} v_{RCS}. Now for this circuits v_{BE} is actually given by, v_{BE} we can write is v_{BE} intrinsic that is the intrinsic drop across the pn junction plus I_B R_B + I_E R_E.

(Refer Slide Time: 00:28:35)

These are the drops across the parasitic resistances. Now for a small size device the resistances are usually large because the resistance depends on the cross sectional area. If we have a smaller size device, you have a larger resistance. So if you talk of very high speed devices, the extrinsic resistances are quiet large and so this value v_{BE} may be as large as 0.9 volts. It is not that the 0.9 volts is dropped across the pn junction but large part is dropped across the parasitic base an emitter resistances. So say v_{BE} is 0.9 volts, v_{CE} so this transistor suppose we assume its 0.5 volts, the collector emitter drop and v_{RCS} is 0.2 volts say then we have 3 into 0.9 plus 0.5 plus 0.2. So which means 3.4 volts so this is actually the modulus of that.

So v_{EE} we can have is minus 3.4 volts for this structure and the current of course or I write it here, I is equal to I_{cs} the current source value going through the current source, there is one current source here plus there are two level shifting parts the current will flow through these two, one current source two level shifting and two emitter followers.

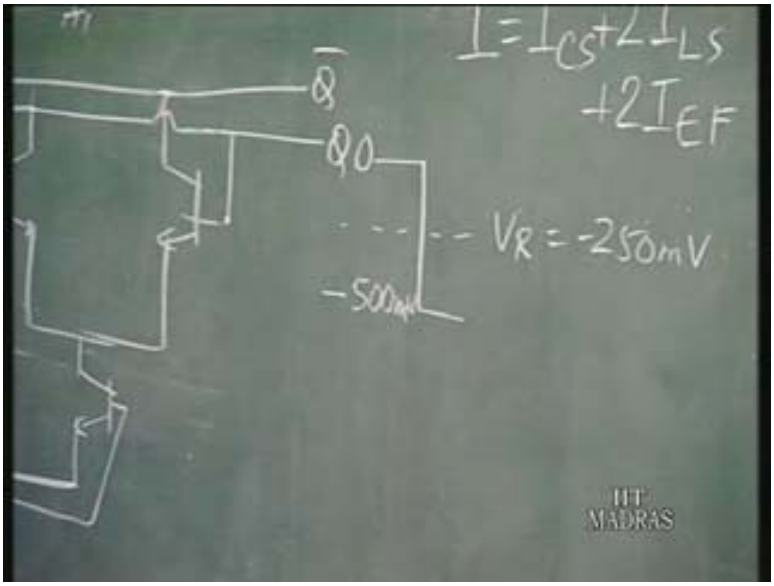
(Refer Slide Time: 00:30:11)



So you have I_{cs} plus 2, I should say level shifting circuits plus 2 I emitter followers. This is the amount of current which flows and you have the voltage and so the voltage into current is the power dissipation. So now if you have to reduce the power dissipation what you have to do is we have to tackle it both ways that is you can reduce the voltage power supply voltage as well as the current.

So a circuit which has lower power dissipation can be constructed by making a small modification in this circuit. Firstly what you can do is you can remove this emitter follower stages. (Refer Slide Time: 00:31:05) So basically what you have now is this goes in directly here as the thing and here goes in directly. So you have removed the emitter follower. The emitter follower has been removed which means basically the output voltage is no longer varying from minus V_{BE} to minus V_{BE} minus 500 volts but the output voltage so here this is Q bar and this is Q here, the output voltage variation now is from 0 to minus 500 millivolts and V_R would be centered somewhere is equal to minus 250 millivolt.

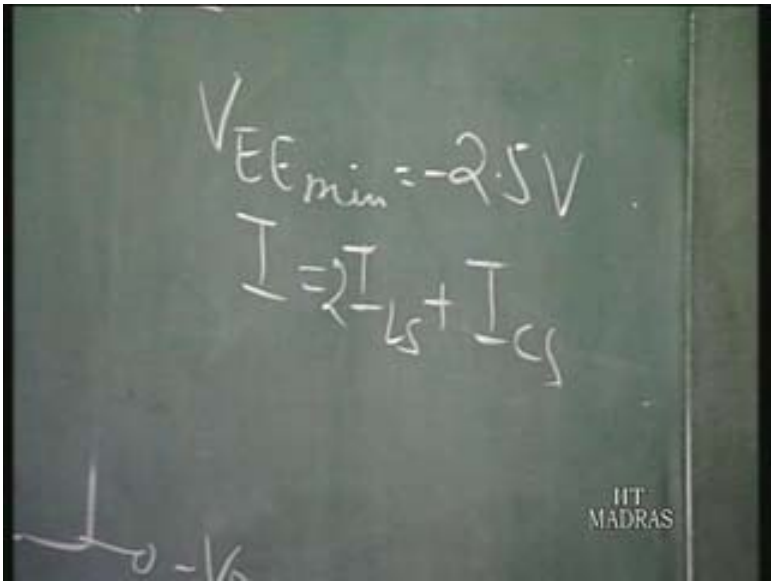
(Refer Slide Time: 00:32:08)



So the input voltage here that is at the clock input here is no longer this minus v_{BE} minus 500 volts but it is now from 0 to minus 500 millivolts. What has happened now? What is the change in the v_{EE} minimum? So basically what we have done is we have increase the input voltage by v_{BE}, it was initially the previous circuit minus v_{BE} to minus v_{BE} minus 500 so we have the raised the input voltage by v_{BE}, shifted it up. The v_R also have been shifted up by v_{BE} so it has no problem as such.

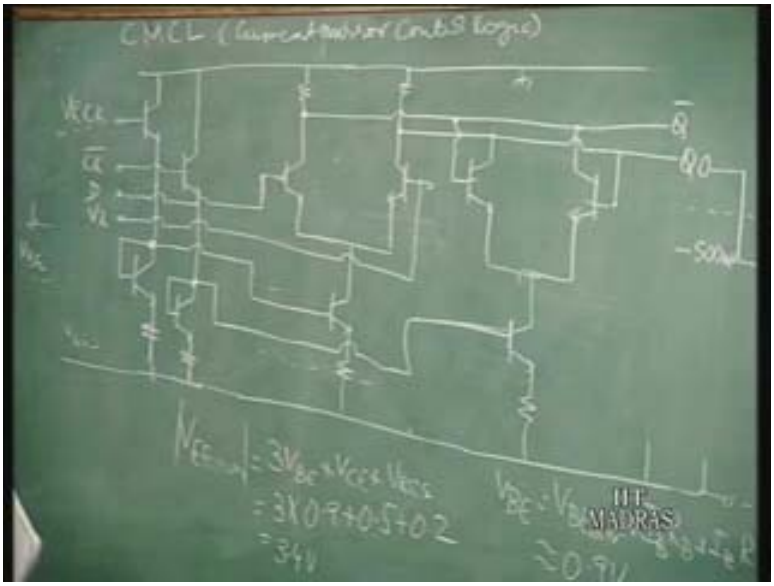
Of course you may have to be careful about the fan out as we had discussed in the first class but there is always a tradeoff. So here we are looking at low power dissipation. So what happens to v_{EE} min? Since the input voltage now has been shifted by v_{BE}, so the input voltage can be straight away 0 volts. So there is no extra drop of v_{BE} here. So the v_{EE} minimum is going to be instead of the previous case we have 3 v_{BE} plus v_{CE} plus v_{RCS}, so in this case it is going to be 2 v_{BE}, 1 v_{BE} is less.

(Refer Slide Time: 00:34:29)



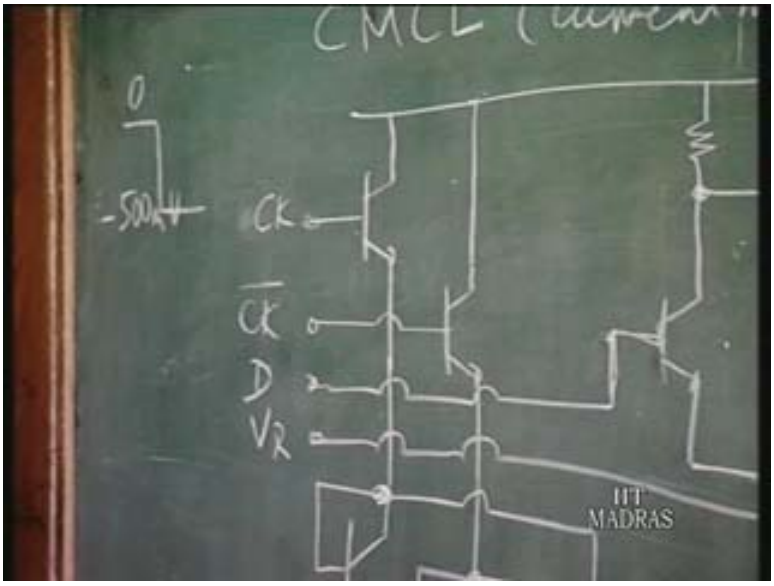
So the V_{EEMIN} for this circuit is equal to minus 2.5 volts and I again have also being reduced (Refer Slide Time: 00:34:29). What happens? The emitter followers have been removed, so you have 2 I_{LS}, 2 level shifting plus I_{CS}. So this is a lower power circuit. Now what we shall do is so this is about the lower power stacked ECL circuit to achieve a D flip flop. Now I will come to the newer concept of the circuitry which is called the new circuit which has been proposed. So the circuit is called by the name CMCL or current mode control logic. Now we shall see what is the modification here. In this circuit it is slightly different it looks different. This is current mirror control logic (Refer Slide Time: 35: 58).

(Refer Slide Time: 00: 37:13)



So what you have here is a current mirror arrangement. Here you have a current, suppose you are aware of what is a current mirror. That is basically you have circuit here which controls the current flowing in some other circuit. Now here this goes in here and this goes in here as the input. So all this remains the same as in the previous circuit. This is D, this is V_R and again what you have here is the input voltage variation is from 0 to minus 500 millivolts (refer slide time: 00:37:32). So this is 0, this is minus 500 millivolts.

(Refer Slide Time: 00:37:32)



Now what you have here is this is the current mirror arrangement, this transistor and this transistor and this is another current mirror arrangement. So basically what you have is a diode configuration here. The collector and base is shorted and whatever is

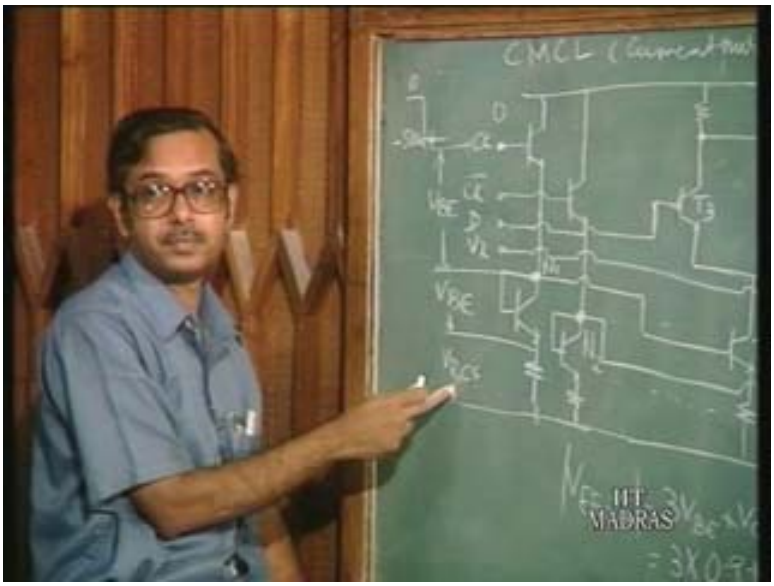
the current flowing here so if this transistor is on, so this voltage here is going to be high and which would mean that this transistor $v_{B.}$ will be high and this is going to be on. Whereas if this voltage at this node, if we call it a node $n_{1.}$, this node $n_{2.}$.

If the voltage at node $n_{2.}$ is high then the base voltage of this transistor to which it is connected is going to be high and this is going to be turned on. So basically what we want to say is previously in the previous circuit you had an emitter coupled system here to which you are feeding the clock and clock bar and depending on whether the clock is high or clock bar is high, in the upper stack either the left part was being on or the right hand side stack emitter coupled structure was on.

Here instead of having an emitter coupled structure here at the lower part of the stack, you have an arrangement like this. So basically what is going to happen is say if clock is high that means here the voltage is 0 volts say that would mean clock bar is low that is minus 500 millivolts and then which would mean that voltage at node $n_{1.}$ is going to be high because basically a level shifting here.

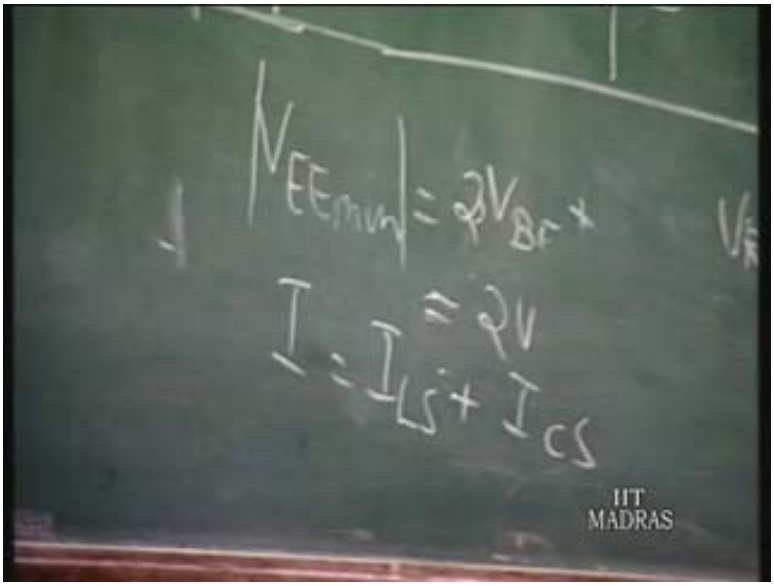
Voltage at node $n_{1.}$ is going to be high and the voltage at the node $n_{2.}$ is going to be low. So which means that between these two transistors say transistors $t_{1.}$ and $t_{2.}$, $t_{1.}$ would be having a much larger current compared to $t_{2.}$. $T_{1.}$ and $t_{2.}$, $t_{1.}$ is drawing much larger current compared to $t_{2.}$ because the base voltage of $t_{1.}$ which is the same as the node voltage $n_{1.}$ is much higher than the base voltage of $t_{2.}$ and that is how basically transistors $t_{3.}$ or $t_{4.}$ can be on, whereas $t_{5.}$ and $t_{6.}$ will be off because $t_{2.}$ is carrying very little current. So $t_{5.}$ and $t_{6.}$ will remain off, $t_{3.}$ and $t_{4.}$ will be on. Now in this case what is the maximum value of the power supply voltage?

(Refer Slide Time: 00:41:11)



What you have here is this again v_{RCS} let us say this is the voltage. From here to here you have v_{BE} at the base at node n_1 and from here you have another v_{BE}. What is the maximum value of the input voltage, what is the maximum value of the power supply voltage? This twice v_{BE} plus v_{RCS} which means it is just 2 volts, twice v_{BE} is 1.8 volts and v_{RCS} is 0.2 volts, so the power supply voltage can be as low as 2 volts. So here this is going to be, v_{EEmin} is going to be twice v_{BE} plus v_{RCS} which means it is as low as 2 volts.

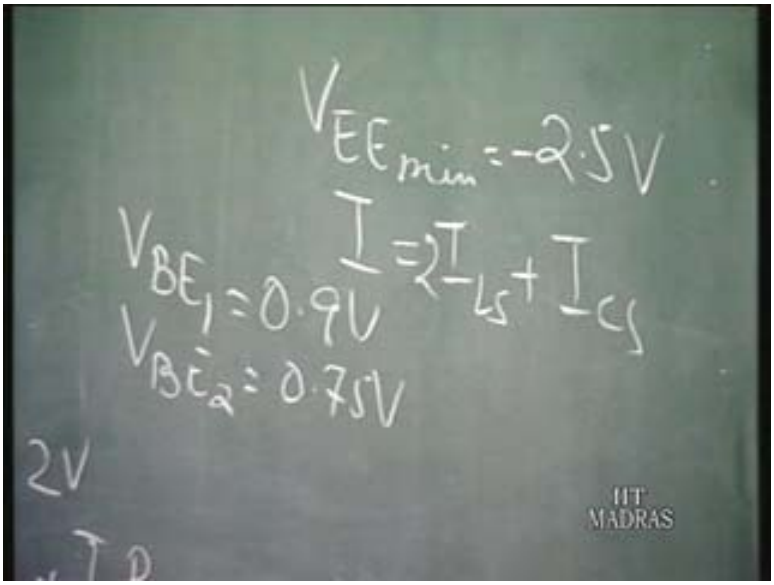
(Refer Slide Time: 00:42:23)



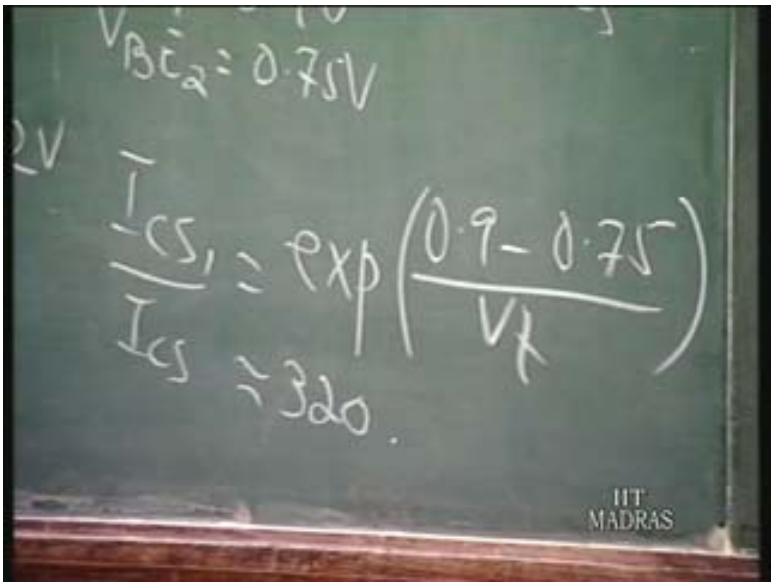
Also the current of course it is the sum of... What we want to say is that one of these is going to be on at a time as well as one of this is going to be on at a time. So we can say I is equal to I_{LS} + I_{CS}. Basically let us see if it is 2 volts let us say then minus v_{EE} is minus 2 volts here (Refer Slide Time: 00:42:38) and the input voltages clock and clock bar 0 and minus 500 millivolts. So if it is zero the node one n_1, if we assume v_{BE} is 0.9 volts, n_1 is going to be 1.1 volts whereas n_2 is going to be minus 1.4 volts. Minus 0.5

at the clock bar input, see basically what you have is 1.5 volts is going to be dropped between v_{BE} of this level shifting transistor plus this diode arrangement here. So the maximum voltage which can be dropped if both of them are carrying the same current per junction is 0.75 volts.

(Refer Slide Time: 00:44:02)



(Refer Slide Time: 00:44:30)



So this transistor is going to be off which is less than the requirement of v_{BE} which we have said is 0.9 volts. So if this is say 0.75 volts, so if you say that at the base of t_2 you have 0.75 volts and at the the base of t_1 you have 0.9 volts, so v_{BE1}.. So if you say that v_{BE1} is equal to 0.9 volts and v_{BE2} is 0.75 volts then you can say that the 2 currents, so

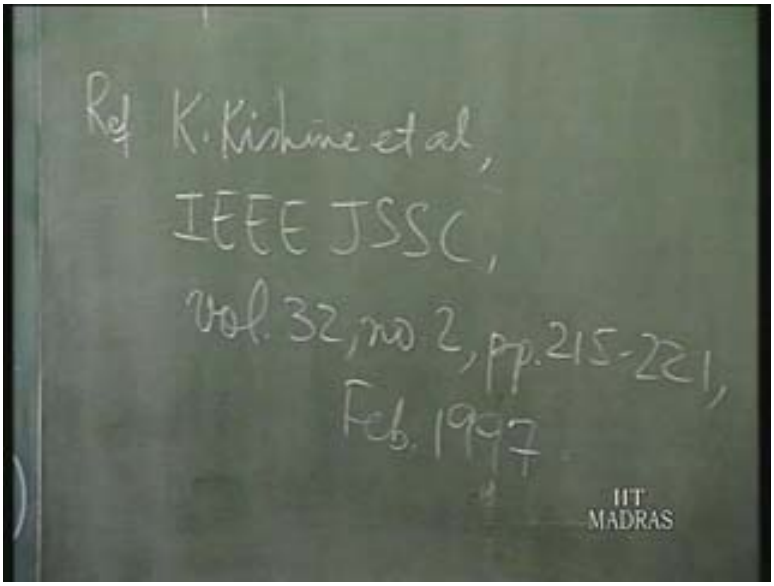
I_{cs1} by I_{cs2} will be equal to that is the 2 current source values is equal to exponential because it is dependent on exponential v_{BE}. So it is going to be exponential 0.9 minus 0.75 by v_t, so this is around 320.

The current flowing through one branch here is going to be about 300 times that of the other branch. So we can safely say that only the current is actually flowing in one of them and the other current is almost zero. That is basically depending on which node n_1 or n_2 is high, one of the branches are going to control the current. So here with a current mirror instead of an emitter coupled structure, we choose which branch is going to be conducting and in the process what happens is the power dissipation is reduced because of the fact, we require a lower power supply voltage at the same time the current requirement is also less.

In fact in that paper they have given some results, they have fabricated D flip flops operating at I think D flip flops just give you some results at 3.1 gigahertz clock frequencies and drawing power at 1.8 milliwatts per flip flop. So that is the level of power, only 1.8 milliwatt power flip flop and also they have done fabricated T flip flops operating at 4.3 gigahertz and they claim that this is the lowest power dissipation for any gigahertz family and I will also give you the references so if you are interested you can go through it, K. Kishine and others, IEEE journal of solid state circuits, volume 32, number 2, pages 215-221, February 1997.

So this is a new logic family I mean sort of variation of the ECL where you achieve a lot of reduction in power dissipation which is the stumbling block in ECL and with this advancement, one hopes one can realize LSI level circuits using ECL that is what they claim in that paper.

(Refer Slide Time: 00:47:03)

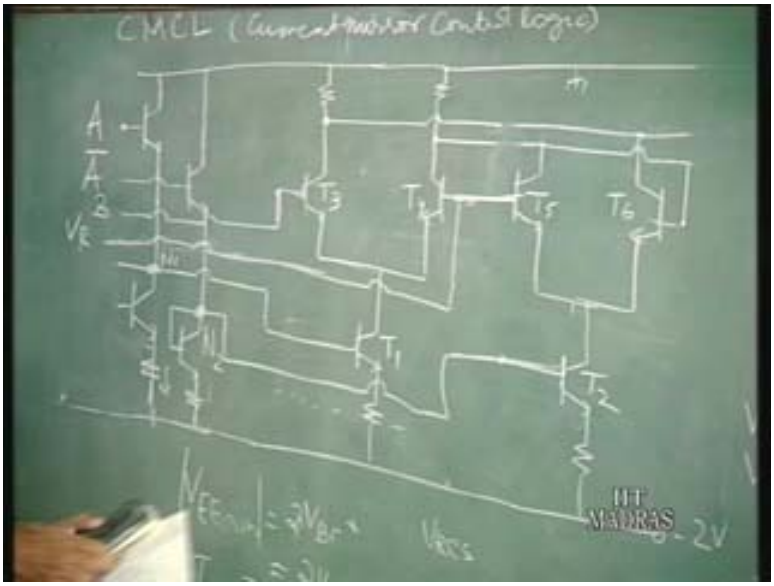


So in fact this is the d flip flop using the same concept here, one can actually realize other logic circuits also just like a stack, just like a two level stack you can realize other logic circuits where the lower level is actually controlled not by an emitter couple structure but by a current mirror arrangement as given here.

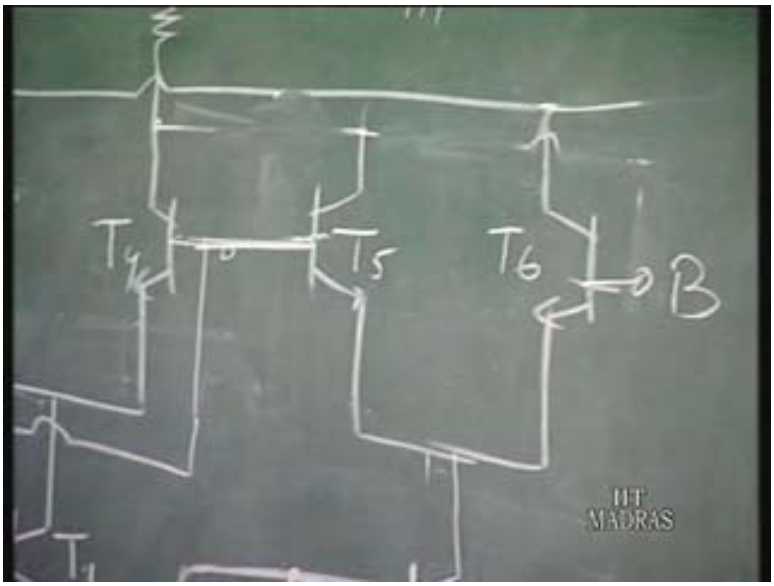
So I just give an example, maybe I just modify this, it is easy for me to do on the blackboard. If I want an exclusive OR circuit, just like a d flip flop we have discussed, what does a d flip flop do? Just the difference between d flip flop and exclusive OR. D flip flop it is, the Boolean function is Q_n is equal to clock D plus clock bar into Q_{n-1}. Here in an exclusive or it is A bar B plus AB bar.

So it is quiet similar that is what you have to do is here in one of the inputs, you put A and here you put A bar. So if A is high one of these nodes will go high and A bar the other nodes is going to go high. So if A is high then this circuit is on, if A is low then the other circuit is on.

(Refer Slide Time: 00:49:42)

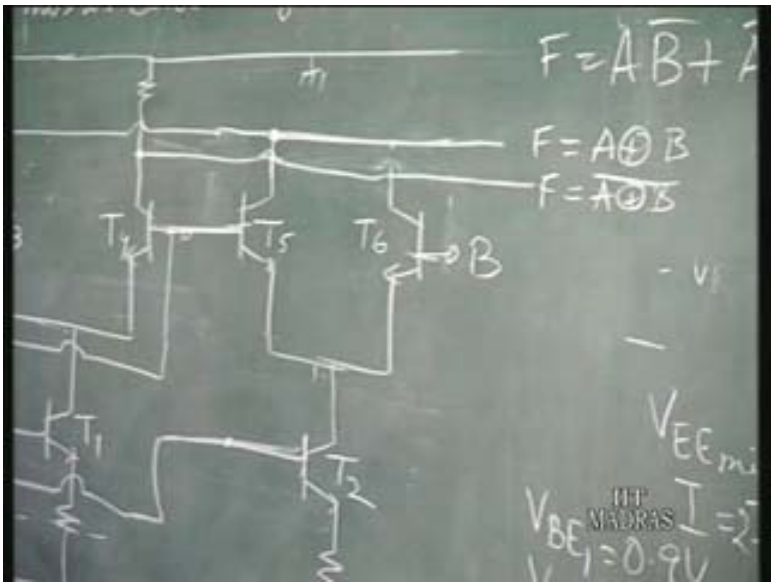


(Refer Slide Time: 00:49:51)



So what you have to do is we put a reference voltage here. So here this is the reference voltage and the other input here you put B and here also you put B here also you put B. So what we have to do is if A is high that is here in this circuit, this output is equal to B bar the, you have B here so this is reference voltage. Just like an ECL gate this corresponds to B bar, nor output B bar this corresponds to B.

(Refer Slide Time: 00:51:04)



So exclusive OR just F is equal to A B bar plus A bar B. So when A is high F is B bar when A is low F is B. So when A is high that is this part is on, this is B bar and when A is low then this circuit is on the output should be B. So if this is B you get here B. You should short this to outputs here and this is going to be F = A exclusive or B. The other two outputs give the complement actually. So if A is high, this part of the circuit is on so this is going to be A exclusive or B. If A is high, F is going to be B bar. If A is low then this gives B, so the output is going to be B, so these two are shorted. So that gives A exclusive or B. the other two outputs is these two are the collectors can be shorted to give exclusive nor combination.

So today we have discussed the new circuit concept that is the current mirror control logic and this is again a variation of ECL gate and it helps in reducing the actual power dissipation in ECL gates, ECL family of logic gates. So there has been lot of work in this area and this gives you some idea of the ongoing work which is going on, lot of people are still working at it, how to reduce the power dissipation. Next few clauses we shall look at the attempts to increase the speed of ECL gate still further. The ECL is the fastest logic family but there is a continuous need to achieve higher and higher speeds. So what is the way people have done it from technology point of view as well as maybe from the circuit point of view.