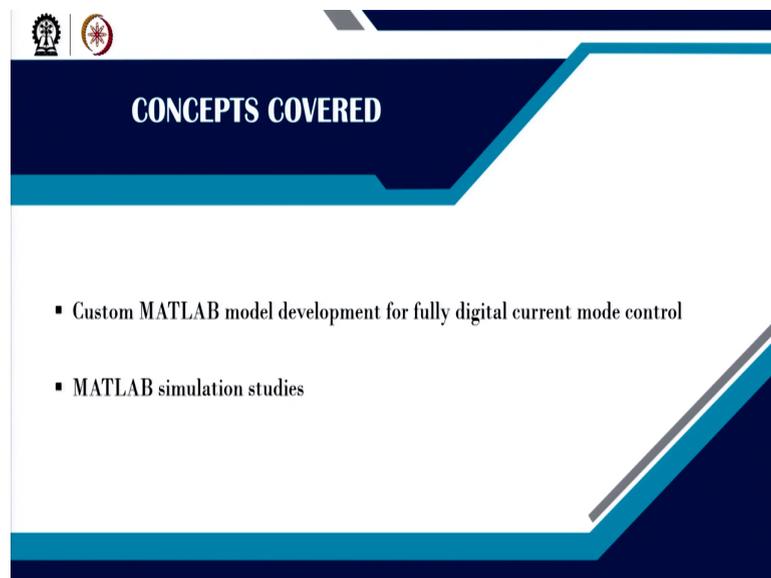


Digital Control in Switched Mode Power Converters and FPGA-based Prototyping
Prof. Santanu Kapat
Department of Electrical Engineering
Indian Institute of Technology, Kharagpur

Module - 03
MATLAB Custom Model Development under Digital Control
Lecture - 27
MATLAB Model Development for Fully Digital Current Mode Control

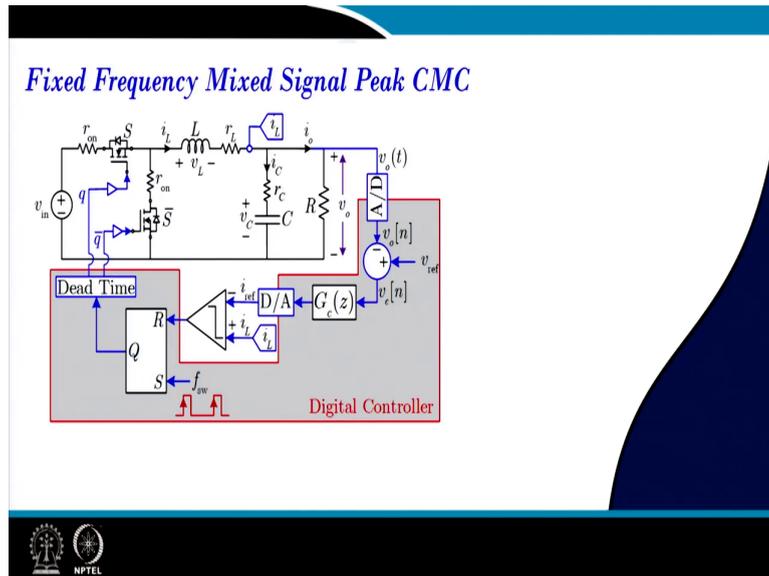
Welcome back. So, in this lecture, we are going to talk about fully digital current mode control architecture.

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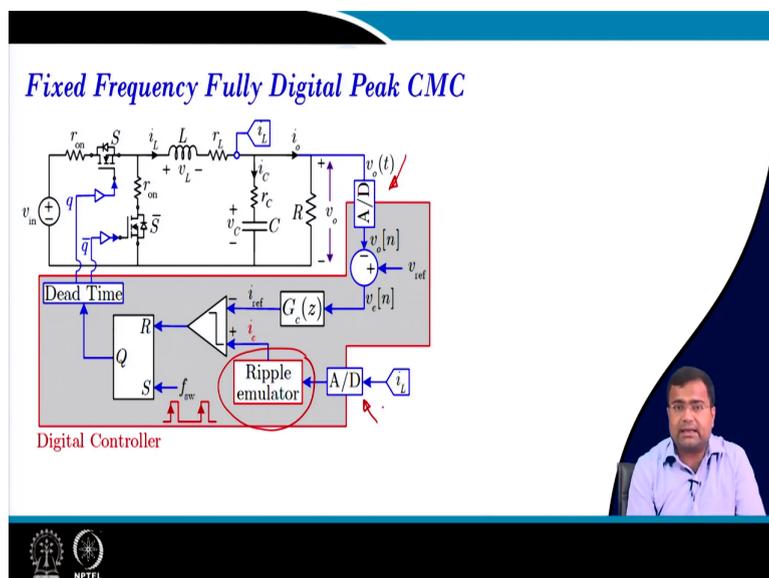
So, first I will show you a custom MATLAB model development for fully digital current mode control and then I want to consider a few simulation case studies.

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So, first, we will start from fixed frequency mixed signal peak current mode control, because we have discussed in the last class, where we have considered the analog current loop and digital voltage loop.

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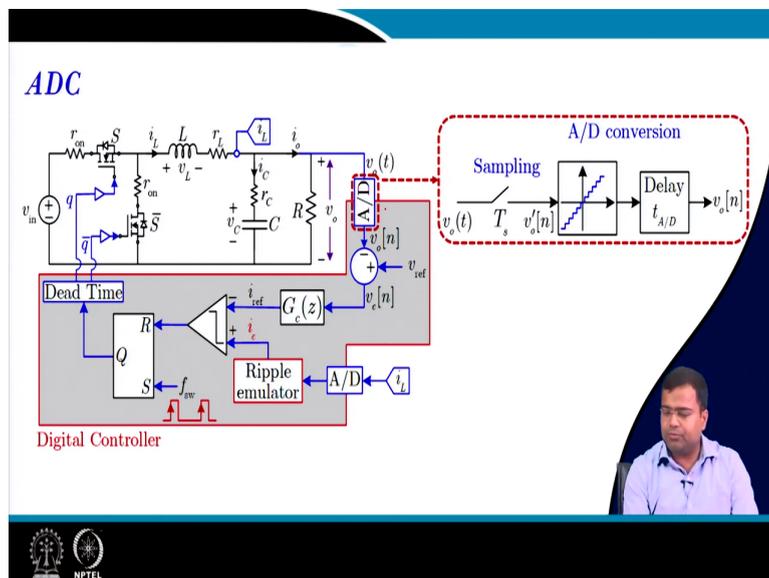


Now, if you go to fully digital current mode control then we also need to sample the inductor current; that means, we have already sampled the output voltage here. But we also need to sample the inductor current and we have discussed there are two possibilities, if we sample the inductor current because we need to retain the ripple information of the inductor current.

So, one way you can use a very high sampling rate for the current loop, but that may not be preferable because that will incur more losses and you need a very high sampling or high-speed A to D converter. But, rather is more you know kind of effective way.

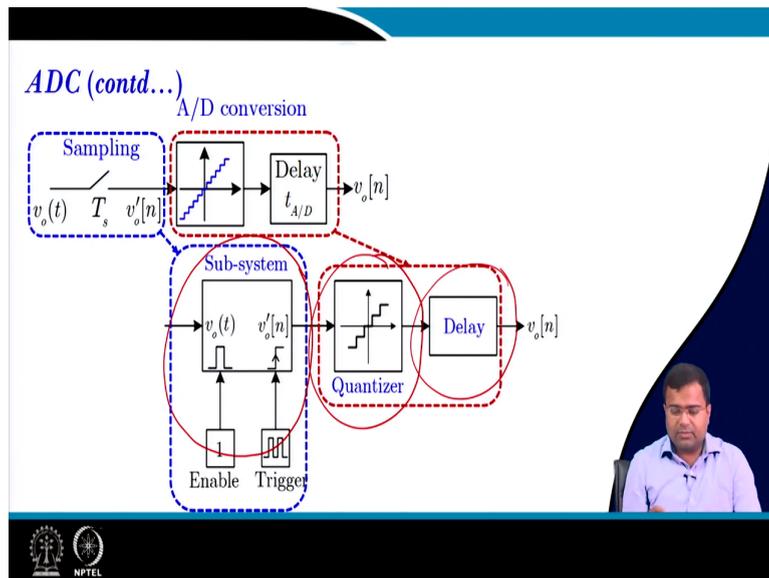
If you can sample once per switching cycle and emulate the ripple of the inductor current internally using the digital control platform that means, but it is not necessary that we need to generate the same rising slope of the inductor current. It may be different ok, but we are trying to emulate this current ripple inside the digital platform and we are taking samples of the inductor current once per switching cycle.

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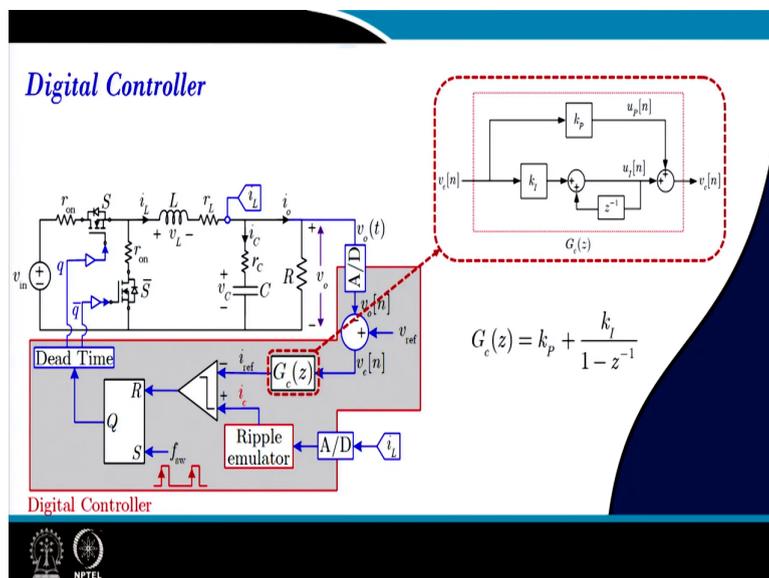
So, how to start with? So, we want to repeat the same process as the A to D converter that we have discussed for the voltage loop it has sampler quantization and the delay.

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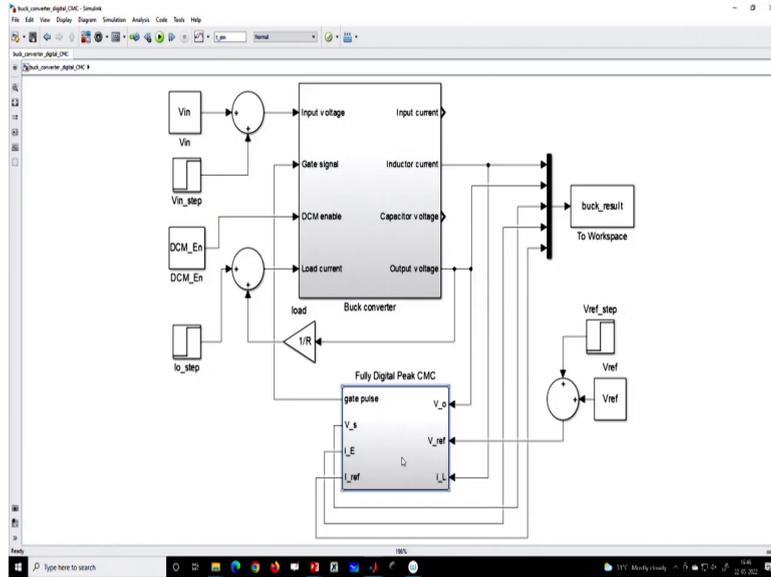
And we have already discussed that the whole A to D process can be divided into this event trigger sampling followed by quantization and you can add one additional delay also.

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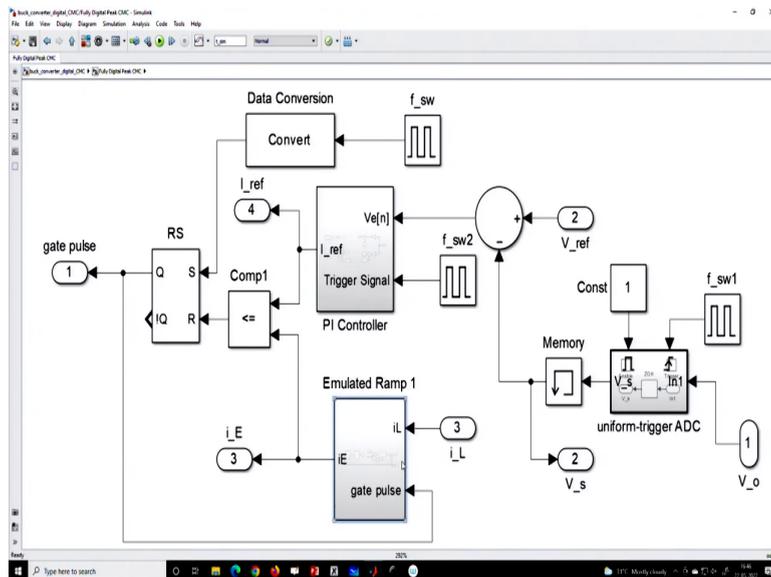


Next, this part we have discussed and we have discussed it for multiple lectures. We have also discussed how to implement a PI controller. In fact, in the previous lecture, we discussed that if you want to implement a PI controller using a difference equation, not by transfer function then it has to be clock synchronized.

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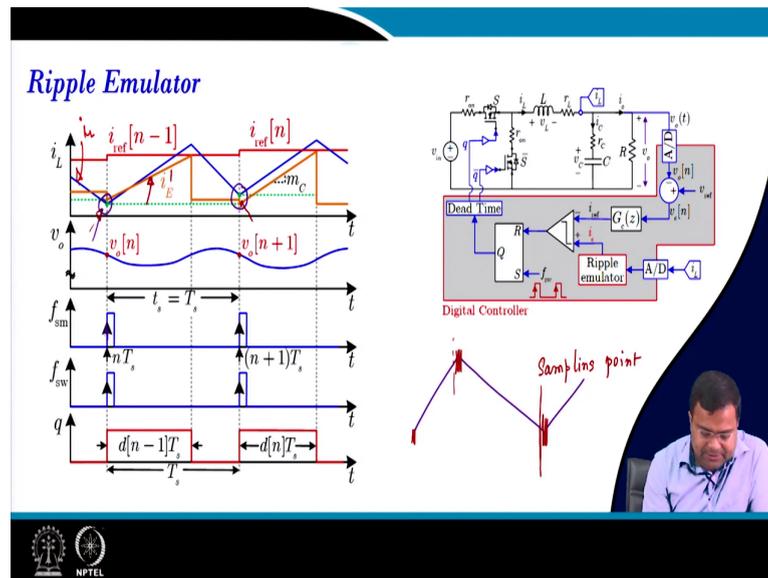


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And if you go back to the MATLAB file; that means, this is a full digital peak current mode control.

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Next, this part is very important because here we are not using an analog current loop. We are using emulated current; that means, let us first start with the basic concept. If you sample the inductor current, let us say this is our blue one is the actual inductor current ok.

Now, this is the sample of the actual inductor current; that means, we are sending the sampling command that is the point we want to sample, and generally, this sampling point is slightly earlier than the actual switching takes place. Because if you go to any current sensor right? So, you will find the spike in the current sensor the switching spike. One the switch turns on or the switch turns off.

So, every time; that means, I am talking about this as the actual inductor current, but let us say if you go for any sense inductor current then you will have switching spikes here after the switch turns on and off. So, to avoid a such spike, so we want to sample just before the switch either turns on or turns off. So, in this case, we are talking about the trailing edge modulation. So, we are talking we are taking the sample here; that means, where this is the sampling point.

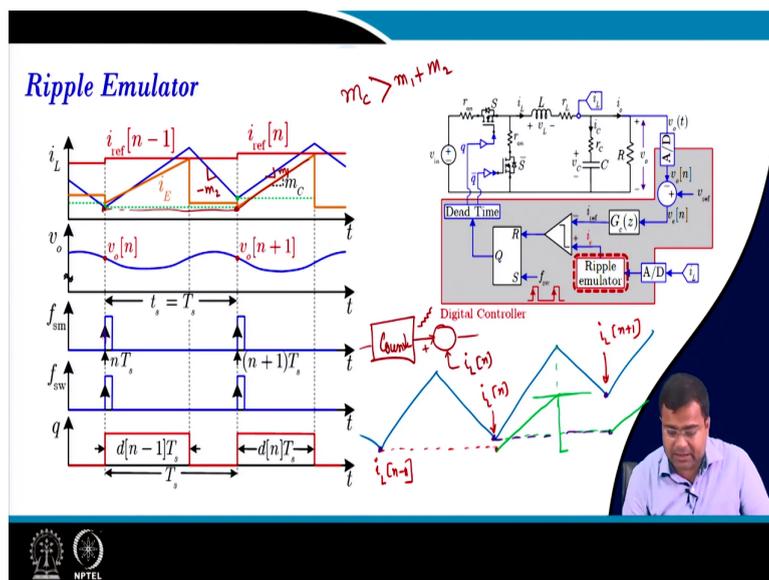
This is just below the switch that is about to turn on; that means, it is in the off state. That means you can say it is a valley current. Now that means, we are sending the sampling command here. But, as I said the A to D converter requires time for conversion; that means, we cannot get any immediate sample available for the controller, because we need to add this

Sawtooth waveform to the ramp I will discuss. But, we cannot use the current sample for the running cycle because we need to provide some time for A to D conversion.

So, that is why the sample command is sent here, but the actual current sample is used in the next cycle. So, there is an inherent 1-cycle delay. So, that means, this is the point of sampling here, but the availability of the sampling including we are forcefully delaying you know for the safe side because we need the information of the valley current. Because we cannot take any other point, because we need to take the valley point.

So, using that valley current information in the next cycle and you can see this one this particular waveform indicates the Sawtooth waveform that is used inside the digital controller; that means if I want to draw let us say this conceptual point.

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So, suppose I am just taking let us say I am just considering the inductor current like this ok. So, this is the inductor current waveform. Now we are sampling the current here; that means, we are just sampling just before the switch turns on.

But, we are using this sample in the next cycle; that means, this sample if we just interpolate this sample if we extend it here. Now we want to add a ramp; that means, we want to create a Sawtooth waveform here this is addition. That means if I take this is my $i_L n$ minus 1 and if this sample is $i_L n$ and if this sample is $i_L n$ plus 1 and so on. So, we want to add a ramp.

So, Sawtooth waveform means it is like a staircase implementation and if you take a very narrow staircase it will be like this.

That means if we want to that means, whenever we start switching at this point we are using a different color. Let us say we want to start this slope may be different, this slope may be different 1 minute. So, this slope should be different, and why we are going up to this is because here we have to turn off. And how it is turned off? As if there is a peak current reference that is coming here.

When this hit the peak current then turn it off and since we are using a counter we will simply reset this. Because we are using the counter and why we have reset it because we want to after this there is a latch operation, it is a trailing edge modulation the switch will cannot change state; that means, once the switch is turned off the switch cannot turn on throughout the rest of the interval.

So, it has to wait for the next clock edge. So, that means, it is not necessary to extend this waveform beyond that or we do not need to emulate the falling slope for peak current mode control because that information is simply redundant, we do not need that. So, we simply reset it.

Next time now this sample point is extended. So, this sample point is extended here; that means, we are using this sample point is extended here. But our Sawtooth waveforms our ramp signal; that means, this will start from here. Again it depends upon the peak current. So, that means, you can see this waveform that means if I rub up all these parts.

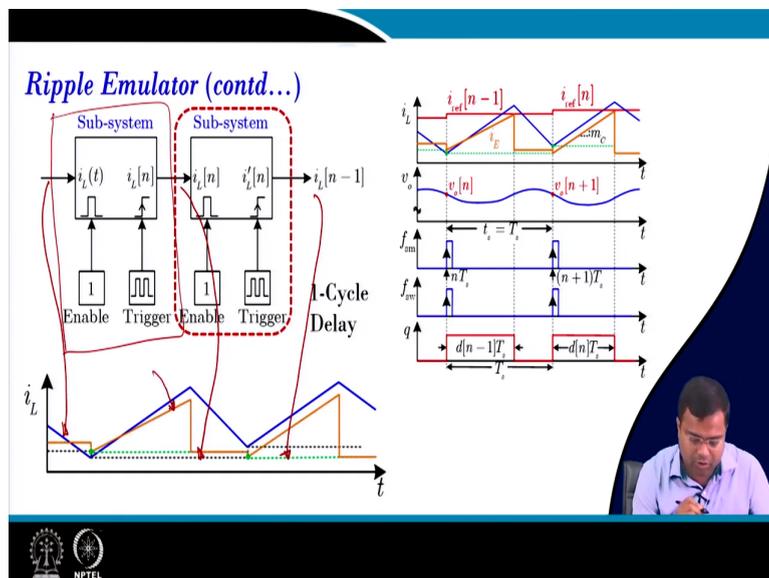
So, you can see the sample of the inductor current is used in the next cycle here and with an added ramp. Although it looks like the ramp is the same as the rising slope, it is not necessary, the ramp can be different. You know there is much research that this ramp should be different and we cannot keep this m_1 slope because it will be unstable even with this m_c requirement when I go to the analysis part.

It can be shown that the m_c has to be greater than m_1 plus m_2 ; that means, m_1 is the minus m_2 is the falling slope of the actual inductor current and m_1 is the rising slope of the inductor current. So, this m_c has to be greater, otherwise, it will be inner current loop will be unstable and that can be proved. But what I am showing here is that you need to add a ramp ok to emulate this current.

Now, so I think the basic operation is clear. We have to take the sample of the inductor current we have to delay by 1 cycle and then we have to add the compensation. So, compensating ramp or the emulated ramp is always added in every cycle, but the only thing it base point depends because the if you say a counter let us say if say counter which generates this Sawtooth of waveform like this the output of the counter should be added with our sample current, whether it is $i_L[n]$ or $i_L[n+1]$ it will be updated.

So; that means, the base value will be changed according to the value of the inductor current sample ok.

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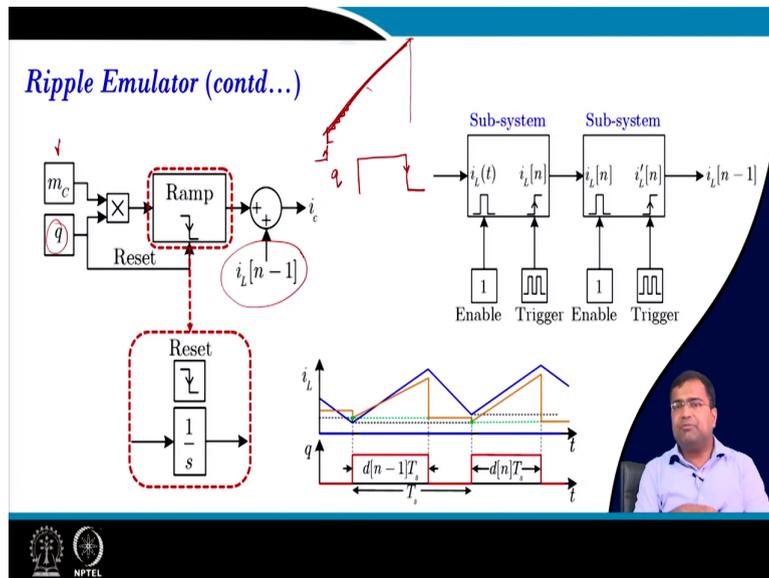


So, that means, now so how do you generate this sample inductor current? So, this is we know we can simply use an A to D converter block and that we know even trigger a DC, but we need to delay by one cycle, so you would another. So, if you simply use this current. This is the actual inductor current which is shown here and this current is shown here. This is a sample current.

You see it is taking the sample of the current just it is updating. But we need a realistic current sample for the controller, because this sample may not be available immediately. So, we need to use another such block which will delay by 1 cycle. And if you see 1 cycle delay, so this waveform is the green waveform here. So, that means, we are generating the first block will generate the sample and hold of the current valley point and the second block will delay by 1 cycle.

So, this is the overall implementation of the sample value, but it is not sufficient. Because we have to add this ramp because, after this sample point, we have to add this ramp; that means, we need an additional block of this.

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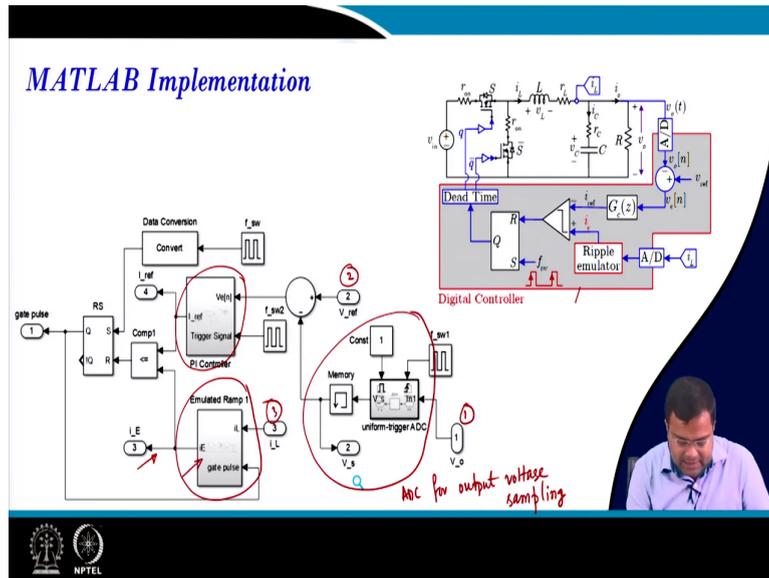


And how to generate a ripple emulator? So, that means, that means m_c and we are only activating this m_c because it is just for the MATLAB program, but if you use an FPGA or any digital controller you have to use this Sawtooth waveform right?

So, it can be a simple counter and it will start counting when the clock signal comes. That means that every rising edge of the switching clock; that means when the switch is turned on will keep on incrementing and whenever that means, this clock this ramp output plus the sample current is added when it hit the peak current then it is reset. So, that is why there is a reset signal. So, that means reset will happen when you take the q signal; that means, when the switch goes low that means, this is the gate signal.

When it goes low that is resetting the the resettingter. So, it will just stop and this is the overall current controller that is used to; that means, and now this ramp here we are using simply integrator. It will integrate you can reset, but in the actual implementation, you can use a counter ok.

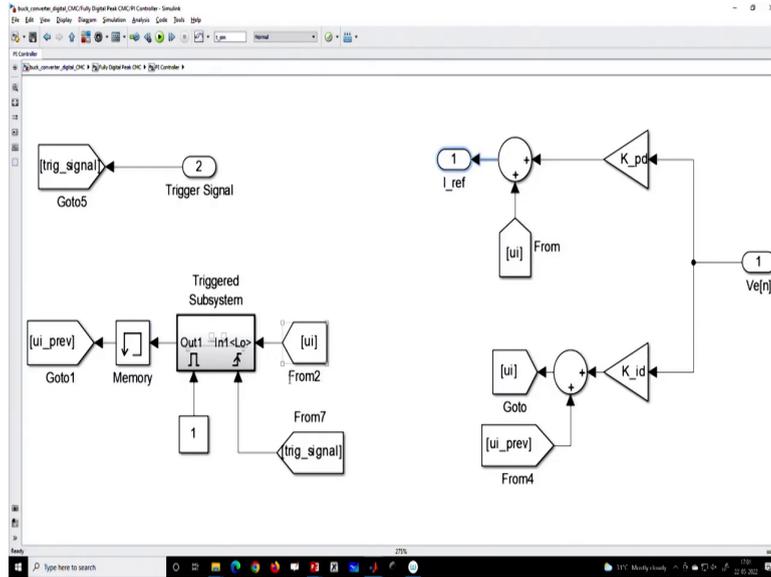
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What we are doing here? And for simulation, we have to verify we want to check what the emulator signal emulated ramp looks like. What does the reference current look like? And you can also see the sample voltage. So, all are captured in the workspace. Next, if we zoom the whole block of this controller.

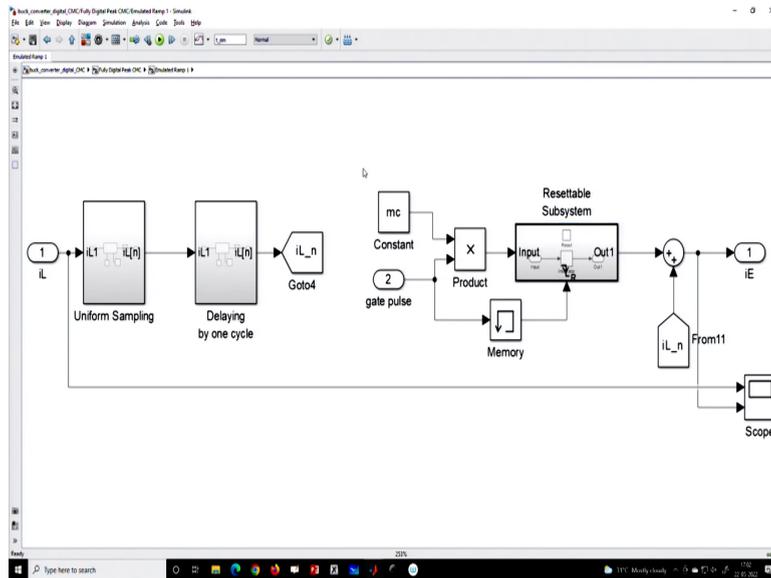
So, it starts with this you can see them; that means if you take this output voltage this is the number 1 number 2, and number 3 input port. So, the number 1 input port is this. Number 2 is the reference and number 3 is the inductor current. So, this block is our what is this block. This is your ADC for output voltage sampling ok. It is for output voltage sampling, ADC for output voltage sample. Next inductor current emulated ramp as well as the sampling block that should be inside and this is the PI controller ok.

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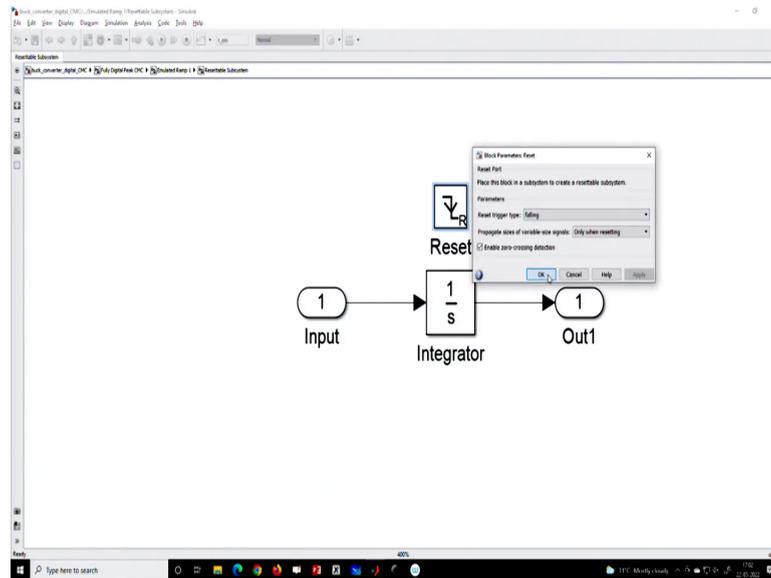


So, if you go to the MATLAB let us go to the MATLAB. Here you can see this is a controller block emulated ramp block that we are discussing.

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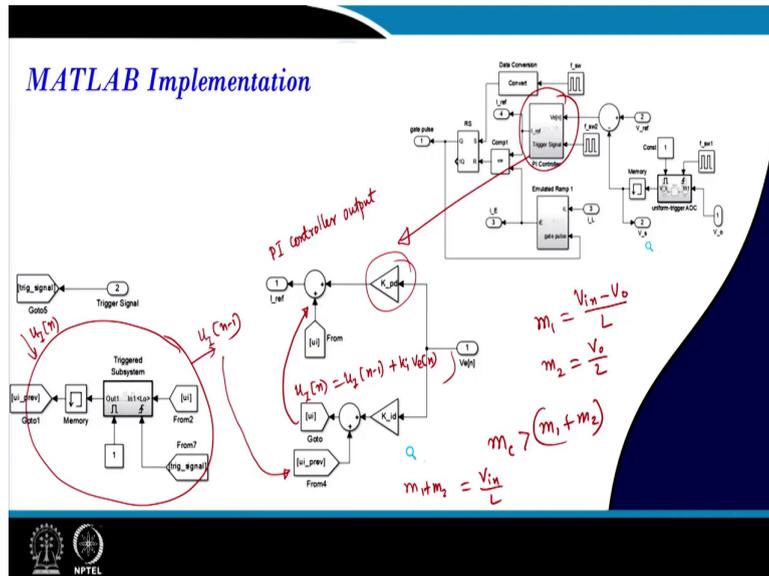
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So, if you go to the resettable block, there is a resettable integrator. That means, the integrator generally if it is reset otherwise the integrator will keep on increasing ok. And who will reset the integrator? The integrator reset happens; that means, you know based on the gate pulse. That means, the gate pulse has to there will be an edge you know is the edge detection circuit, and when you detect this edge.

So, this is an edge resettable edge. So, it will detect the falling edge and that falling edge is used to reset the integrator that is it. Next, the constant is the slope of the current that you want and output and this is the A to D converter for sampling ADC. This is for 1 cycle delay and this is added here. So, you can see this block and this block are the same go-to block and the form block and this will generate our actual emulated ramp. And I want to show you all the waveform, but before that, I want to explain the remaining part.

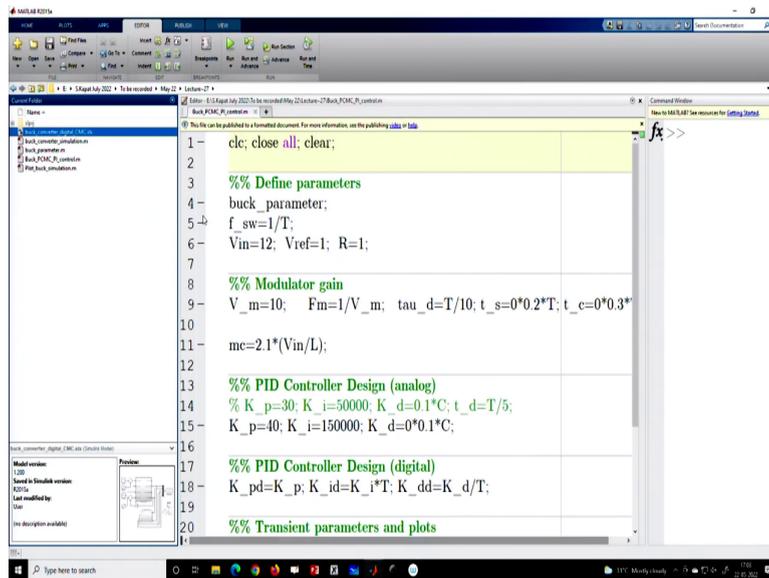
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Next, this is a PI controller. So, I am talking about this block. This block is shown here and we have discussed is the same as mixed-signal current mode control, where it is a PI controller and it is a clock-driven PI controller which is implemented using a difference equation.

And again this is used to generate what? If the input is $u_i(n)$ then the output will be $u_i(n) - 1$ and that is actually added here and then this $u_i(n)$ is generated which is $u_i(n) - 1$ plus k_i into $v_e(n)$ and this is $v_e(n)$ and this is your proportional controller and this output goes here by this block and this is overall. So, this is a PI controller output ok.

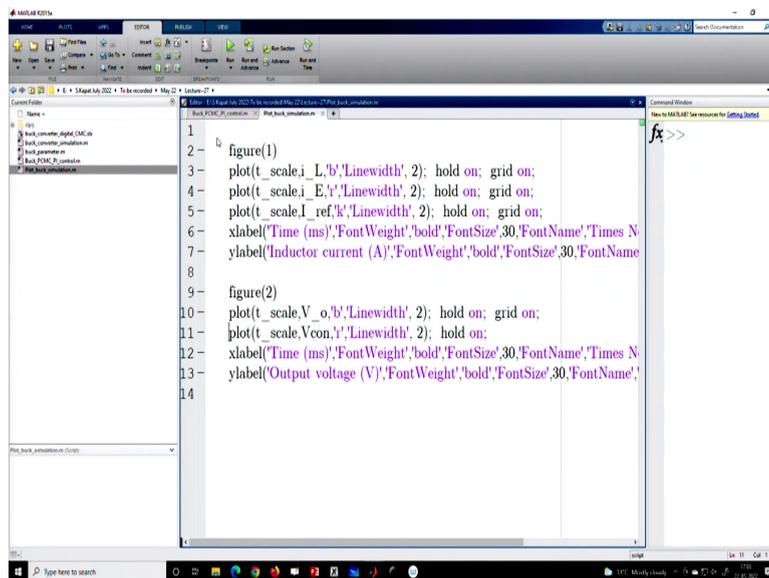
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```
1- clc; close all; clear;
2-
3- %% Define parameters
4- buck_parameter;
5- f_sw=1/T;
6- Vin=12; Vref=1; R=1;
7-
8- %% Modulator gain
9- V_m=10; Fm=1/V_m; tau_d=T/10; t_s=0*0.2*T; t_c=0*0.3*
10-
11- mc=2.1*(Vin/L);
12-
13- %% PID Controller Design (analog)
14- % K_p=30; K_i=50000; K_d=0.1*C; t_d=T/5;
15- K_p=40; K_i=150000; K_d=0*0.1*C;
16-
17- %% PID Controller Design (digital)
18- K_pd=K_p; K_id=K_i*T; K_dd=K_d/T;
19-
20- %% Transient parameters and plots
```

So, now let us go to the MATLAB and try to understand. So, we will simulate a few case studies.

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```
1-
2- figure(1)
3- plot(t_scale,i_L,'b',Linewidth', 2); hold on; grid on;
4- plot(t_scale,i_E,'r',Linewidth', 2); hold on; grid on;
5- plot(t_scale,I_ref,'k',Linewidth', 2); hold on; grid on;
6- xlabel('Time (ms)',FontWeight',bold',FontSize',30,FontName',Times N
7- ylabel('Inductor current (A)',FontWeight',bold',FontSize',30,FontName
8-
9- figure(2)
10- plot(t_scale,V_o,'b',Linewidth', 2); hold on; grid on;
11- plot(t_scale,Vcon,'r',Linewidth', 2); hold on;
12- xlabel('Time (ms)',FontWeight',bold',FontSize',30,FontName',Times N
13- ylabel('Output voltage (V)',FontWeight',bold',FontSize',30,FontName',
14-
```

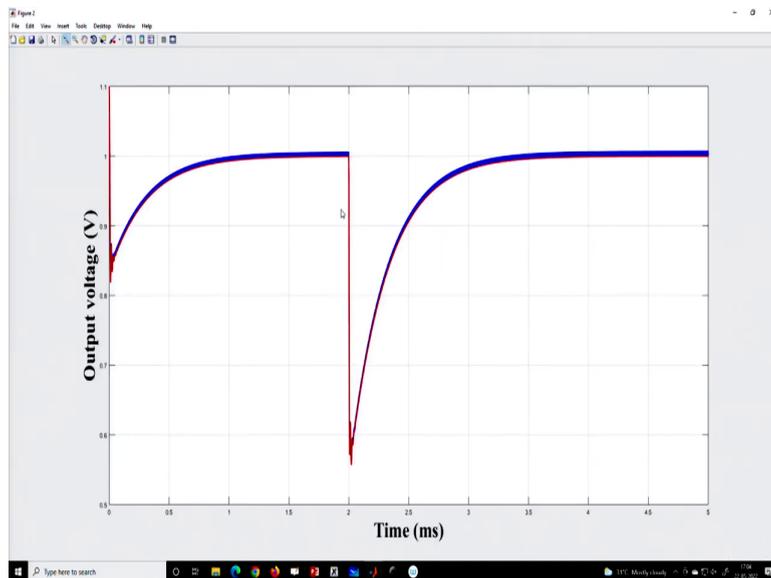
So, in this, I want to first you know if I go to the MATLAB I want to show a peak current mode control with a delay.

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```
8 %% Modulator gain
9 V_m=10; Fm=1/V_m; tau_d=T/10; t_s=0*0.2*T; t_c=0*0.3*
10
11 me=2.1*(Vin/L);
12
13 %% PID Controller Design (analog)
14 % K_p=30; K_i=50000; K_d=0.1*C; t_d=T/5;
15 K_p=40; K_i=150000; K_d=0*0.1*C;
16
17 %% PID Controller Design (digital)
18 K_pd=K_p; K_id=K_i*T; K_dd=K_d/T;
19
20 %% Transient parameters and plots
21
22 t_sim=5e-3; t_step=2e-3;
23 delta_Io=20; delta_Vin=0; delta_Vref=0;
24
25 buck_converter_simulation;
```

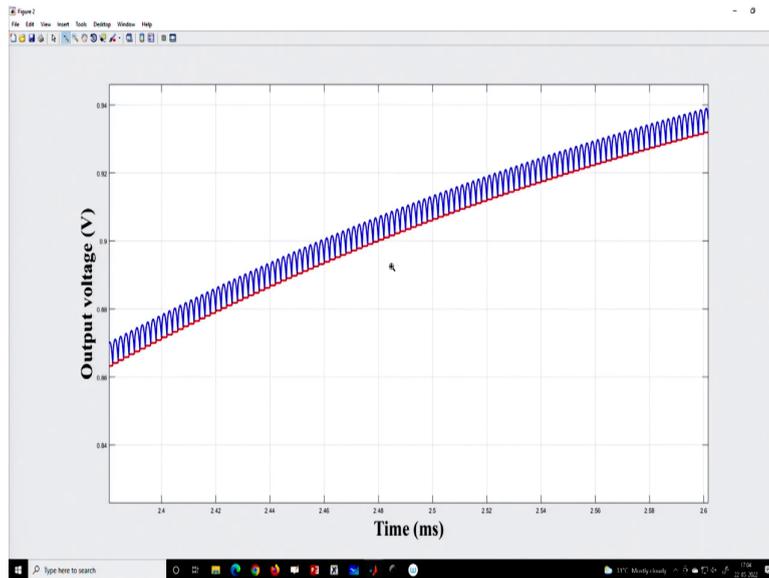
Where we are using again a low transient and we are not using a very large gain. So, let us first run the simulation and I want to show you all the signals ok.

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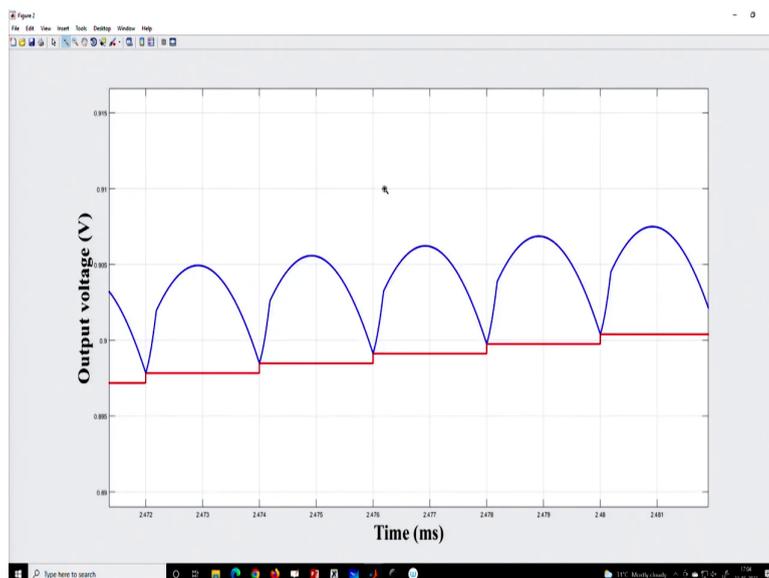


So, first I want to show the output voltage waveform.

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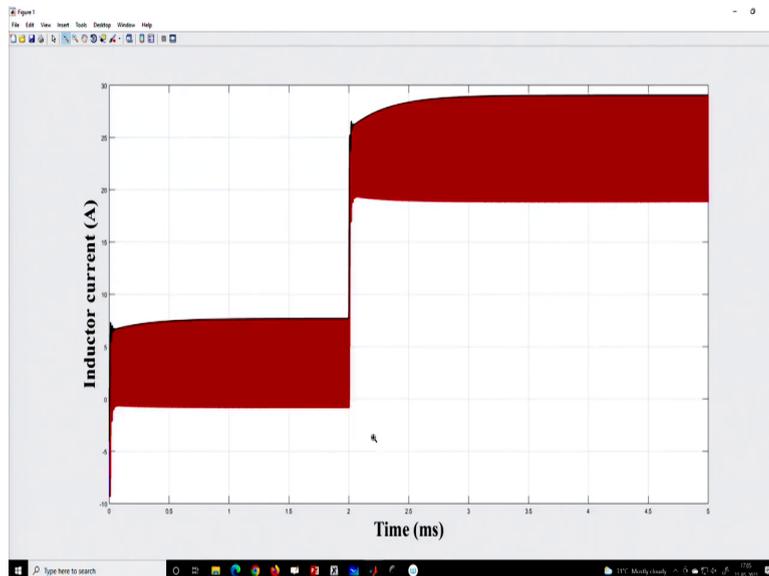
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And if you see the output voltage waveform you can see. So, here I am not showing any delayed version of the output voltage. Because if you add delay you can add it you can customize it based on the requirement, but I want to first try to show the basic implementation of fully digital current mode control. Where you there is no need to consider a delay. So, you can assume that the output voltage is sampled exactly at the switching point or just below before that.

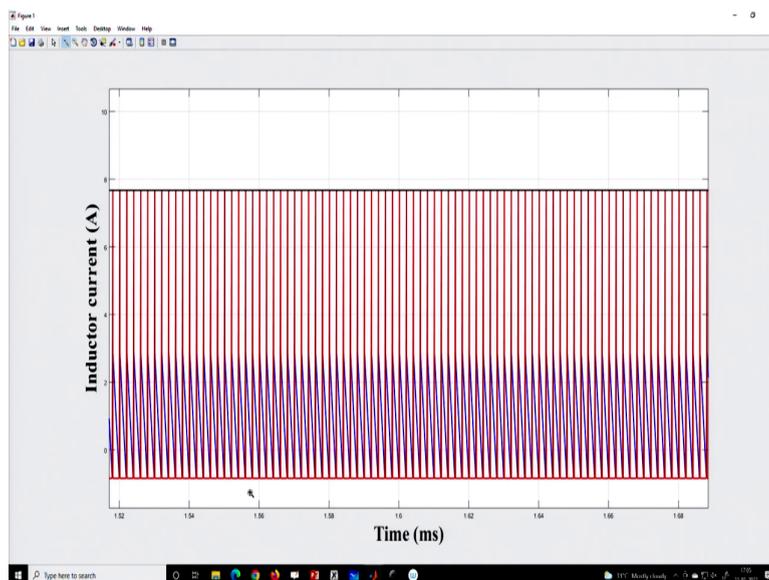
But one can go because if you go to delay, there will be a more advanced level. The analysis will be very complicated and is a research topic.

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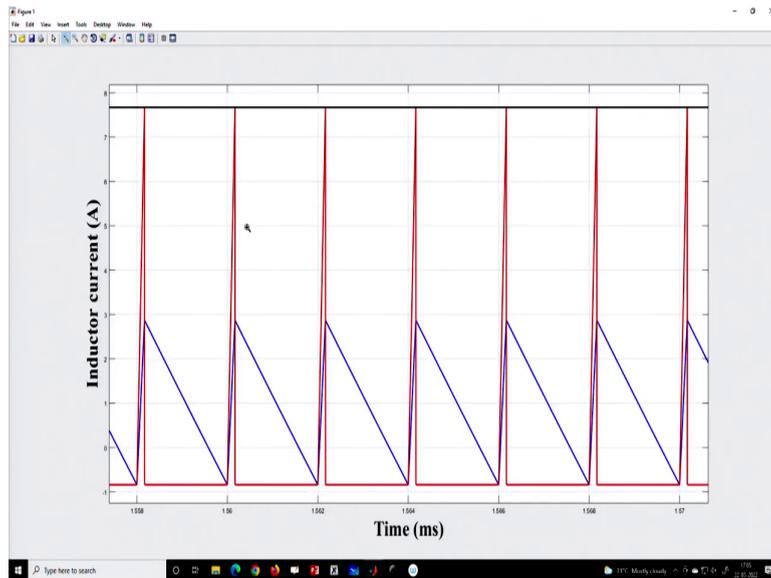


So, in the next part, I want to show the current waveform. So, let us go to the current waveform.

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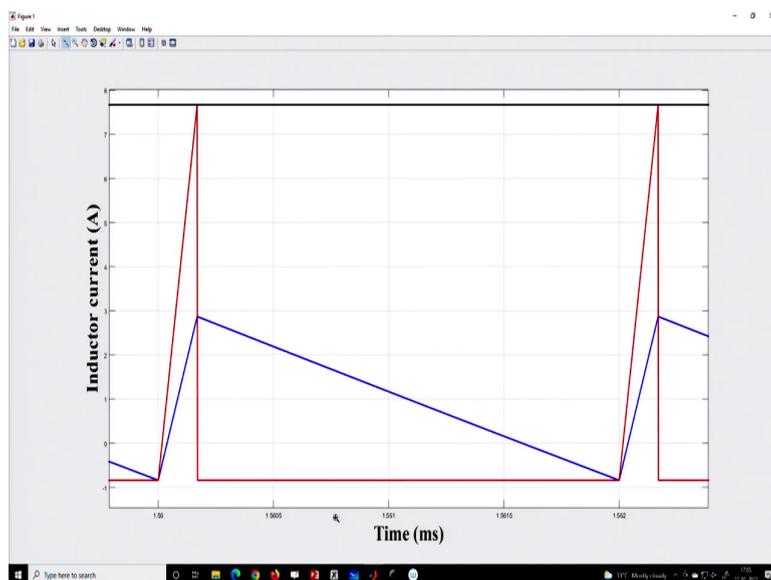


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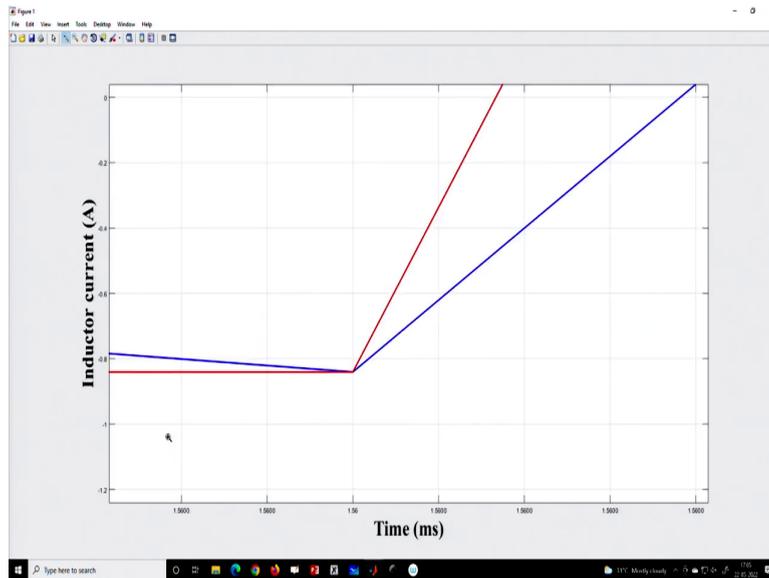
If you go to the current waveform the first thing I will show you now is that if I take one complete cycle.

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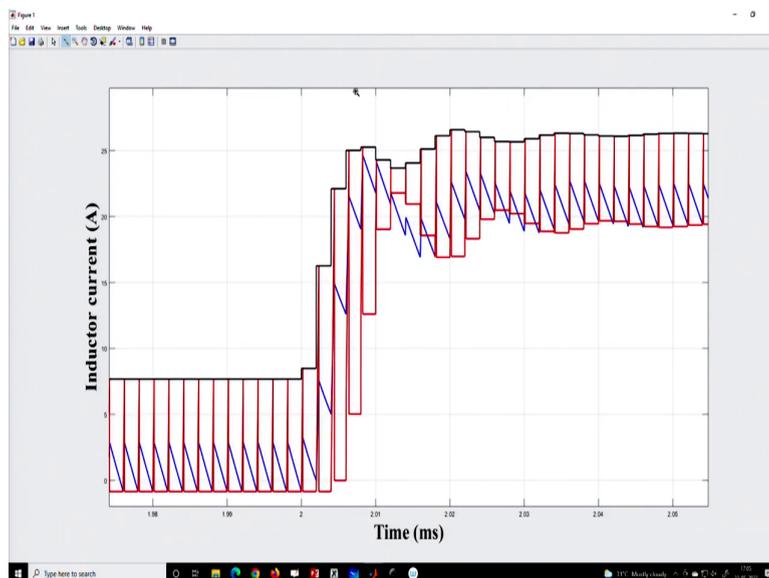
So, you can see the blue one is the actual inductor current which is like a sense inductor current and the red one is an emulated slope; that means, which is much higher. Otherwise, it will be unstable, I will show you.

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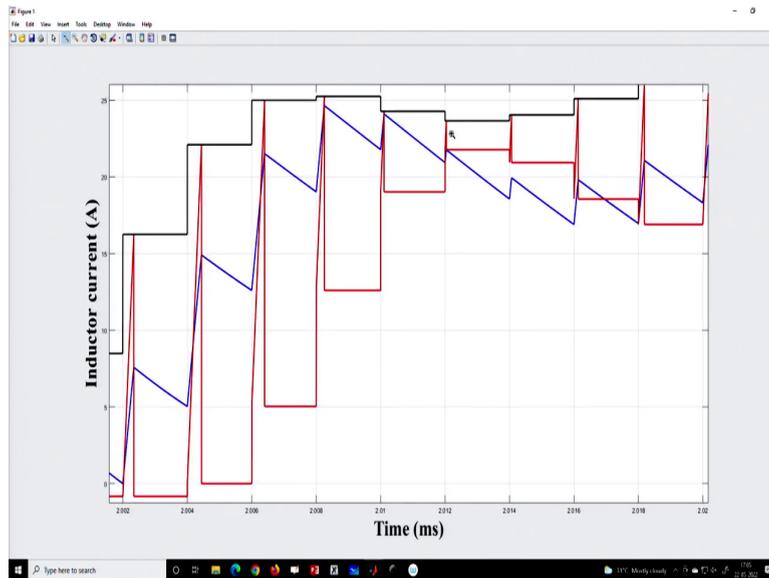
And after adding the sample with the emulated slope you can see here under steady state when it reaches under steady state since the valley point is exactly like repeating every cycle. Then it will look like as if like a sample and then added the ramp.

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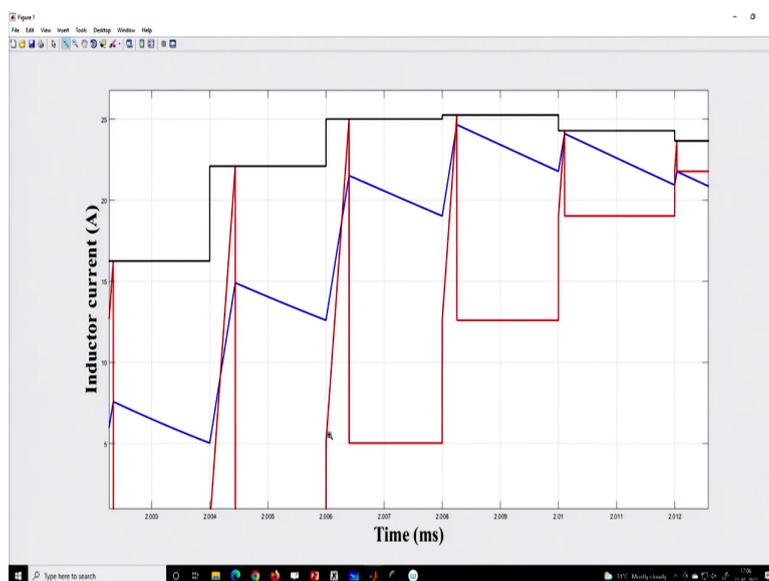
But I will show you the transient case also. But if you take a transient case I am just showing I just want to emphasize.

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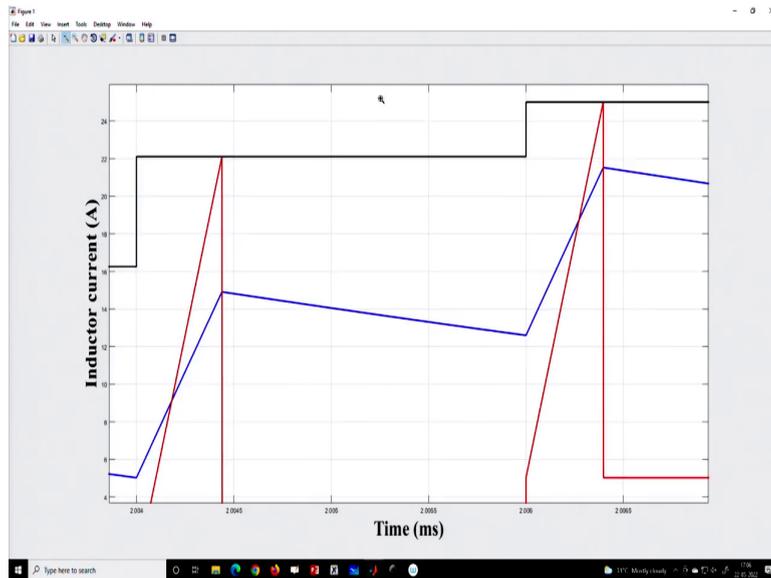
You can see that let us first consider maybe here yeah.

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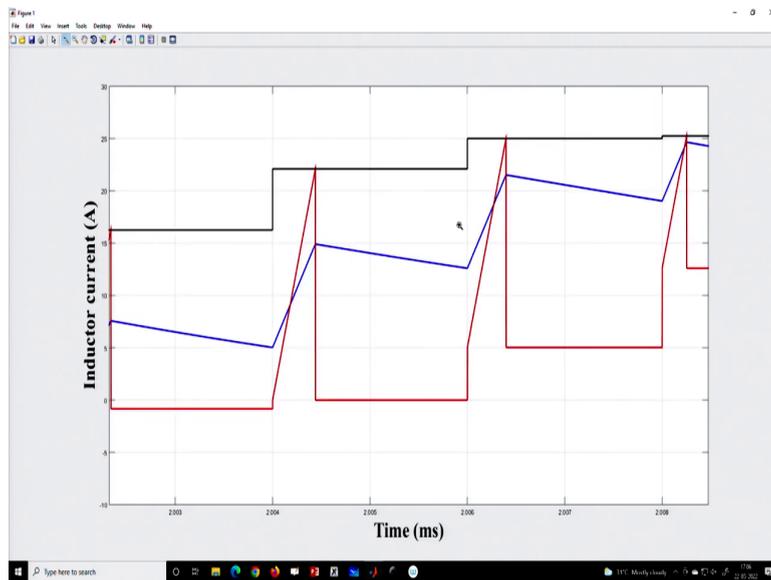
You can see this point this is the inductor current for this cycle. For this cycle, the valley point of the inductor current is here. So, you can interpolate and this is a valuable point.

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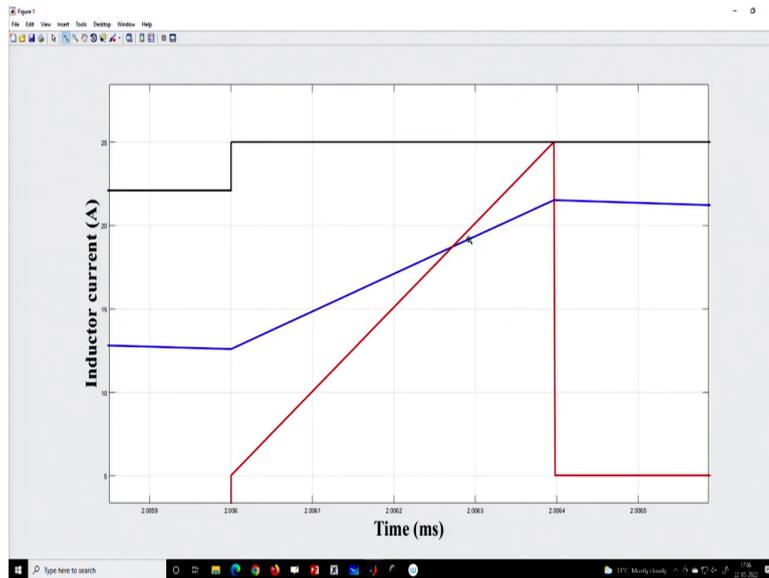
That means, your ramp is added which means if I further zoom this cycle this point is interpolated here, and then we have added this slope.

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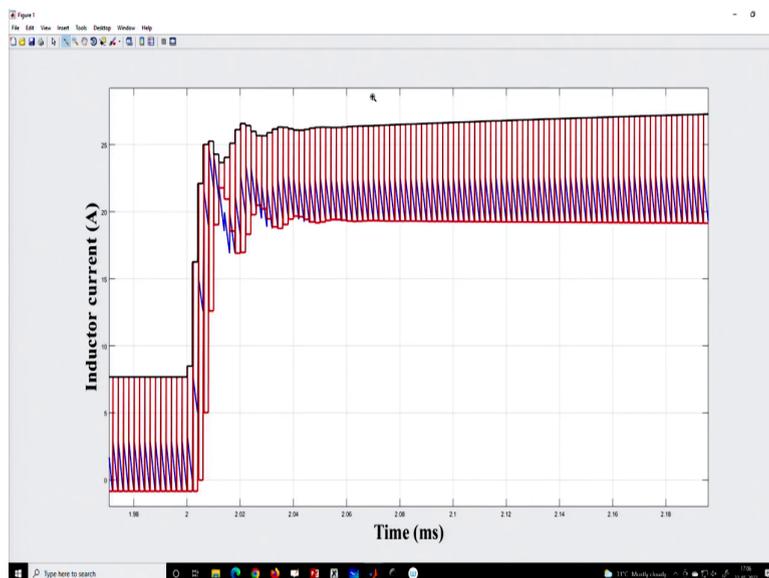
That means if you carefully observe we are making 1 cycle delay. This is your actual inductor current and its sample is used in the next cycle.

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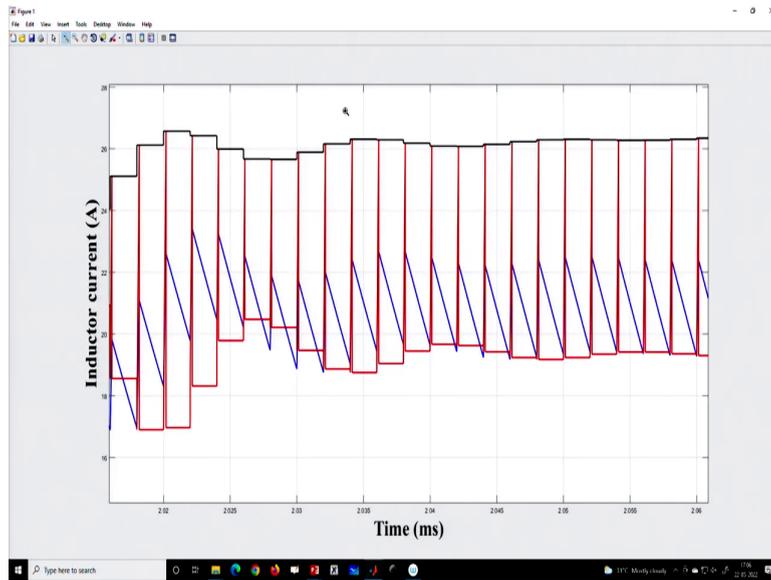


And then we added that m c and after m c this is an emulated ramp plus sample current when the overall current is compared with the peak current. When it hit the peak current the switch is turned off and that is exactly what we have explained.

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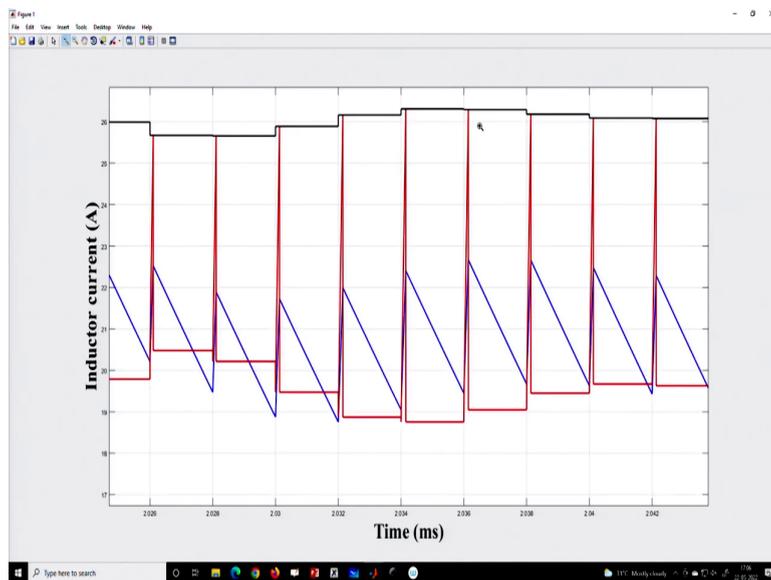


(Refer Slide Time: 23:22)



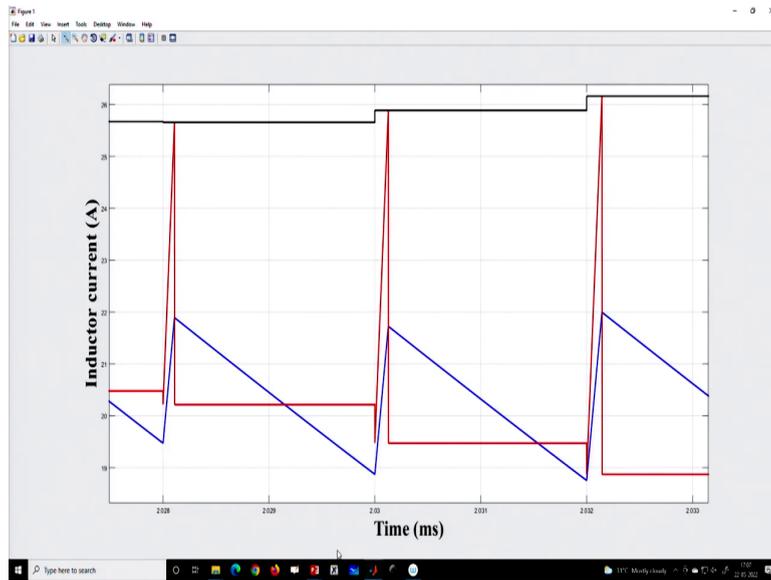
That means if you try to understand this part.

(Refer Slide Time: 23:24)



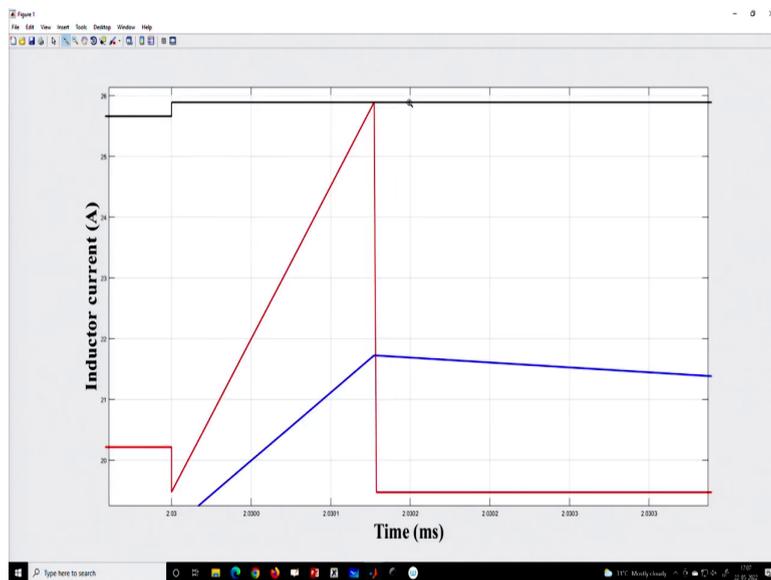
So, if you go to this block take a few cycles.

(Refer Slide Time: 23:27)



So, the inductor current in this sample is used here.

(Refer Slide Time: 23:34)



And we have taken a very large ramp, so otherwise, it will be unstable.

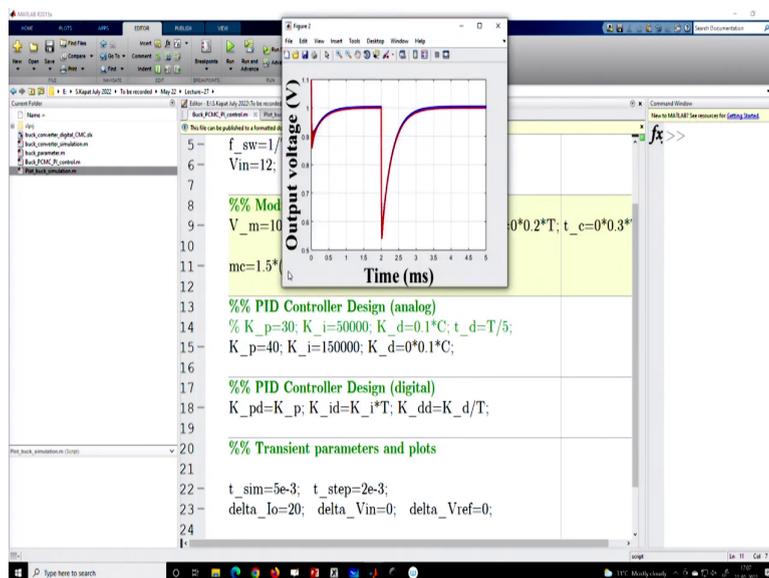
(Refer Slide Time: 23:42)

```
5 f_sw=1/T;
6 Vin=12; Vref=1; R=1;
7
8 %% Modulator gain
9 V_m=10; Fm=1/V_m; tau_d=T/10; t_s=0*0.2*T; t_c=0*0.3*
10
11 mc=1.5*(Vin/L);
12
13 %% PID Controller Design (analog)
14 % K_p=30; K_i=50000; K_d=0.1*C; t_d=T/5;
15 K_p=40; K_i=150000; K_d=0*0.1*C;
16
17 %% PID Controller Design (digital)
18 K_pd=K_p; K_id=K_i*T; K_dd=K_d/T;
19
20 %% Transient parameters and plots
21
22 t_sim=5e-3; t_step=2e-3;
23 delta_Io=20; delta_Vin=0; delta_Vref=0;
24
```

WINDOW: I/O
eliminate this message, set the Algebraic loop option in the Diagnostics page of the Simulation Parameters Dialog to "None"
> In buck_convert
In Buck_PCMC
Found algebraic loop
'buck_convert_
'buck_convert_
'buck_convert_
'buck_convert_
'buck_convert_
fx

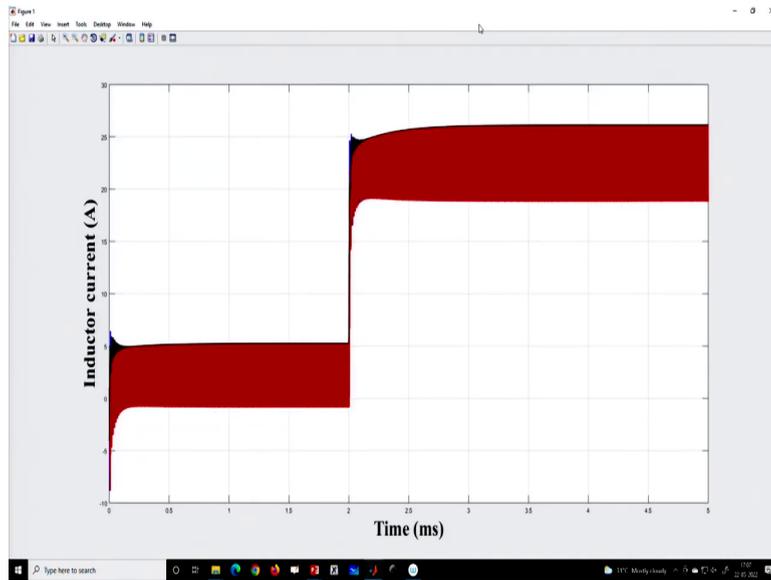
So, let us see if it is 2.1 type. So, if we use a ramp let us say 1.5.

(Refer Slide Time: 23:49)



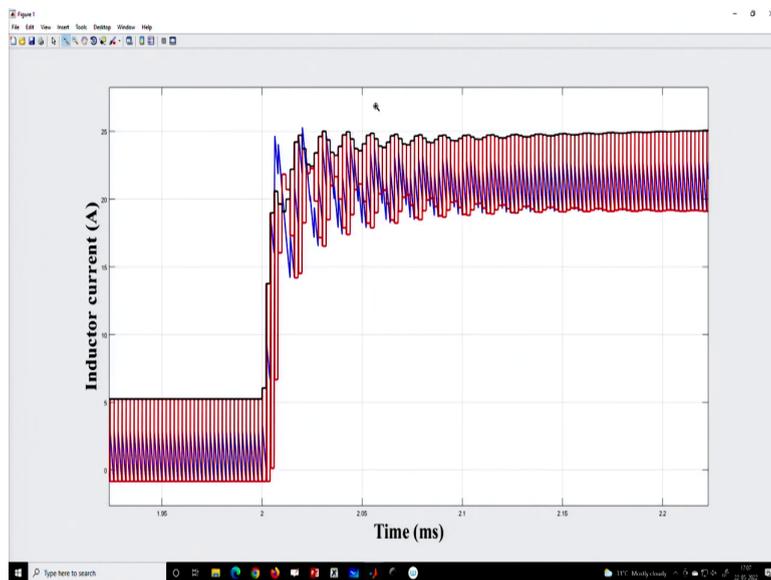
And we want to see it is the Vin by L.

(Refer Slide Time: 23:51)



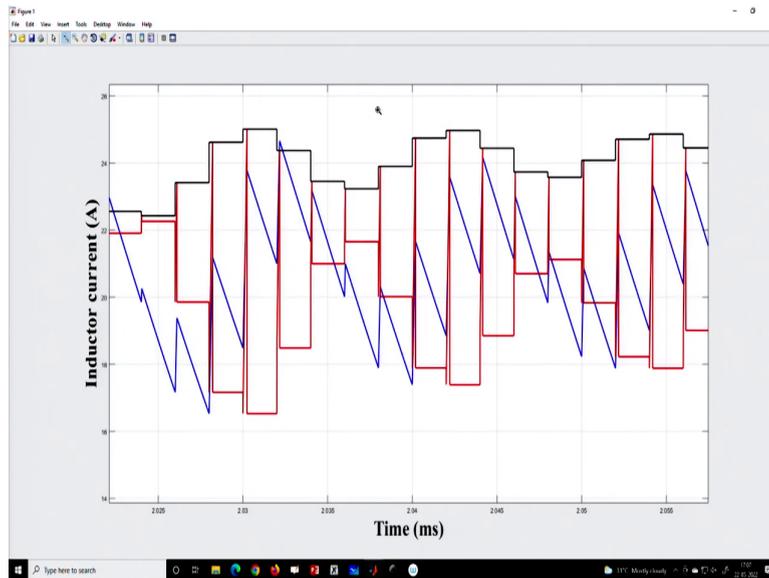
You know we have taken a more conservative slope much more conservative slope.

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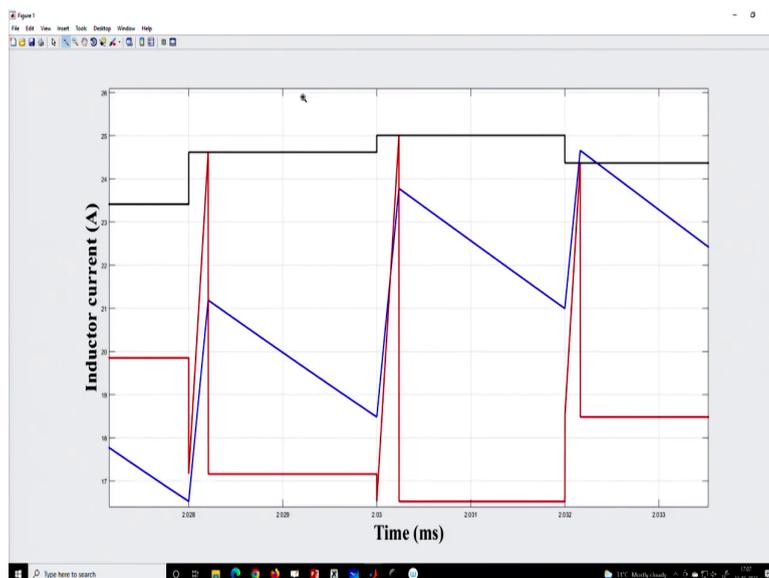


So, although it is stable now.

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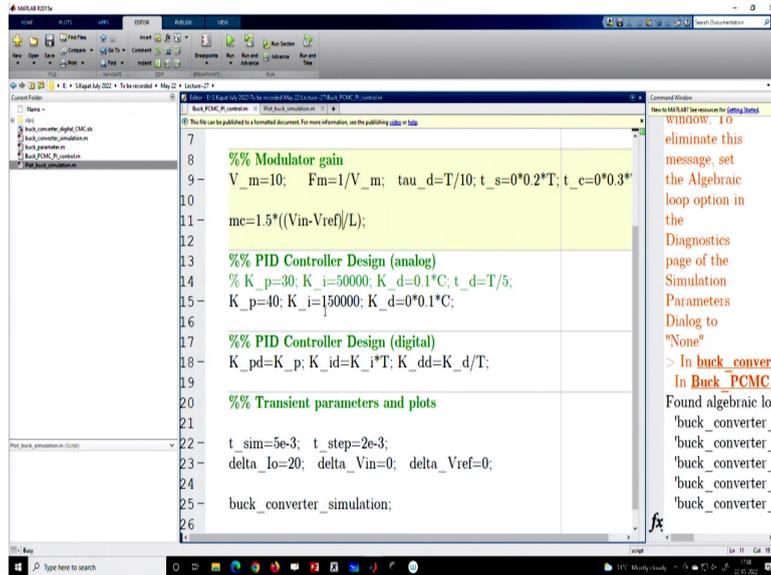


(Refer Slide Time: 24:01)



The slope of this is even higher, but again this operation I am showing. Now suppose if I want to say let us say what is the rising slope of the inductor current?

(Refer Slide Time: 24:14)

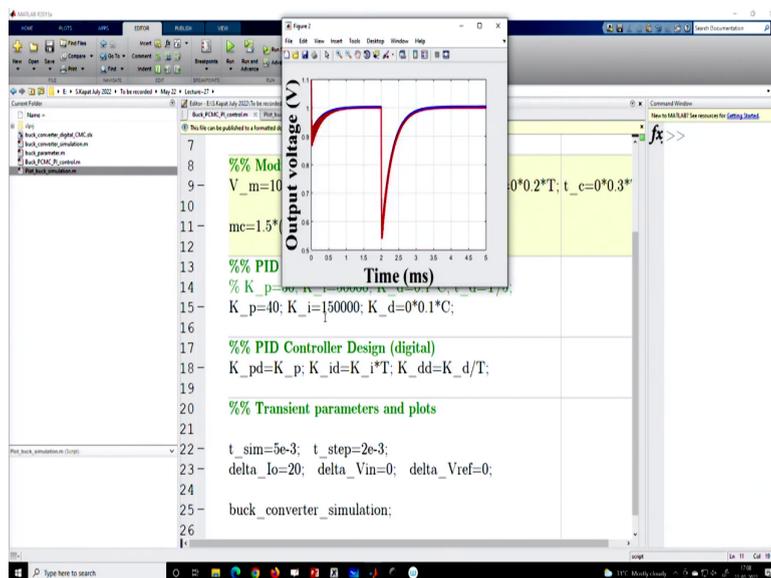


```
7
8
9 %% Modulator gain
10 V_m=10; Fm=1/V_m; tau_d=T/10; t_s=0*0.2*T; t_c=0*0.3*
11
12 mc=1.5*((Vin-Vref)/L);
13
14 %% PID Controller Design (analog)
15 % K_p=30; K_i=50000; K_d=0.1*C; t_d=T/5;
16 K_p=40; K_i=150000; K_d=0*0.1*C;
17
18 %% PID Controller Design (digital)
19 K_pd=K_p; K_id=K_i*T; K_dd=K_d/T;
20
21 %% Transient parameters and plots
22
23 t_sim=5e-3; t_step=2e-3;
24 delta_ilo=20; delta_Vin=0; delta_Vref=0;
25
26 buck_converter_simulation;
```

WARNING: I/O eliminate this message, set the Algebraic loop option in the Diagnostics page of the Simulation Parameters Dialog to "None"
> In buck_convert
In Buck_PCMC
Found algebraic lo
'buck_converter_
'buck_converter_
'buck_converter_
'buck_converter_
'buck_converter_

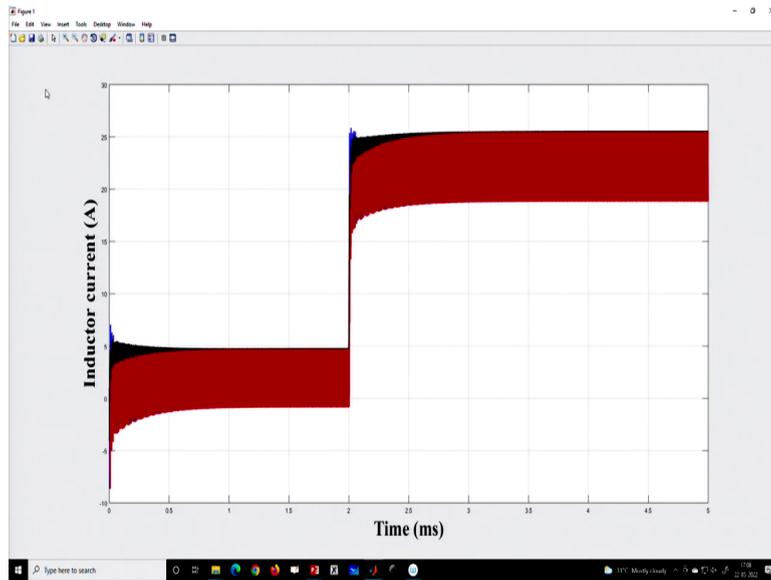
It is something like a V in minus let us say V ref. So, let me check yeah it is V ref.

(Refer Slide Time: 24:36)

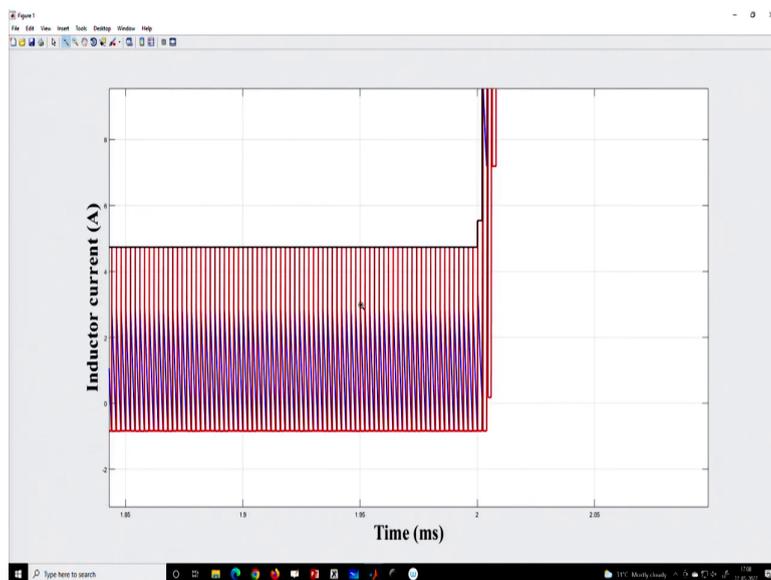


So, suppose I am taking just V in my inductor rising slope 1.5 times. Will it work? Let us see.

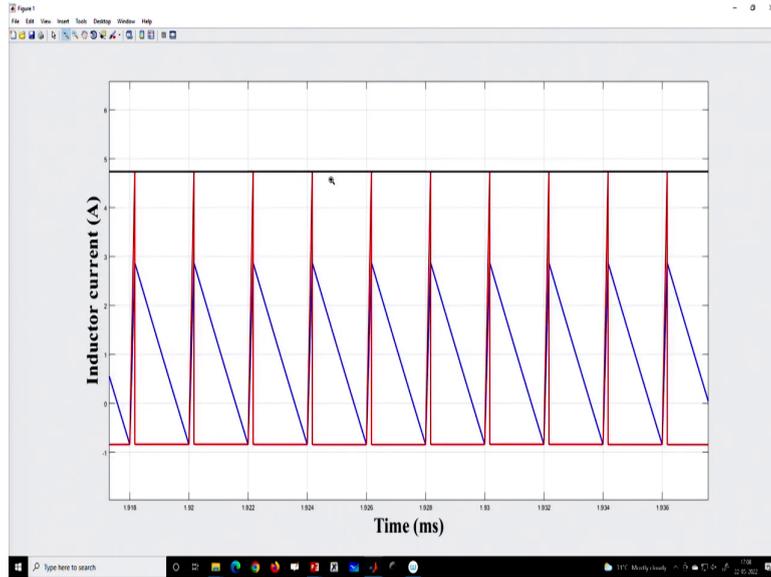
(Refer Slide Time: 24:37)



(Refer Slide Time: 24:42)

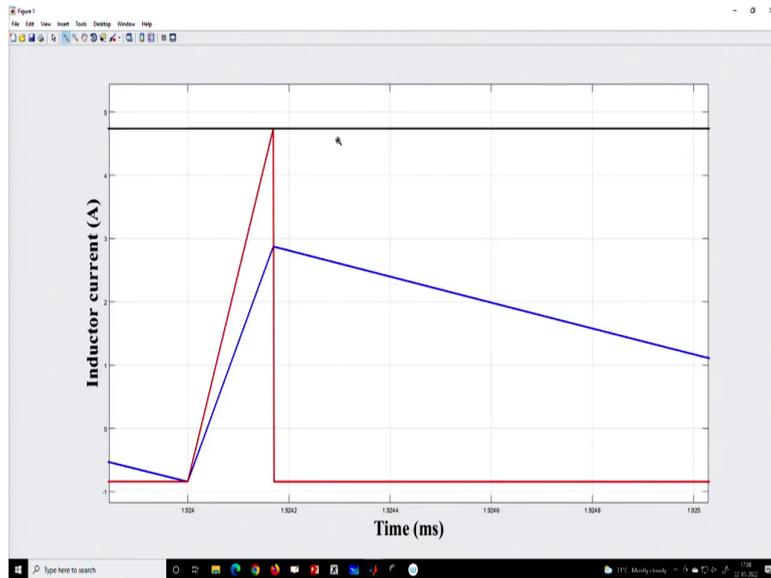


(Refer Slide Time: 24:43)



It is still working, but it is slowly going into sorry it is still working; that means, we have used the slope.

(Refer Slide Time: 24:47)



(Refer Slide Time: 24:57)

```

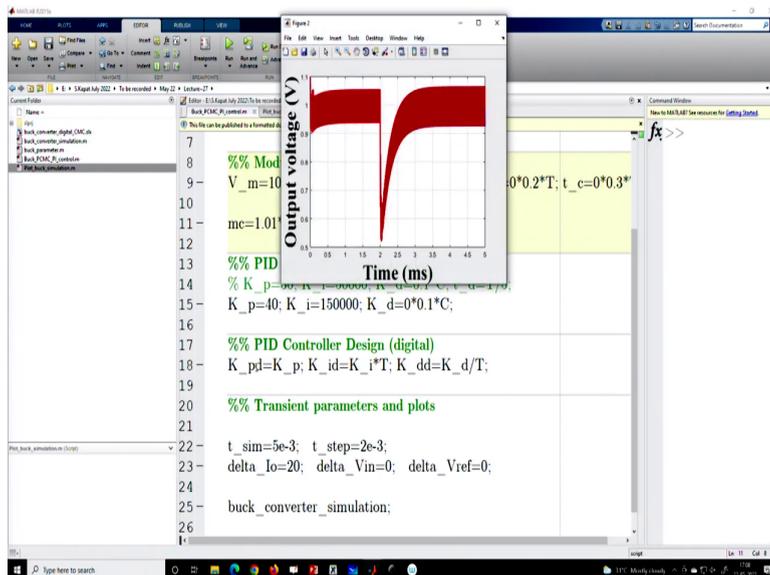
7
8
9 %% Modulator gain
V_m=10; Fm=1/V_m; tau_d=T/10; t_s=0*0.2*T; t_c=0*0.3*
10
11 mc=1.01*((Vin-Vref)/L);
12
13 %% PID Controller Design (analog)
14 % K_p=30; K_i=50000; K_d=0.1*C; t_d=T/5;
15 K_p=40; K_i=150000; K_d=0*0.1*C;
16
17 %% PID Controller Design (digital)
18 K_pd=K_p; K_id=K_i*T; K_dd=K_d/T;
19
20 %% Transient parameters and plots
21
22 t_sim=5e-3; t_step=2e-3;
23 delta_Io=-20; delta_Vin=0; delta_Vref=0;
24
25 buck_converter_simulation;
26

```

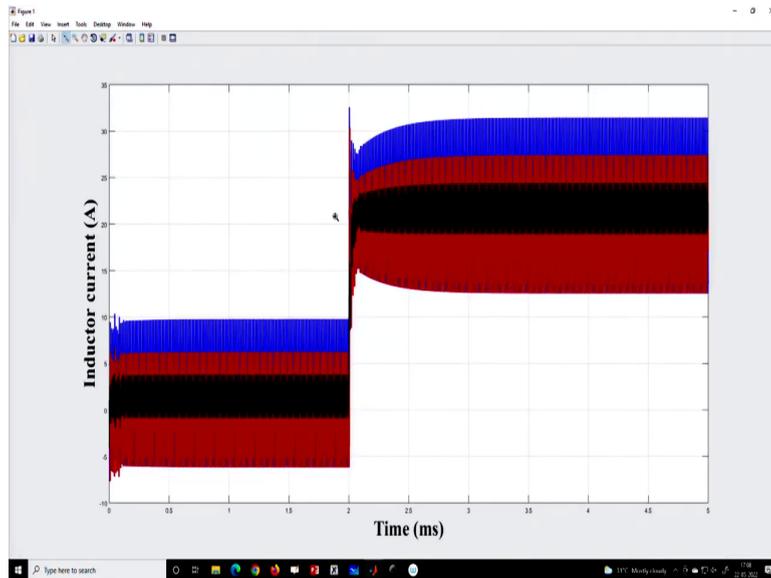
How MATLAB sees resources for getting started
 window 10
 eliminate this message, set the Algebraic loop option in the Diagnostics page of the Simulation Parameters Dialog to "None"
 > In buck_convert
 In Buck_PCMC
 Found algebraic lo
 'buck_converter_
 'buck_converter_
 'buck_converter_
 'buck_converter_
 'buck_converter_

If you see just 1.5 times, but suppose we make it just the same or maybe 0.01 just slightly above it must be unstable that I can show.

(Refer Slide Time: 25:03)

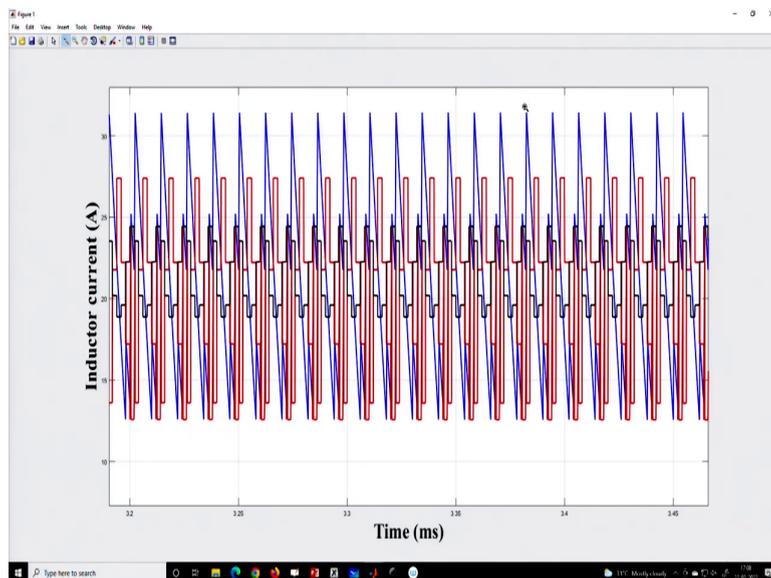


(Refer Slide Time: 25:05)



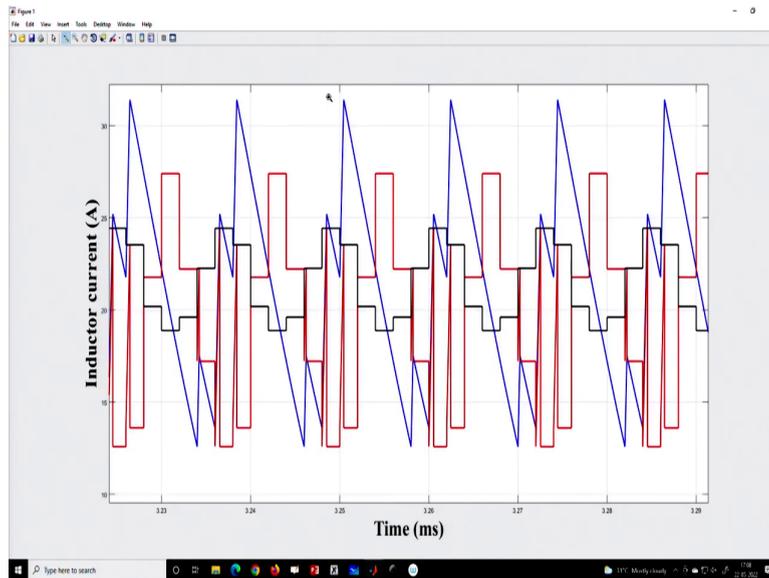
And it is unstable. You can see there is a subharmonic instability that is coming.

(Refer Slide Time: 25:09)



Because the current loop is unstable.

(Refer Slide Time: 25:11)



And when you go to the analysis part it will be shown that you need this is nothing, but m_1 plus m_2 plus; that means, the m_c should be greater than the sum of m_1 plus m_2 . m_1 is the rising slope.

(Refer Slide Time: 25:29)

```

7
8
9 %% Modulator gain
10 V_m=10; Fm=1/V_m; tau_d=T/10; t_s=0*0.2*T; t_c=0*0.3*
11 mc=1.2*((Vin-Vref)/L);
12
13 %% PID Controller Design (analog)
14 % K_p=30; K_i=50000; K_d=0.1*C; t_d=T/5;
15 K_p=40; K_i=150000; K_d=0*0.1*C;
16
17 %% PID Controller Design (digital)
18 K_pd=K_p; K_id=K_i*T; K_dd=K_d/T;
19
20 %% Transient parameters and plots
21
22 t_sim=5e-3; t_step=2e-3;
23 delta_Io=20; delta_Vin=0; delta_Vref=0;
24
25 buck_converter_simulation;
26
t

```

That means if you go to let us say what is; that means, that will be discussed in the theory; that means, I am saying the m_c should be greater than m_1 plus m_2 . And in a buck converter, what is m_1 ? It is V in minus V_0 by L .

And what is m_2 ? It is V_0 by L . Then what is m_1 plus m_2 ? It is simply V in by L . So, that is why we have taken. If we just m_c is above V in by L , then it should be stable and we are going here.

(Refer Slide Time: 26:06)

```

7
8 %% Modulator gain
9 V_m=10; Fm=1/V_m; tau_d=T/10; t_s=0*0.2*T; t_c=0*0.3*
10
11 mc=1.01*(Vin/L);
12
13 %% PID Controller Design (analog)
14 % K_p=30; K_i=50000; K_d=0.1*C; t_d=T/5;
15 K_p=40; K_i=150000; K_d=0*0.1*C;
16
17 %% PID Controller Design (digital)
18 K_pd=K_p; K_id=K_i*T; K_dd=K_d/T;
19
20 %% Transient parameters and plots
21
22 t_sim=5e-3; t_step=2e-3;
23 delta_lo=20; delta_Vin=0; delta_Vref=0;
24
25 buck_converter_simulation;
26

```

Command Window:

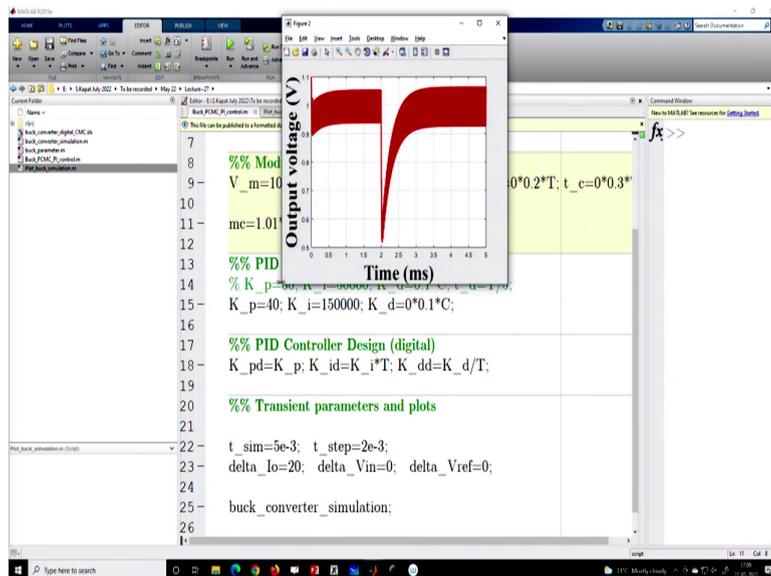
```

Warning: In buck_converter_simulation: Found algebraic loop in block 'buck_converter_...'.

```

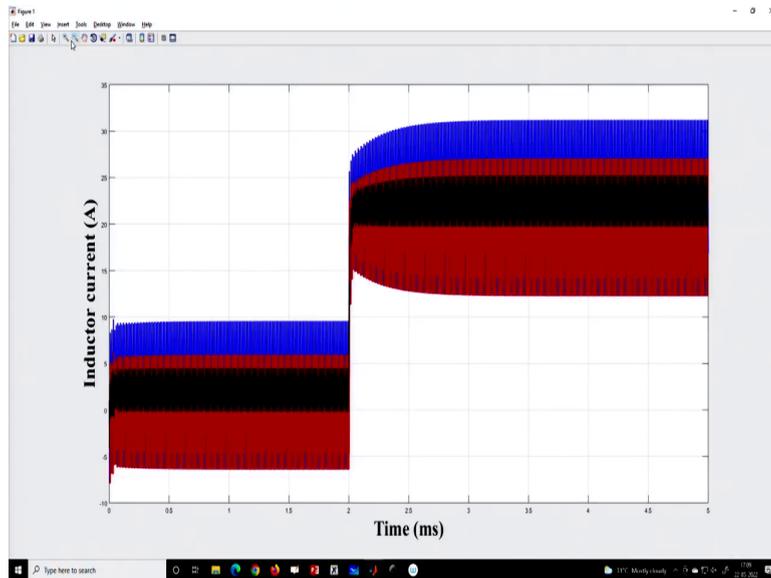
That means, initially what we have considered is if we just take V in just 1.0 time. This is a verge of very close to the instability we are considering very close, it is even unstable.

(Refer Slide Time: 26:18)

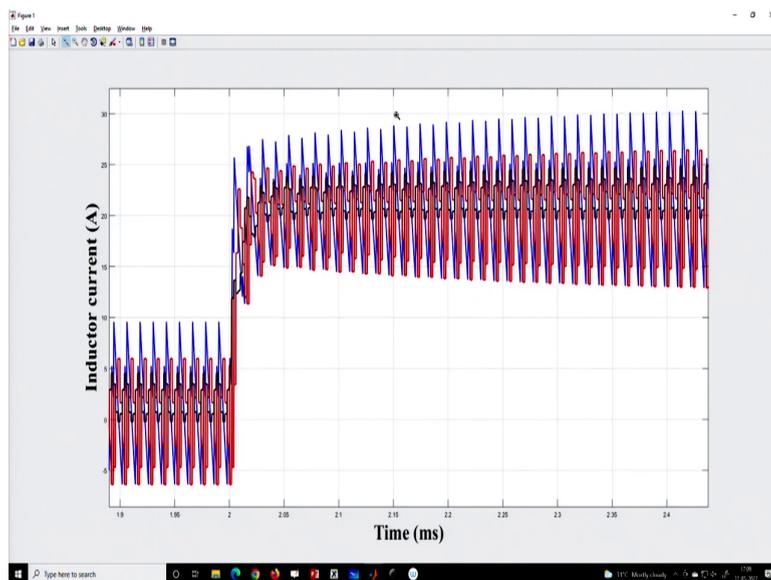


And I will show I mean it research paper there is a research paper.

(Refer Slide Time: 26:19)

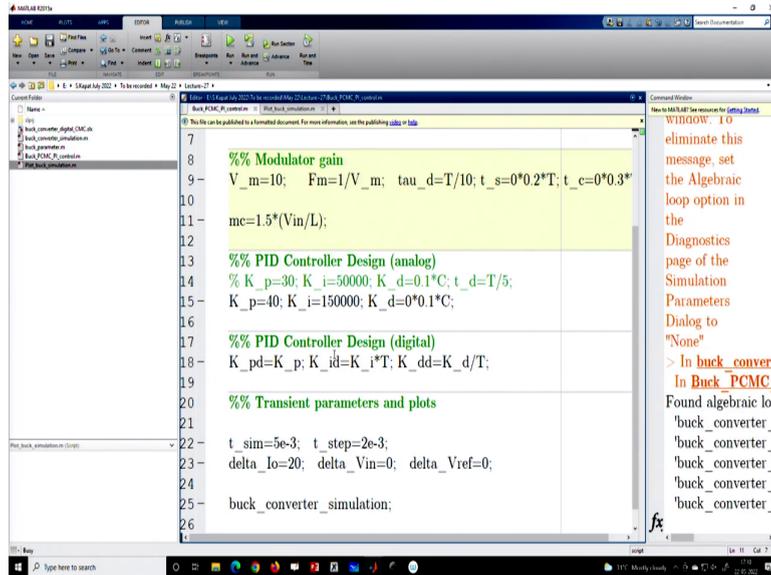


(Refer Slide Time: 26:24)



When we will go to analysis, even even if you make it higher it is not enough when you close the outer loop. Again these are research topics.

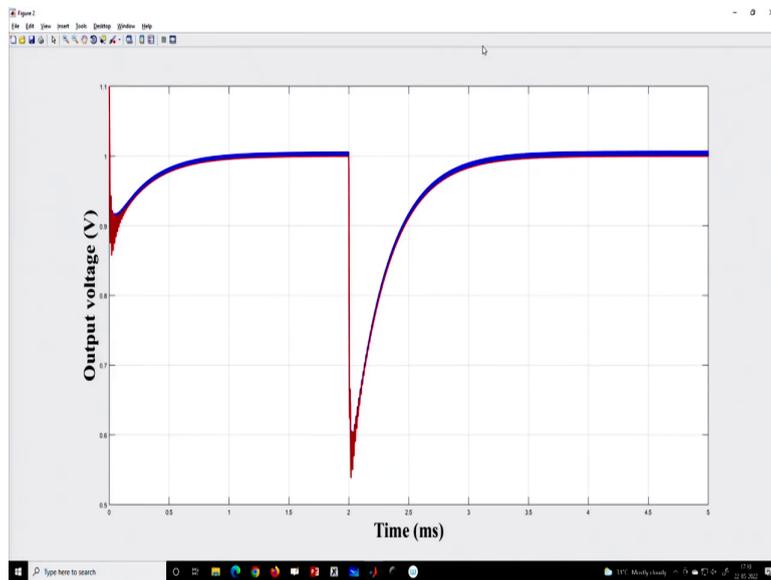
(Refer Slide Time: 26:36)



```
7  
8 %% Modulator gain  
9 V_m=10; Fm=1/V_m; tau_d=T/10; t_s=0*0.2*T; t_c=0*0.3*  
10  
11 me=1.5*(Vin/L);  
12  
13 %% PID Controller Design (analog)  
14 % K_p=30; K_i=50000; K_d=0.1*C; t_d=T/5;  
15 K_p=40; K_i=150000; K_d=0*0.1*C;  
16  
17 %% PID Controller Design (digital)  
18 K_pd=K_p; K_id=K_i*T; K_dd=K_d/T;  
19  
20 %% Transient parameters and plots  
21  
22 t_sim=5e-3; t_step=2e-3;  
23 delta_io=20; delta_Vin=0; delta_Vref=0;  
24  
25 buck_converter_simulation;  
26
```

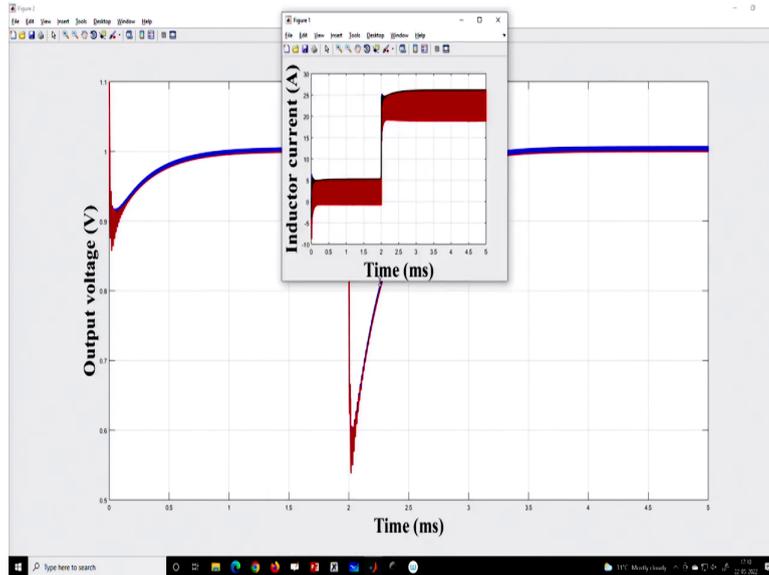
But I can say that we need to take sufficiently a conservative choice of this. So, that it will be stable. So, we have to make sure the current loop is closed.

(Refer Slide Time: 26:43)



Because if we increase and you can see it is stable it is stable.

(Refer Slide Time: 26:49)

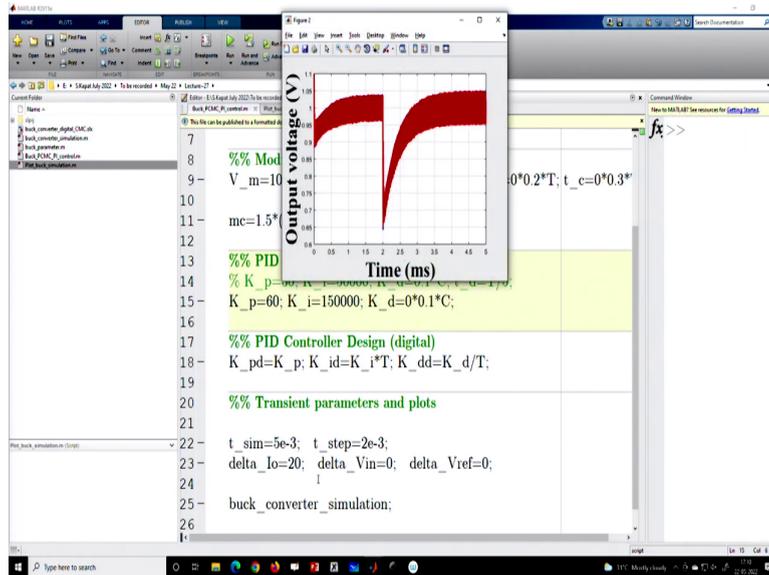


(Refer Slide Time: 26:56)

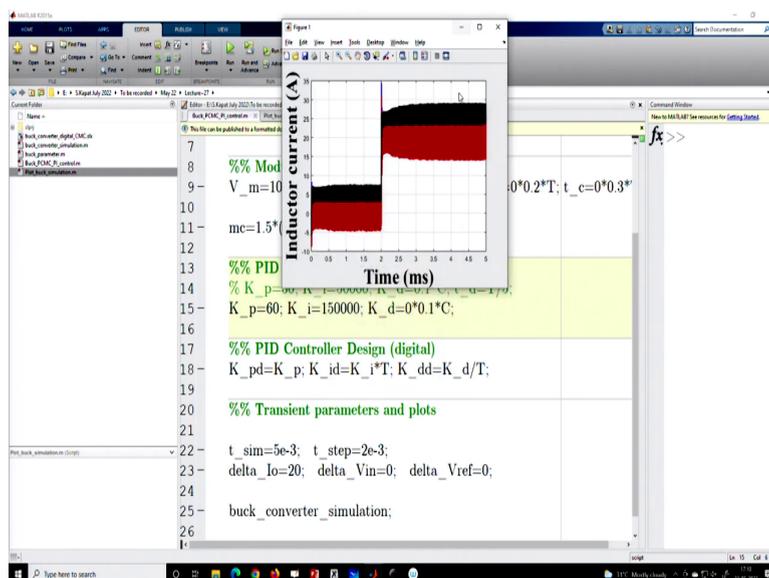
```
7  
8 %% Modulator gain  
9 V_m=10; Fm=1/V_m; tau_d=T/10; t_s=0*0.2*T; t_c=0*0.3*  
10  
11 mc=1.5*(Vin/L);  
12  
13 %% PID Controller Design (analog)  
14 % K_p=30; K_i=50000; K_d=0.1*C; t_d=T/5;  
15 K_p=60; K_i=150000; K_d=0*0.1*C;  
16  
17 %% PID Controller Design (digital)  
18 K_pd=K_p; K_id=K_i*T; K_dd=K_d/T;  
19  
20 %% Transient parameters and plots  
21  
22 t_sim=5e-3; t_step=2e-3;  
23 delta_lo=20; delta_Vin=0; delta_Vref=0;  
24  
25 buck_converter_simulation;  
26  
t
```

But suppose if we make this controller if we make 60; that means we have increased the controller gain and see what happened. Is it still really stable?

(Refer Slide Time: 27:01)



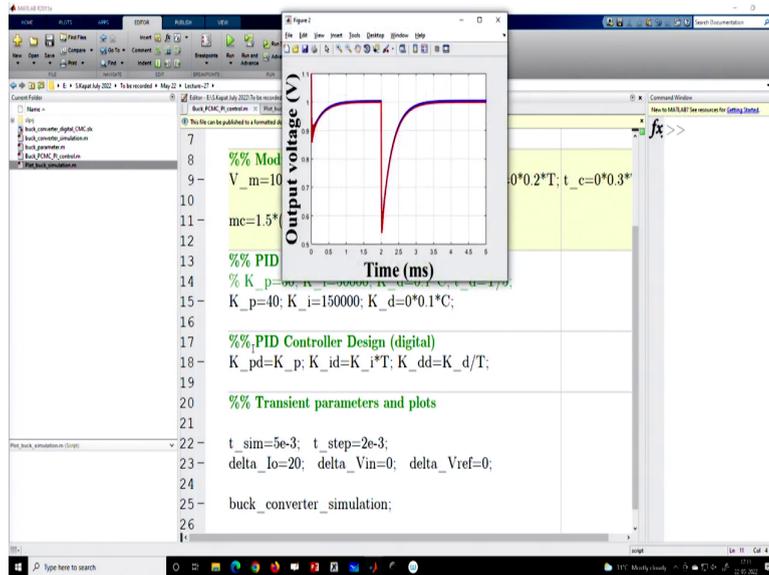
(Refer Slide Time: 27:03)



So, it becomes unstable; that means, the choice of the slope also depends on the closed loop there is a research paper, but again I am not discussing it. I am just showing that you know you need to be careful about this design and we are not going to consider the design of full digital current because this is a more advanced topic, but it gives you some kind of motivation that you know this is a very interesting problem.

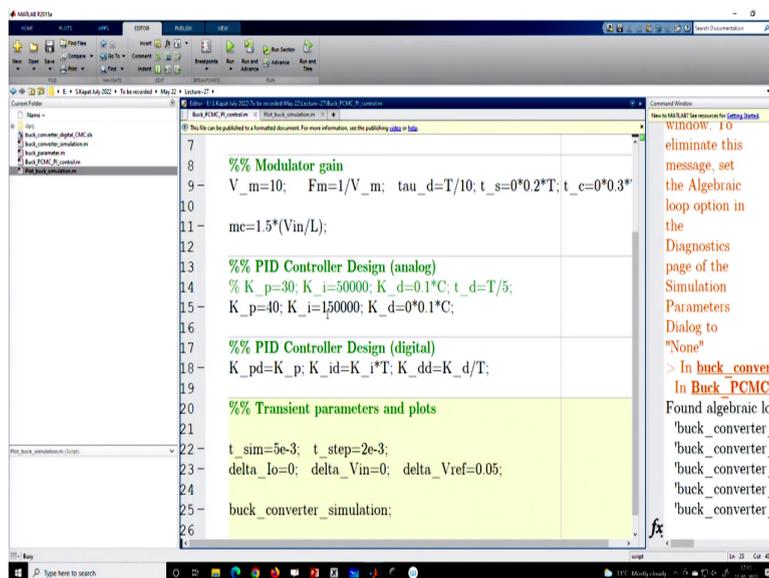
And you know you have to be careful about the selection of an outer voltage loop otherwise you will end up with instability.

(Refer Slide Time: 27:31)



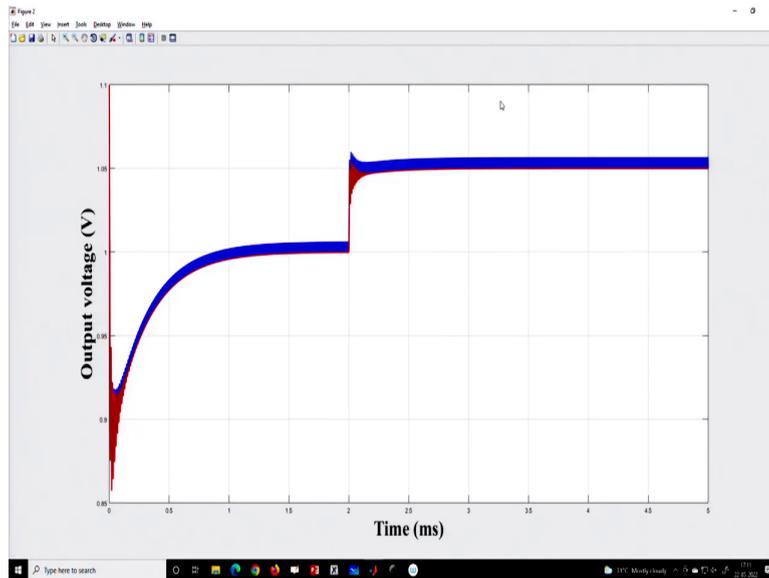
So, you can also perform here I did load transient.

(Refer Slide Time: 27:36)



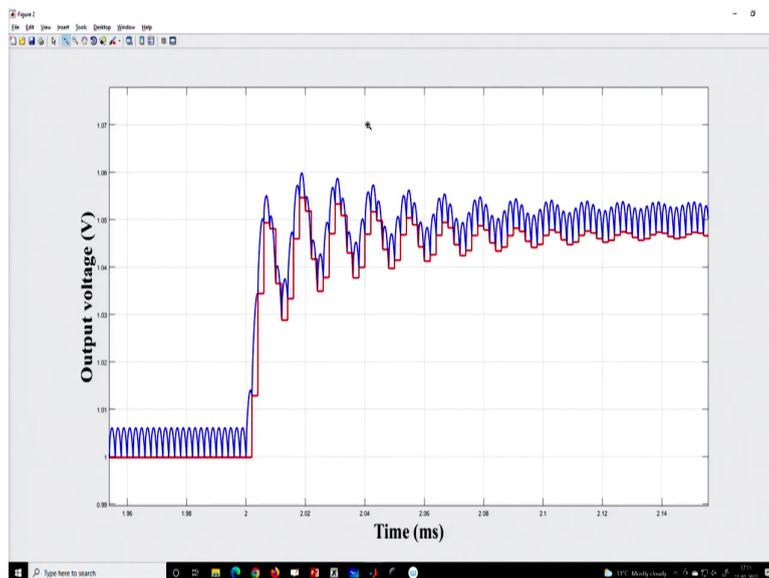
You can do reference transient and you can carry out the same reference transient that we have performed for mixed-signal current mode control ok.

(Refer Slide Time: 27:45)



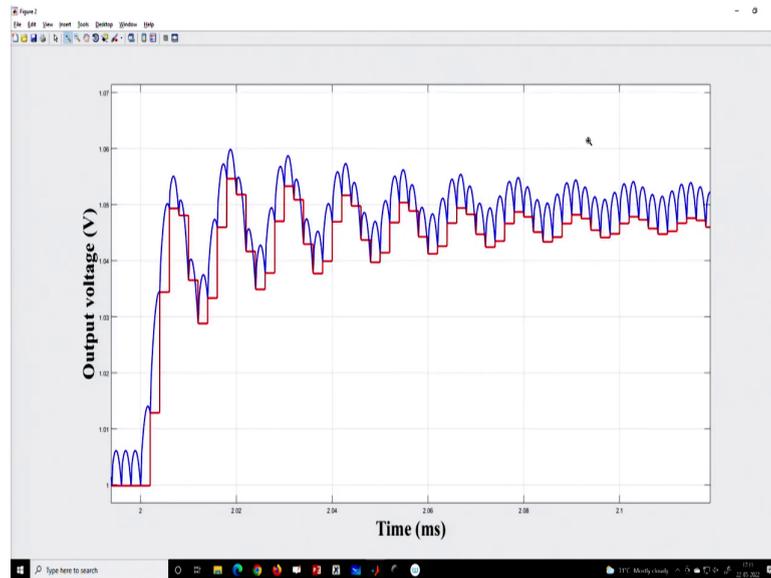
But, because this is on sample delay.

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You can see there is some kind of oscillatory behavior.

(Refer Slide Time: 27:52)



Because any delay will cause the phase margin I mean to degrade the phase margin and because of that poor phase margin, it will also become more oscillatory ok.

(Refer Slide Time: 28:09)

CONCLUSION

- Custom MATLAB model development for fully digital current mode control
- MATLAB simulation studies

So, we need to be careful about this design process ok. So, in summary, we have discussed custom MATLAB model development for fully digital current mode control and we have discussed we have considered a few MATLAB simulation case studies.

So, here we want to finish the fixed frequency digital current mode control implementation. In the next lecture, we are going to talk about variable frequency digital current mode control. So, with this, I want to finish it here.

Thank you very much.