Control and Tuning Methods in Switched Mode Power Converters
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Module - 12
Performance Comparison and Simulation
Lecture - 59
Challenges and Opportunities in Digitally Controlled High Frequency SMPCs

Welcome this is lecture number 59. In this lecture, we are going to talk about Challenges and Opportunity in Digitally Controlled High Frequency Switched Mode Power Converter.

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So, in this lecture, we will first talk about stability aspect in digital control; particularly the effect due to quantization and sampling. Again, this lecture is just a brief introduction to digital control. We are just highlighting some key issue, but the digital control can be a separate course..

Because here, we are just showing at the end that whatever we have learned in the previous lecture, if we can want to do in digital control, then what type of architectures are available, what may be their impact in stability and what are the opportunities that we can move forward.

But, in actual digital control had many more things. Then, we can say modeling and analysis of digitally controlled DC-DC converters and then, opportunity using variable frequency digital control architecture.

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So, first, we will recall our fixed frequency you know high frequency voltage mode control DPWM and DPWM here stands for Digital Pulse Width Modulator architecture; Digital Pulse Width Modulator architecture and this you have learned; that means, your output voltage is sampled in digital domain.

Then you know it is compared with reference and generating the error voltage, then you have a compensator and then the controller output is compared with a sawtooth waveform. The sawtooth is also generated inside the digital controller, and the comparator is a digital comparator.

So, that means, it does not require much of (Refer Slide Time: 01:56). It is very simple and then, the whole you know there will be dead time and Half-Bridge gate drive; the dead time can be generated from here and then, we can actually control the switch. So, here the benefit we have discussed that is a reconfigurable..

This can control. We can do real time energy optimization. We can implement this whole block up to this switch, including the switch. The whole block can be inside one IC right. So,

this block and we can do very fast prototyping because HDL port, we can plug in into FPGA, do prototyping and that very log code, we can use to synthesize our actual as if.

Then, this digital control also provides the power management bus interface for interaction between multiple converter because most of the system portable device that will use that have multiple converter. So, there should be an interaction between them or communication.

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We have also shown in the lecture number 57 the effect due to quantization in digital control. If we actually consider the sense voltage here and then, we have an A/D converter right and this is our voltage loop sense discretize, or the digitized voltage; it is compared to the reference voltage and the compensator and a DPWM..

Now, if there will be a clock right because we can initially assume or basically the very simple because, for the time being here, we are assuming there is a counter. It is just incrementing, and that is basically your kind of digital pulse width modulator. And this increment size depends on the clock, t clock at which clock you are using the time period of the clock and which is used to increment this counter..

So, t clock by T switching period is my duty ratio resolution because this will set the minimum resolution of the duty ratio that can be achieved and if you take a smaller and smaller clock time period for a given switching period, then you can reduce the duty ratio resolution.

Because this duty ratio resolution plays a significant role in the stability of the digital control, in the particular, the quantization effect. If the resolution of the duty ratio is poor than that means, DPWM resolution the delta d the ADC because ADC will also have a resolution right.

Then what will happen? The quantized voltage, this may not be mapped all the time here and here. It may be mapped in between and if so, mapped in between, then actually you cannot get the perfect duty ratio. As a result, the duty ratio will back and forth between its upper and lower limit and that may lead to limit cycle oscillation. So, exact duty ratio may not be achievable..

So, you may not be able to lock the error voltage inside the zero-error-bin. What is zero-error-bin? Suppose, if this corresponds to the actual output voltage, this control voltage; that means, this voltage if it is not mapped to a particular number, then the error voltage here. So, error quantized error voltage will not be 0 at steady state. Because you want the quantized error voltage to be 0 at steady state so that it will become particularly become a number, then it is a constant number.

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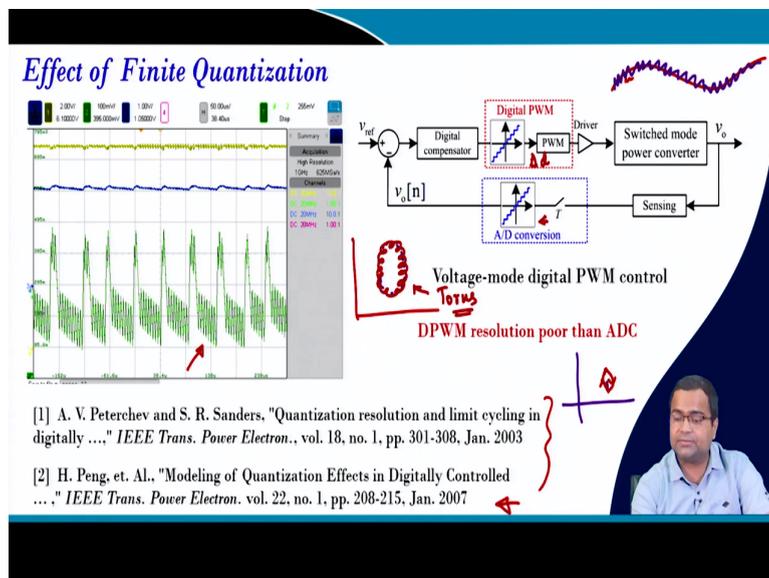
So, if this is coarser; that means, DPWM resolution poor than ADC, then you will end up with limit cycle oscillation and this has been well reported and these two are very highly cited paper. So, initially, you know it was shown the steady state effect; that means, the resolution effect and then subsequently, this paper shows the dynamic impact is also very important..

So, if we take into account this quantization aspect, then this may not look like a limit cycle. It is like more non-linear phenomena but a limit cycle means there is a slow scale oscillation like this on top of the actual switching converter frequency. That means, this is your converter switching frequency can be much faster and you have a like a slow scale oscillation and that we typically consider limit cycle oscillation.

But, generally, switching converter in the fastest sense, it also is a limit cycle. But, that means, we have learned in the phase plane geometry, that means, switching converter itself has a limit cycle because on off operation. But, this limit cycle corresponding to each of this profile, they are very high frequency. But here, we are talking about another limit cycle which is very slow. So, it may look like in the phase plane, it may look like something like this..

That means, due to the limit cycle, you will have this kind of oscillation and on top of that, you are getting you know this limit cycle oscillation. It will look like this. So, this kind of behaviour you can find. So, it will actually chatter around this behaviour. So, it will create lobe around this and it will move on with this ok. So, it will something like a torus.

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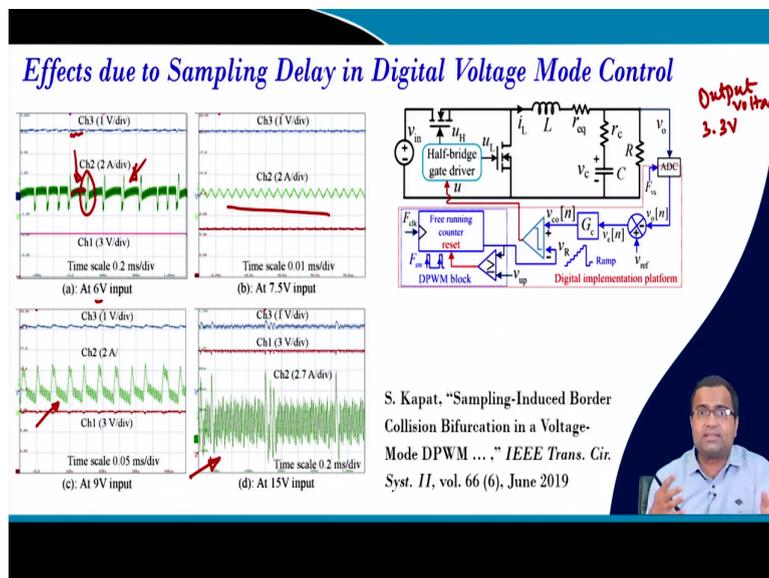
But, actually we have just talked about the effect due to quantization; that means you have to make sure that the resolution of the duty ratio, this duty ratio where we are getting delta d here, must be finer than the resolution of the ADC. But, this is not sufficient because we have discussed in the previous class, there is a sample delay right and that delay is quite significant and what was not investigated earlier that what could this delay make..

I mean along with this, can it do? So, this is one of the scenario, where you can see this is a different input voltage of the buck converter at 6 volt. So, here the output is 3.3 volt. This is my output voltage; my output voltage is 3.3 volt. Now, if you operate at 6 volt, there is a voltage mode control. You see during this particular time, your duty ratio actually your error voltage as if get locked to the 0 error beam, and it stays and you can see from the output voltage profile, it stays and in this time, the error voltage quantized error voltage becomes 0..

So, output of the controller looks like a fixed number and that will lead to some natural or the open loop behaviour of the converter and due to which slowly it is increasing and it can hit the upper limit. Once it hit the upper limit, it again goes out of this band and, by that way, it may not ever settle into this. But, this is even with satisfying all these DPWM quantization criteria.

Now, if you increase the input voltage, you will get some point is perfectly stable behaviour; that means, it is periodically repeated. There is no limit cycle, nothing. Now, if you further increase, you may end up with somewhere, where it is something similar to the limit cycle, but not exactly limit cycle. So, it is a non-linear complex phenomenon, though it can be sometime you know there is a slow scale; I will not say oscillation, but periodicity, but this kind of behaviour is sometime called a coexisting attractor.

But, if you further increase the input voltage, then you may land up with a situation, where your duty ratio can saturate and it will lead to very large ripple in the current and filter and this may not be the only cause due to the quantization because as if here the quantization criteria is satisfied. So, what was the issue? Here it was due to the sampling and why it is so?
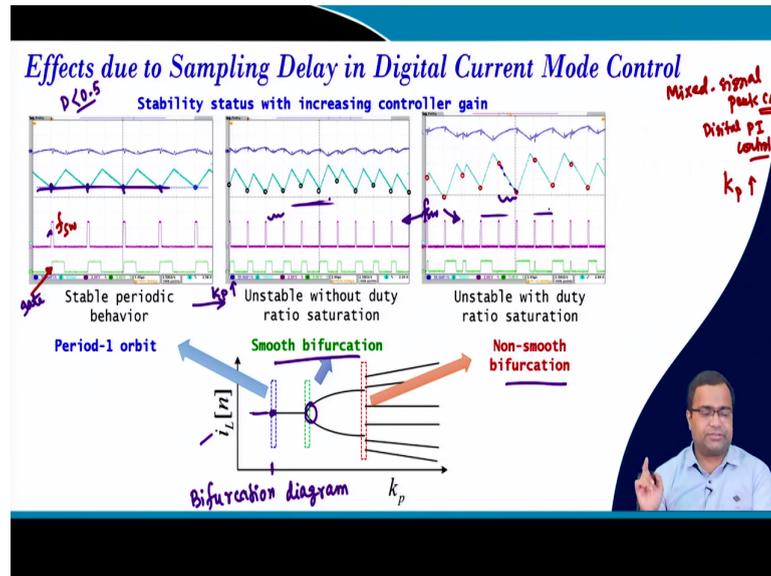
Now, consider, so that we will discuss because we have in this paper, we have discussed that this the cause of sampling can be it can severely impact the stability of the system; whereas, the quantization is kind of steady state behaviour and that will cause some slow scale oscillation..

But, the sampling can lead to drastically different non-linear phenomena and in most of the cases, it leads to duty ratio saturation, where your RMS current everything increases drastically. Now, before we go into see what is the reason. If we take current mode control, the same scenario can happen; how? Suppose, here I am showing a peak current mode control mixed signal peak current mode control.

We are talking about a mixed signal peak current mode of control; that means, mixed signal peak current mode control in which the outer loop voltage loop is in digital and that is sample one for cycle. But, the current loop is in analog and that we have already discussed in the previous class..

Here, we are first operating at a lower proportional gain. So, it is we are using a PI; the digital PI controller, we can say digital you know digital PI controller, where k i is fixed and k i will have hardly any impact on such kind of stability; but we are changing k p, we are increasing k p. For lower value of k p, you can see this is our switching clock, this is our f s w clock, and this is our duty ratio or I will say gate signal, this is our gate signal.

So, this is our gate signal ok. So, you can see, it is repeating at every size rising of the clock, the current is representing it is very perfectly stable behaviour. But, if you go for next, this is again our switching clock; but they are not repeating, that means, there is something instability and we can see the suburban instability in current mode control often. But, this is with very low duty ratio operation. You can see the duty ratio is much lower than 50 percent, much lower than 50 percent..

This is when we change, we increase the k p; that means, we have increased the k p. But, here in every cycle, you see there is a on-off operation. It means on-off operation is happening, but along with that, there is instability. But, if you further increase, again this is the switching clock, you will see if you see this cycle, the switch is totally off; that means the switch is totally like off there is no on.

It may so happen if you go further up, the switch can be completely on. So, here, it is unstable. The current loop is not stable, but along with that it has duty ratio saturation and that first one is called period one behaviour and this diagram is called a bifurcation diagram. Again, I am not discussing detail about this..

This is called a bifurcation diagram, and this is my sample current; that means, if I under steady state, if I sample the current at every rise in it like I am taking this sample and if I display in this axis for a given particular proportional gain, then I will get one point here right; one point here. That means, all inductor current will overlap like they will keep on repeating the same place because they like a straight line right..

But, if you increase, you will see this region, you have some sort of instability and that is exactly is happening. I am just showing qualitative plot, but it is not quantitative, it is not an exact point-to-point map. But, here, if you go to this region, this is a duty ratio saturation and that is called non-smooth bifurcation and it is called smooth bifurcation..

Again, this bifurcation terminology, I am just using just to you know those who are familiar can look into this; but otherwise, you can imagine that this is a kind of instability, where in this instability there is no duty ratio saturation, but here there is a duty ratio saturation.
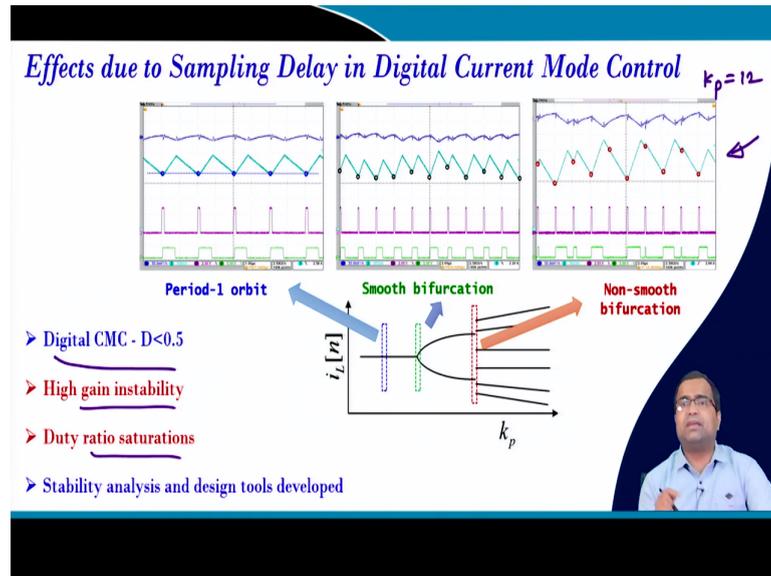
So, here, we found that this is even for duty ratio much lower than 50 percent and this high gain instability, when the increase the gain because we generally need a little higher gain because we want to go for optimal tuning like you know large signal tuning or we want to go for faster bandwidth right; high bandwidth..

So, we need some higher gain and in digital control. This may lead to such this kind of instability and that was not explored earlier. So, what we found that this kind of stability does happen and it leads to high gain in stability with duty ratio saturation and this stability analysis and design tool, we have developed.
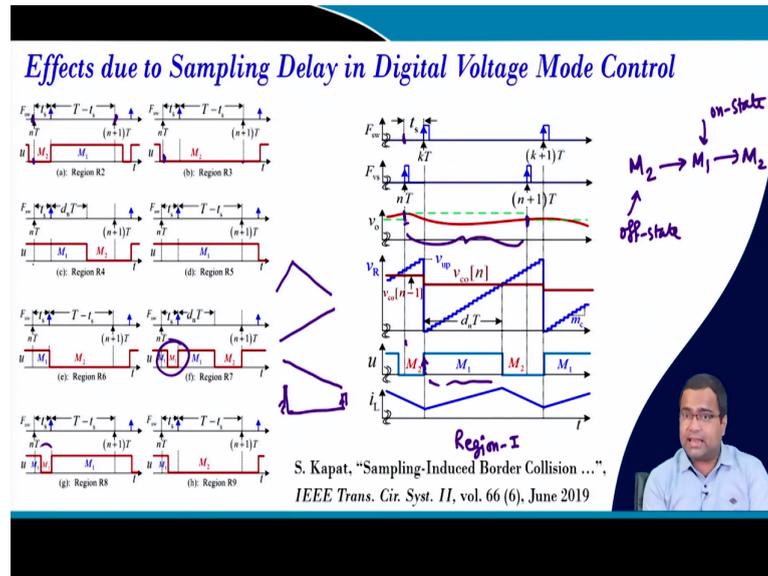
What is the cause? If we take the voltage mode control, this is our sampling point right. So, that means, if I take this point and next sampling point is here. So, if we take about a periodic operation between two subsequent sampling, what can we expect? During the first sample, the switch should remain off and during the next sample also switch should remain on, in between the switch should be on..

That means, in the sampling instant the switch should be off that is our desired requirement or requirement or the desired or expected waveform and in between switch will be on because when the switching clock will come, the switch will turn on here right switch will turn on here.

And depending upon duty ratio, it can be smaller duration or larger longer duration. But for the two subsequent sampling points here, we are expecting they should appear in the off time and in between they should be on. That means we should get something like a off, then on, then off; this is my state two off state, and this is my on state. So, off, on, off. But, actually there can be mean if you take..

So, this is I will say my desired a region 1. But, here, if you take between two sampling points, it can be off and fully on; it can be totally off, it can be on-off, it can be totally on, it can be on-off and in between. Also, there can be switching. So, there are such total 9 possibility can exist..

So, if you take about analog control between two switching edges; that means, your switch will on or off right, this is one possibility or it can be totally on or it can be totally off in case of analog because we take the sampling, it is a stroboscopic sampling; virtual sampling..

There is no sampling in analog. So, if you take between two clock edges because you are talking about these clock edges, so that in between two clock is 3 possibility can happen; but here in between three sampling edges, you can have 9 possibility and this is the reason for such kind of instability. And if you do not take this delay properly, you may end up with you know chaotic behaviour, duty ratio saturation such thing and it was reported here and subsequently, we have also reported in last epic about this in current mode control.

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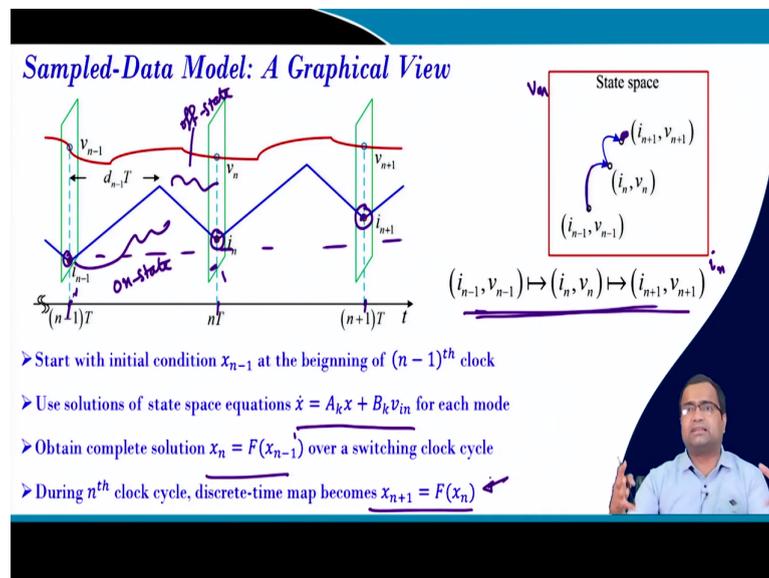
So, the reason is that how to justify if we do you know sample data model; that means, we can use this like a window, like a window at every clock edge. Here in our for analog control, we can use this window in synchronizing with the switching clock. We want to see the value when this intersect with this, sorry it intersect with this. I would say surface right very interesting and we want to map this value, the voltage and current right map and we want to see in the state space, if we take you know current versus voltage in the discrete plane like a i n and v n. So, it will move one one one. So, that means, if you perturb and if they come in the same line, then that means they are repeating in every cycle, then it will eventually become like a point..

That means there will be no more movement of this point. That means all perturbations have died out, and it converges to a point and there is a stable condition, ok. So, this in order to get this, you know the kind of mapping of this point; you need to start with some initial condition here..

Then, you obtain at the beginning, then use the solution. You will get the on state trajectory solution, then you get the off state trajectory solution and we know about this, we have discussed very briefly at the beginning at the modeling technique, there are something called discrete time model where we can get the solution of the state space equation and for individual subsystem..

And if you get the total solution x n, then you can represent this x n in terms of x n minus 1 and that will create a map and that is exactly what I am showing. But, this is a somewhat, you know I would say complex map. I know and it mathematically somewhat complex; but it is necessary to capture this kind of behaviour. But, this model can also be extended to get the perturb discrete time model and to design the digital control.

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So, the modeling technique in digital control, we can use a traditional small signal model which we have discussed throughout this course and then, we can approximate the delay due to the ADC like a delay in the loop right that people also use and then, you can design a controller. But, this will give somewhat approximate design very nicely, but this model

cannot capture the kind of instability; that means, duty ratio saturation, those things it cannot capture. So, that will be in that sense this model is not accurate.

The discrete equivalent of small signal model. It is totally in continuous domain, where the controller is designed in the continuous domain and then, it map back to the digital domain by means of a transformation; that means, either by linear transformation or backward transformation and so on or you can get the discrete equivalent of the analog and then design the digital controller directly. But, these two techniques are no longer I mean is not used so much because they cannot capture the kind of stability that happens in digital control..

So, they are simple, but still you know some data sheets still use the application node. But, discrete time model, large signal and small signal model particularly is that now it is a very like an essential tool for designing digital control which can predict this kind of stability and also, it can from there you can get the frequency response and various other stuff. So, we can derive various transfer functions for this and this large signal model is very much needed in order to capture the kind of non-linear behaviour for different type of possibilities that we have discussed between two subsequent sampling points.

So, this I am not going to discuss this because this is just touching because we know about this traditional model. We can get this equivalent discrete time model little we know; but all these require thorough you know lecture series to understand in detail. So, I am just touch upon I am just touching this topic so that you know one can go through literature or you know resources and get some information.
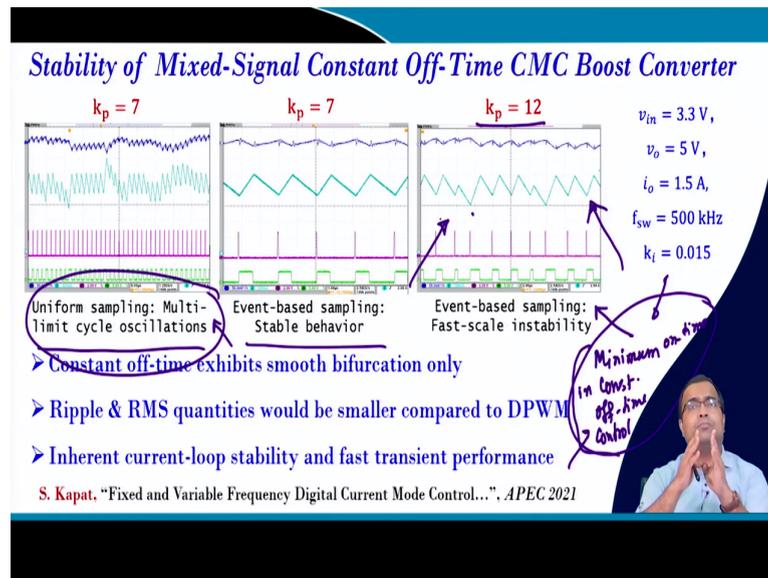
Now, stability of the mixed signal current mode control. So, we talked about stability of fixed frequency current mode control and we saw at k p equal to 7, there also it was k p equal to 7. Sorry, here you are using uniform sampling; that means, if you use a uniform sampling in variable frequency control, this is called multi limit cycle oscillation and that we should not use. So, here we are using event based sampling; that means, we are sampling at the switching event; that means, whenever the switch is about to turn on, then we are taking the sample and putting some delay so that we can capture the clean sag signal..

So, here, we are sampling with respect to an event; but here we are sampling with respect to time. So, that should be avoided. So, the event based sampling is perfectly stable, and if we go to the highest gain, where we saw severe instability with duty ratio saturation. We have discussed this, if k p is around 12, there is severe instability where duty ratio saturation happens..

But, if you go to this technique, there is no duty ratio saturation and it can be shown that. In fact, it is shown in this epic paper that it does not lose the structural stability; that means, every cycle, you will have on off operation. So, it will never happen that fully cycle is on or off because we are utilizing the minimum on time, minimum on time that we have discussed in constant off time control and because of that, your on operation is bound to come between two sample..

So, if you take the sample in one off period, then in between suppose the on time is 0, but we are forcefully adding because this is the nature of this constant off time that we have discussed and it is all commercial product, they do have. So, because of we are introducing on time, just to make sure that there will be minimum on time. So, then it will never have this structural instability..

Now, you may ask me that on time may put a constant in the step down transient. But that can be anticipated in digital control because during a large signal transient, you can disable this minimum off time operation so that the transient can be speed up; we can speed up the transient response and in the last lecture, we saw some of the result that we obtained. We can make the transient response extremely fast; in fact, we can get the optimal response simply by using constant off time control, by disabling this on time only during the large signal transient..

But, when it comes close to a steady state, then we enable this and our whole kind of instability comes in a steady state. So, we can avoid this structural instability under close to steady state. At the same time, we get the fastest performance and since in constant on time or off time control, your current loop is inherently stable. So, there is no stability problem.

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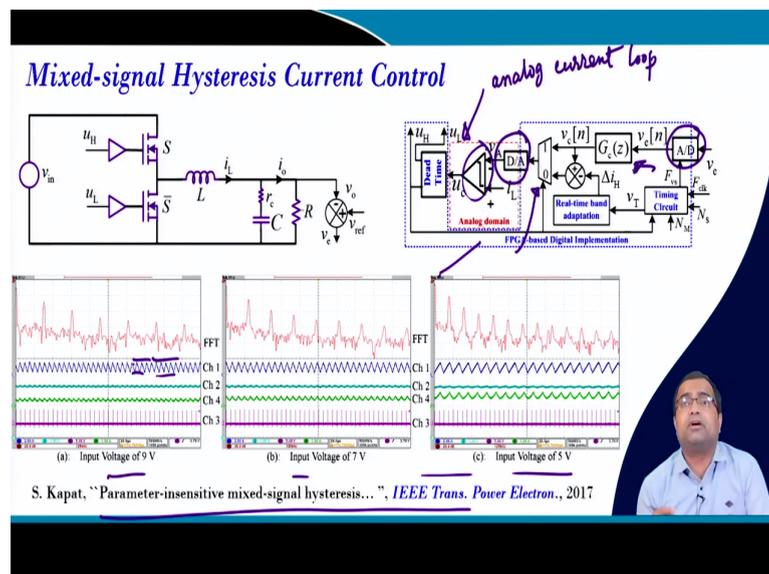
And we have applied this hysteresis mixed signal control; in fact, that was the event based sampling was first introduced here and then, with where we have shown the stability in hysteresis control all this stability criteria. And here, the mixed signal current mode control,

since we have used one sample per cycle, you can see for a wide range of input voltage variation..

The current ripple band remains same; it does not it is not affected right. But, of course, there is a switching frequency variation because if you do not change the current ripple and if you change input voltage naturally switching frequency will be high because in case of you know variable frequency operation, we saw that for a given switching period, the ripple would vary.

You saw for a given switching frequency, ripple will vary with the input voltage. Now, for a given ripple, thus if the variation input voltage happens, then the switching frequency is bound to you know to vary. So, we can adjust it because in digital and here, we have used only one D to A converter and one ADC and one analog comparator and we are using a time multiplexing here..

So, we can get this perfectly stable behaviour and we can get the benefit of fully hysteresis like a mixed signal hysteresis control because the current is in analog loop. So, it has analog current loop. So, it has analog current loop..

So, you can get very fast transient response. We can get a ripple insensitive; sorry, that means, the current ripple will be insensitive to system parameter because it will be fixed for the whole cycle that I discussed. So, you will get many features here and perfectly stable current loop right and you can tune the controller in order to get really fast transient response ok.

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So, you can get an event based sampling in variable frequency control. Then parameter insensitive ripple band that we have discussed but using only one sample per cycle. We can really get very fast transient response and we can in fact configure either in peak, valley or average. So, this can be a very effective technique for battery charging. We have seen other application, where we need to precisely control the average current. So, we can achieve very high current loop bandwidth with precise control of the average current..

But, only issue here, we need to sense the full current. There are current sensors. There will be lossless due to current sensing techniques. We know that inductor and resistance in parallel, we can put a resistance you know. So, this kind of network we can use and when, by sensing this take, we can actually get the ripple information of the inductor without putting a physical resistance and this is the DCR of the inductor right.
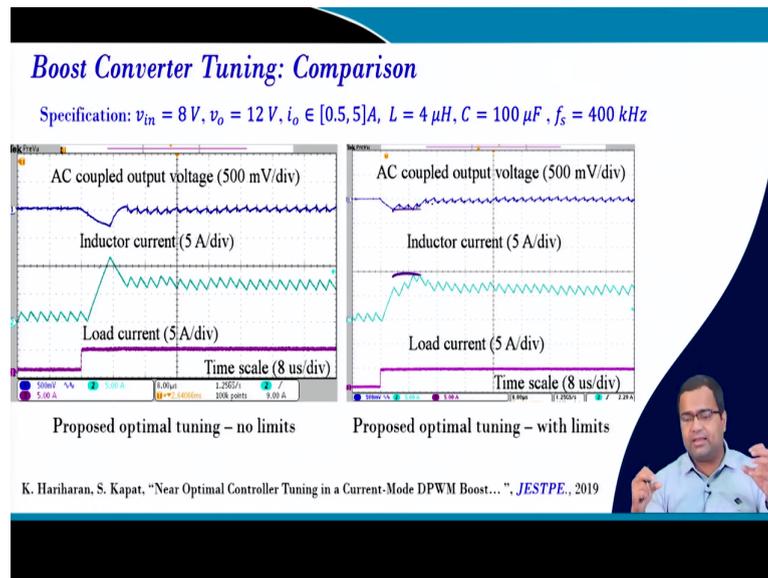
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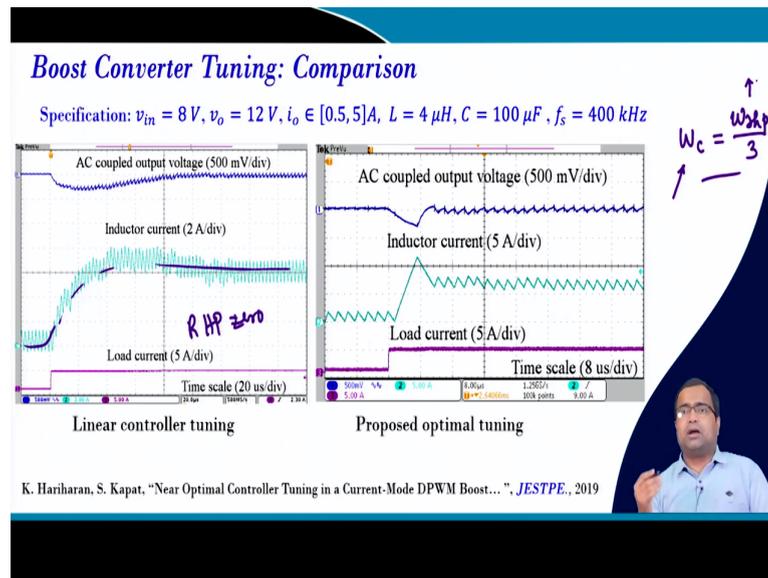
So, this can be used again the tuning method that we discussed for a boost converter. We have actually applied; that means, if we apply this because we have discussed already the previous lecture in simulation how to implement this and that can be easily implemented digital because the tuning parameters are in the digital domain in the voltage loop controller..

So, we can get extremely fast transient response almost 8 to 10 times faster than the analog current controller because that is due limited due to the R HP zero because we have we have discussed that your crossover frequency, we found for current mode control it was R HP zero by 3..

Even though you do digital control, we can adjust the crossover frequency when R HP zero varies because that can vary due to the change in load current, change in duty ratio, then we can adjust in digitally control converter; but that is not enough..

So, we need to incorporate such large signal control to achieve really fast transit. So, the digital control just do not you know we should not go only for small signal, where we can do some better; but since we are investing more because of ADC, DAC and other stuff, so we should take the best out of it.

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So, we have compared that your peak current is pretty high and if you put a current limit as well as the voltage limit here. So, then we can get you know a very good transient response.
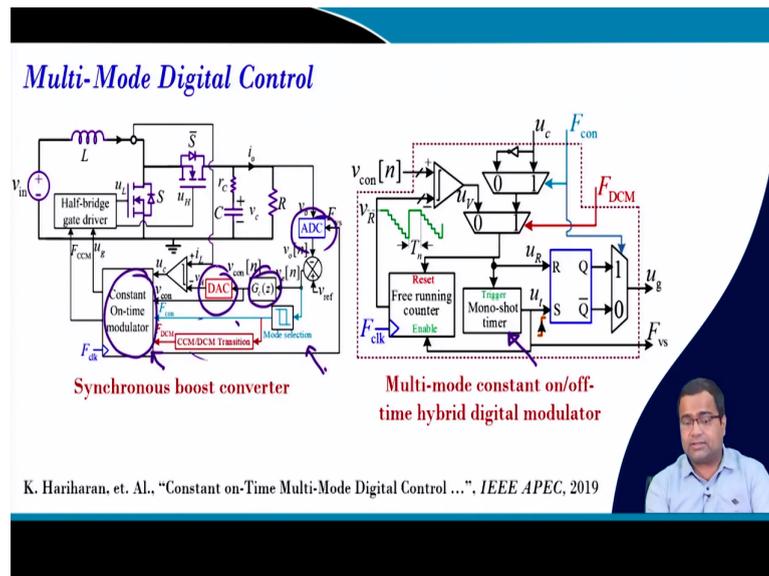
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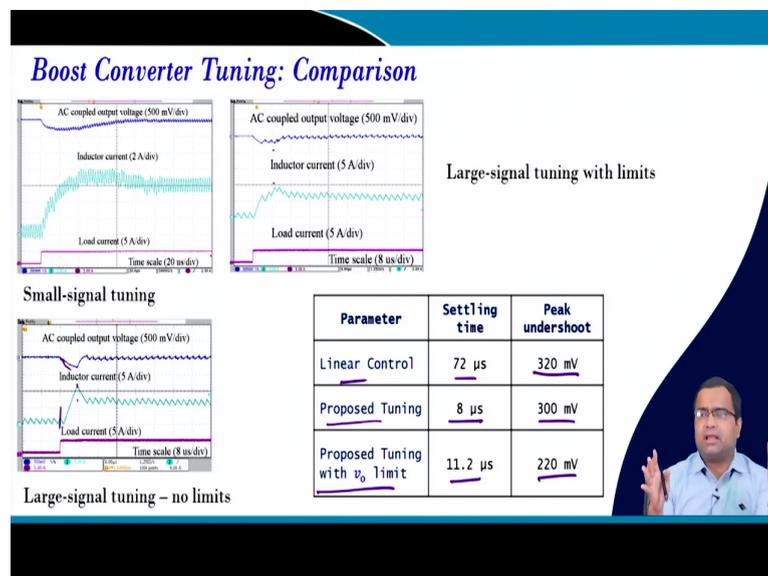
And it is much faster than that. In linear control, you need a 22 micro second recovery time with 320 millivolt voltage undershoot, whereas, our large signal tuning takes 8 microsecond with 300 millivolt. If we go for large signal tuning with the voltage and current limit, then we will get 11.2 microsecond; it is still almost 6 to 7 time faster with reduced voltage undershoot.

Because in boost converter, it has a property. In buck converter, the time optimal control also reduces the undershoot; but in boost converter, if we increase if we increase the duration of on time, the voltage undershoot decreases because during this time the voltage discharge. So, here, in time optimal control by boost converter, you may end up with more current voltage undershoot. So, for that, you have to put some limit and that can even achieve faster response.

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So, here also now since we have learned about constant on time and off time, where what we are going to do? This can be integrated; that means, we can use only one DAC, only one ADC, one controller, but some few extra digital blocks because this is a modulator. We have discussed, this modulator value can be updated because of digital. Because either we can configure to constant on time or constant off time. So, if you consider constant on time, then the value of the on time should be different from the off time. So, as a result you need to just update the timer..

So, you can see it is only one monoshot timer, where we need to put the update the value of the timer so that we can configure the same circuit to constant on time or off time. But only requirement you need to change the sampling edge because it is relies on event based sampling and we will discuss in this..
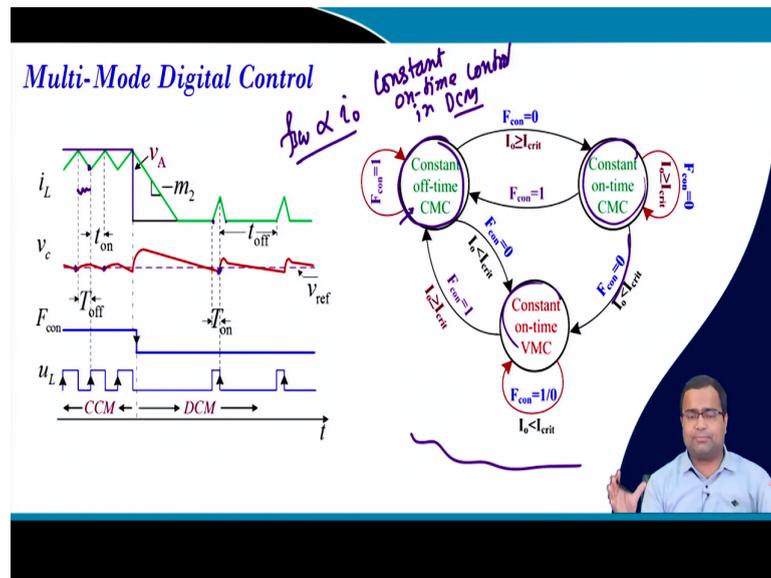
Suppose you take constant off time control. You see, the off time is constant; then, we are taking the sample at every here. We are taking the sample here; that means, the output voltage is taking sample here, when before switch turns on, we are taking the sample because it is like interval two sampling and during the constant on time control; we are taking the sample before switch turns off; that means, we are taking the sample right here, close to here..

So, that means only the changing sampling point; that means, for constant off time, we are using the sampling is to be before switch turns on and for constant on time; we are taking the sampling time before switch turns off.

So, these edges can be changed adjusted by this clock. So, there is no extra hardware requirement except for those small digital you know hardware right; but that controller everything else they are common. So, we can achieve a smooth transition; that means, at high load, we can go for constant off time, where we can take the best benefit of fast transient step up transient..

During step down, we can take the benefit of constant on time. So, we can get a very extremely fast step down transient and also, under light load, once you enter into light load, then we can constant on time, we know about that it can achieve a very high efficiency in the light load by varying the switching frequency proportionally to the load current.

Because it is constant on time control, where your switching frequency is linearly proportional to load current in under constant on time control right, in DCM and that we have learned; in DCM that you have learned. So, this can be very easily programmed using finite state machine, where if it is in continuous conduction mode, CCM, then you go for constant off time, when there is a step up transit..

During step down, we go to constant on time current mode control and if there is a DCM, we can detect the 0 current then that since the current is 0, so we cannot use a valley current control because it is already 0. So, you can use a voltage mesh algorithm and that is typically used for any. So, that means, all these blocks are already inbuilt.

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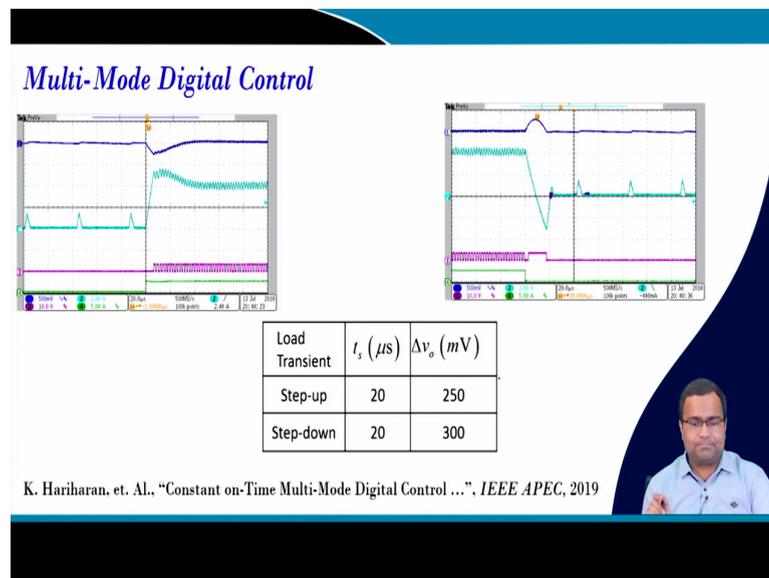
So, we can achieve very fast transient response. You can see there. There is no additional switching here because that is the inherent property of the constant off time modulator. In constant on time also, you can get very fast transient response and but initially, we are using synchronous configuration so that this can be recovered quickly and once it comes back, then we go for DCM operation and there we can enable constant on time. By that way, we can achieve very fast transient response and high light load efficiency and this has been already published.

So, the benefit of opportunity benefits and opportunity using variable frequency control, no current loop stability problems because in either in constant off time, on time control, constant off time control or hysteresis control, there is no current loop stability problem. So, it can be used for wide duty ratio operation and since we are using ripple based architecture right, so you can use very ripple based control algorithm because like hysteresis is a ripple based control..

So, you can it can be easily implemented in digital domain and we can easily synthesize or emulate the ripple inside the digital control also right. So, fast control I can be implemented..

Structural stability retained that we have discussed because, in constant on time off time control, there is no structure like instabilities. As a result, there is no duty ratio saturation unlike in fixed frequency control. Then, the large signal tuning can be implemented in digital, although this can be also implemented in fixed frequency..

Then, the programmable switching frequency because, since we are using a digital platform, we already have an all digital PLL inherent. So, using that feature, we can program the switching frequency and regulate the switching frequency and then, we can easily implement multimode control that we have discussed by changing between constant off time on time to take the best benefit as well as high light load efficiency.

So, we can improve both performance efficiency and we can adjust the switching period and we can get very enhanced stability both fast scale stability. So, that sub harmonic problem can also be reduced substantially.

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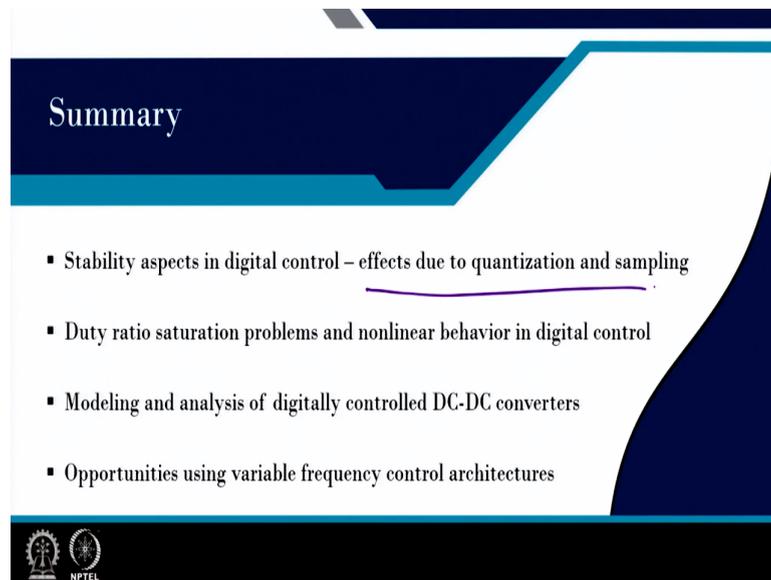
So, with this, I will summarize. The stability aspect in digital current mode controls is discussed; we have discussed the effect due to quantization and sampling. Then, we have also discussed the duty ratio saturation problem and non-linear behaviour in digital control..

Then, we have also discussed modeling and analysis of digitally controlled converter and then, we also discussed opportunity using variable frequency digital control architecture. In fact, these are just you know I am touching upon, what are the emerging you know what is going on some of the architecture; but you can browse through many other digital control architecture..

In fact, majority of the commercial product are slowly shifting; not now, but may be in near future in 5 years or 10 years down the line, you will find that the products are coming in digital. Because it offers so many features of flexibility, programmability, tuning, performance, efficiency..

So, those can be you know obtained. But, we have also we have also observed, there are stability aspects are also there and there are other aspects of you know ADC, DAC

optimization because if there are multiple converter, we may not need multiple ADC. So, we can use the resource in time multiplex mode and you can reduce the requirement.

So, this is something about you know the overview of some aspect of digital control and some variable frequency architecture and I think, you will know more about digital control in future lecture, future course. So, with this, I want to summarize here.

Thank you very much.