

**Control and Tuning Methods in Switched Mode Power Converters**  
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**Module - 03**  
**Fixed Frequency Control Methods**  
**Lecture - 16**  
**Feedback Control of Cascaded SMPCs**

Welcome back, this is lecture number 16. In this lecture, we are going to talk about Feedback Control of Cascaded Switch Mode Power Converters.

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**Concepts Covered**

- Cascaded converter – intermediate bus architecture
- Concept of constant power load
- Example of unstable open-loop system
- Feedback control for active damping

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In this lecture I am going to talk about cascaded converter in the cascaded DC-DC converter, series connected cascaded DC-DC converter which is sometime known as intermediate bus architecture.

In this context, I also want to introduce the notion of constant power load, then also I want to give an example of unstable open loop system; that means, a converter open loops converter can become unstable while driving a constant power load. And then I want to tell feedback control for active damping in order to stabilize the unstable open loop plan.

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*Cascaded Converters and Applications*

*Tele.com*

Examples

- LED driving
  - $v_{in} = 12\text{ V}$
  - $v_{bus} \in [30, 48]\text{ V}$  (with a handwritten  $60\text{ V}$  in red)
  - $v_o = 12\text{ V}$

Head lamp load
- Data center
  - $v_{in} = 48\text{ V}$
  - $v_{bus} \in [6, 18]\text{ V}$
  - $v_o = 1\text{ V}$

Processor load

So, a cascaded DC-DC converter comprises multiple DC-DC converters that are connected in series. You can see the input voltage, this is the input voltage, the input voltage which is connected to a DC voltage. Then the first stage converter output is the bus voltage, it is called the bus voltage  $V_{bus}$  and the second stage converter output is the actual output voltage, which is connected to the load.

So, that is why the first stage converter I will come to where this is called intermediate bus architecture where the last stage DC-DC converter is known as point of load converter ok.

I want to give an example, if you take an LED driving, like automotive LED driving it has a 12-volt battery and then you need to drive multiple LED load. Because most of the recent cars are coming up with led lighting system which include like a headlight, taillight, fog light there are various other lights and they have certain different voltage ranges, like for head light can be between 12 to 14 volt and then you know there are other lights.

But the battery is 12 volt. So, if you want to convert from 12 volt to 14 volt or 12 volt, they are almost close to each other and the battery voltage can also vary. So, in such, while we can use a simply buck-boost converter, but it requires certain stringent performance requirement. Another thing we also need to ensure that led is like a constant current load.

So, we need to maintain the current of the LED string. So, we it is expected that output should have a constant you know inductor; that means, if a DC-DC buck converter can be an output where it has the inductor at the output side.

So, 12 volt where the bus voltage can be even higher instead of 30 to 48 volt, it can be even 60 volt or higher the intermediate bus and the output of the led can be roughly around 12 volt, it can be 14 volt. So; that means, you need first stage converter to boost up the voltage from 12 to 30 or 48, even 60 volt and the second stage DC-DC converter has to convert that voltage into 12 volt ok. So, it is a step down converter and this kind of architectures is used for head light application head for automotive LED.

Another application is the data center. In fact, this is also true for most of the telecom sectors. They have a 48-volt power supply. There are multiple loads like you know you have a processor load, then you have a communication device. Their voltages can be few volt like in 3.3 volt 5 volt or even roughly around 1 volt for the processing application.

So, 12 48 volt to such low voltage in single stage sometime it is difficult to use a single DC-DC converter. As per the recent in data center application, the 48 volt has now become a standard. We need to achieve the output voltage roughly around 1 volt because it has to supply to a processor, where the processor can be server processor, processor can be you know desktop computer, laptop computer or the server computing station. Here, the current is high, and the voltage is around 1 volt at the output terminal.

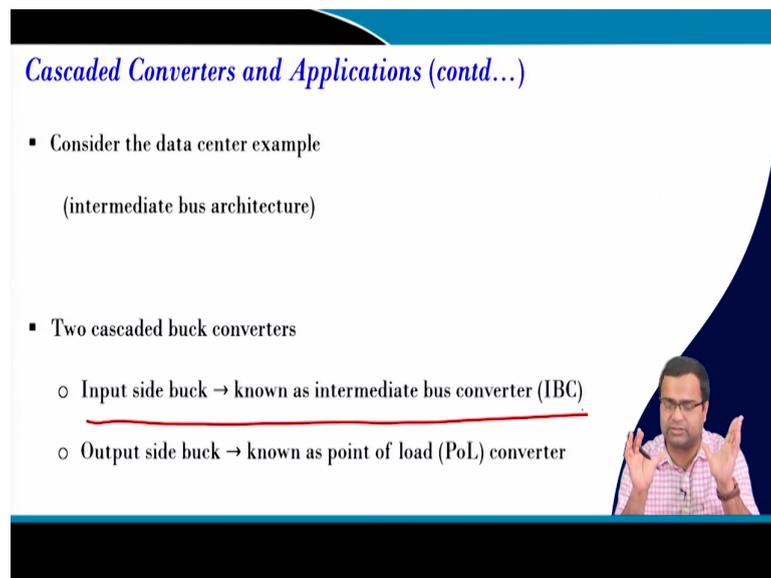
That means, the output load can be a processing load which voltage, of which voltage can be around 1 volt, but the current can be you know hundreds of ampere.

So, in such application when we want to convert 40 to 1 volt and that to a driving to a high current, then though there are you know, recently research is coming up with a single stage converter. You know this uses isolated converter for transformer base high step down converters and a hybrid switch capacitor converter which we discussed at the beginning. And the hybrid switch cap switch cap architecture can be used at the input side to step down the voltage and then it can be just simple multi-phase DC-DC buck converter.

But all this architecture you know, but two stage you know architecture still considered being an effective choice because we can optimize the intermediate bus voltage and by that way we can improve both performance and efficiency of this two stage architecture.

So, this is the processor load. In a telecom application, 48 volt is a common standard. The PoL (point of load) converter's output voltage can be roughly around 3.35 volt or less around 1 volt or so.

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*Cascaded Converters and Applications (contd...)*

- Consider the data center example  
(intermediate bus architecture)
  
- Two cascaded buck converters
  - Input side buck → known as intermediate bus converter (IBC)
  - Output side buck → known as point of load (PoL) converter

For such applications, two-stage architectures are preferred. So, I am here considering the specification which is like an intermediate bus architecture in which I am taking two cascaded DC-DC buck converter, the first stage is converting 48 volt to roughly 12 volt and the second stage I am converting 12 volt to 1 volt ok.

And in this architecture input side buck converter is known as intermediate bus converter IBC and the output side buck converter is known as point of load converter because it is directly supplying to the load that is why it is called Point of Load or PoL converter.

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*Cascaded Converters and Applications (contd...)*

Use earlier simulation models of a conventional buck converter and a synchronous buck converter

- Configure the above files to show a cascaded converter

Now, this is the very simple example of an intermediate bus architecture. So, this is called IBA, Intermediate Bus Architecture. In this architecture, the first stage you know this first stage converter. This is a buck converter number 1 and there is another converter buck converter which include this stage, this is another buck converter; buck converter 2.

And this converter as I told it is called IBC Intermediate Bus Converter, and this converter is known as point of load converter ok. So, the second stage converter is known as point of load converter which is designed to drive low voltage high current application.

And in this case, the load for the PoL converter is a resistive load, but it can be constant current load many other type of load. So, typically it is either resistive load or constant current load. For the source side converter, which is called IBC, the load is a DC-DC converter itself; that means, another converter.

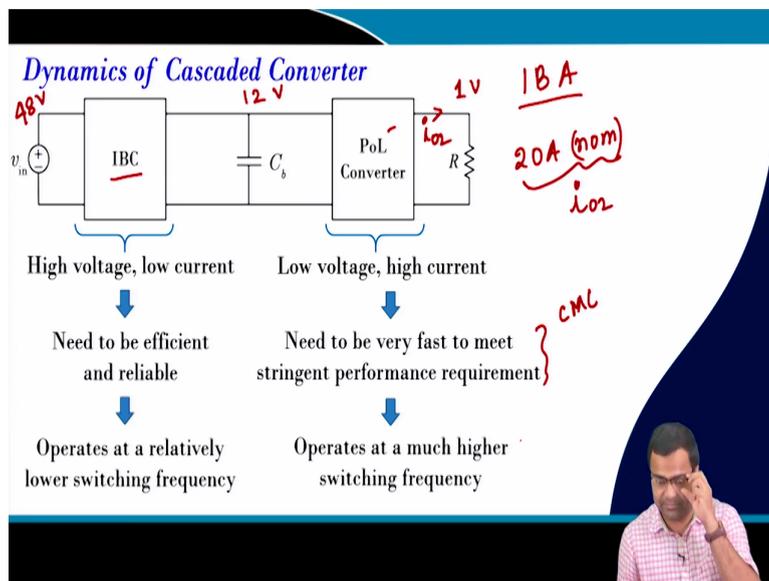
So, the IBC is driving another buck converter. This means, it is neither a resistive load nor a constant current load, but what type of load it is, it can be approximated that we will see. So, we want to first you know I want to show a MATLAB simulation case study.

So, we want to consider our simulation model of conventional and synchronous buck converter. Because in our earlier lectures we have I have showed how to develop you know building block, like how to develop from the scratch a model of a buck and like a buck

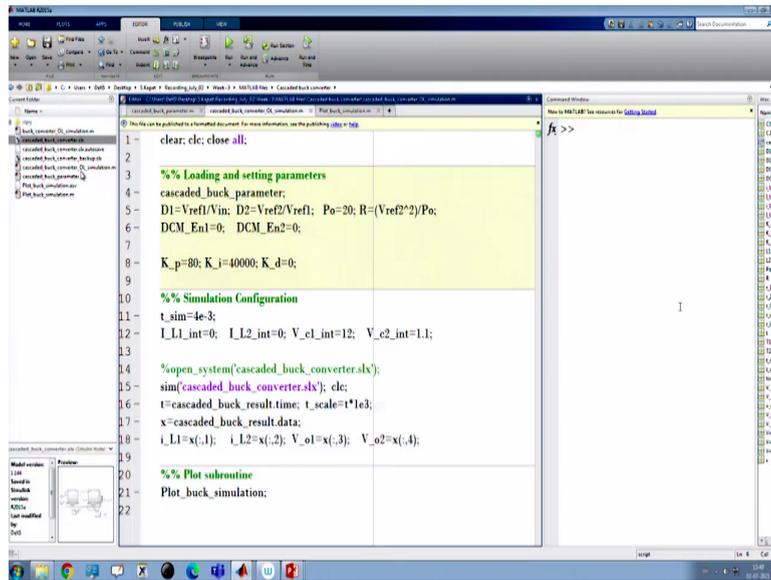
converter. We have also demonstrated boost converter example and I have also demonstrated that a converter buck or boost any converter can be configured either in conventional configuration where it includes a diode or it can be configured as a synchronous configuration where both are switches, synchronous switches.

Now, I want to show that configure the above like I will take one buck converter model in the Simulink MATLAB model and I want to cascade them in order to develop this I intermediate bus architecture. So, how to do that ok?

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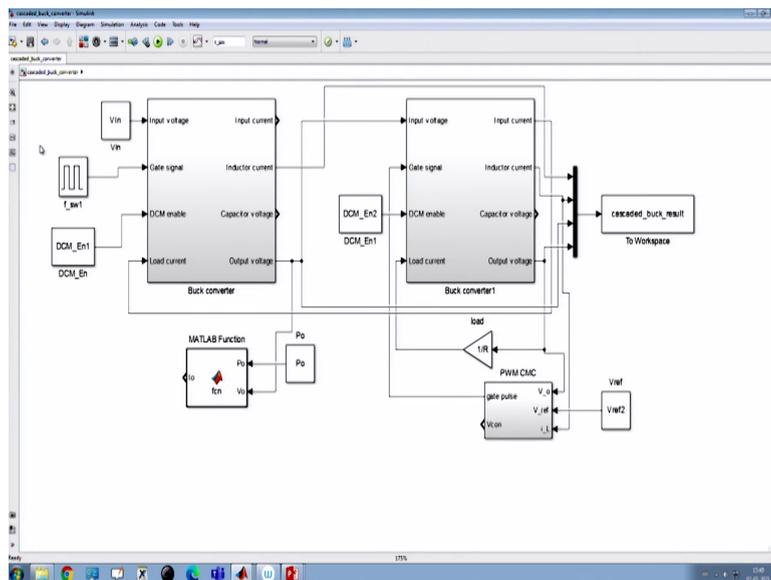


```

1 clear; clc; close all;
2
3 %% Loading and setting parameters
4 cascaded_buck_parameter;
5 D1=Vref1/Vin; D2=Vref2/Vref1; Po=20; R=(Vref2^2)/Po;
6 DCM_En1=0; DCM_En2=0;
7
8 K_p=80; K_i=40000; K_d=0;
9
10 %% Simulation Configuration
11 t_sim=4e-3;
12 I_L1_int=0; I_L2_int=0; V_c1_int=12; V_c2_int=1.1;
13
14 %open_system('cascaded_buck_converter.slx');
15 sim('cascaded_buck_converter.slx'); clc;
16 t=cascaded_buck_result.time; t_scale=t*1e3;
17 x=cascaded_buck_result.data;
18 I_L1=x(:,1); I_L2=x(:,2); V_o1=x(:,3); V_o2=x(:,4);
19
20 %% Plot subroutine
21 Plot_buck_simulation;
22

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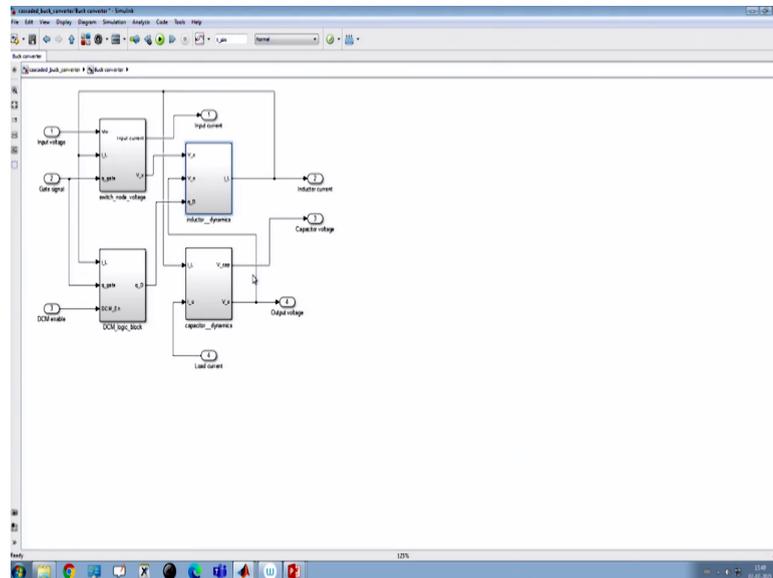


So, in this MATLAB example, I want to show you this is the example ok. So, if I remove everything like you know I remove all these inter connection for example, let us remove everything. So, initially forget about this configuration ok. So, this thing will come slowly. Now, if we remove everything we have earlier explained; what is this?

So, this is one buck converter. We have already developed a model for it and I have just taken that model and I have pasted here; that means, you can simply take this model, particularly

this model, you can copy it and paste it here. So, this model is nothing, but the copy paste version of this ok, that is it.

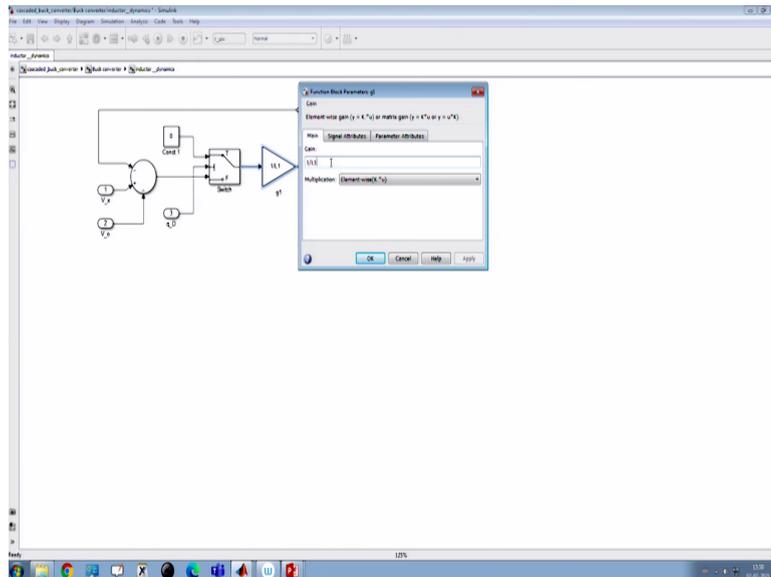
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But if we go inside what you need to change here because each converter we may not use the same inductor capacitor because each converters their voltage and current ratings are different and we have also discussed how to design power stage for a given input voltage output voltage load current specifications. So, that is why we should not assume both the converters to have same inductor capacitor value.

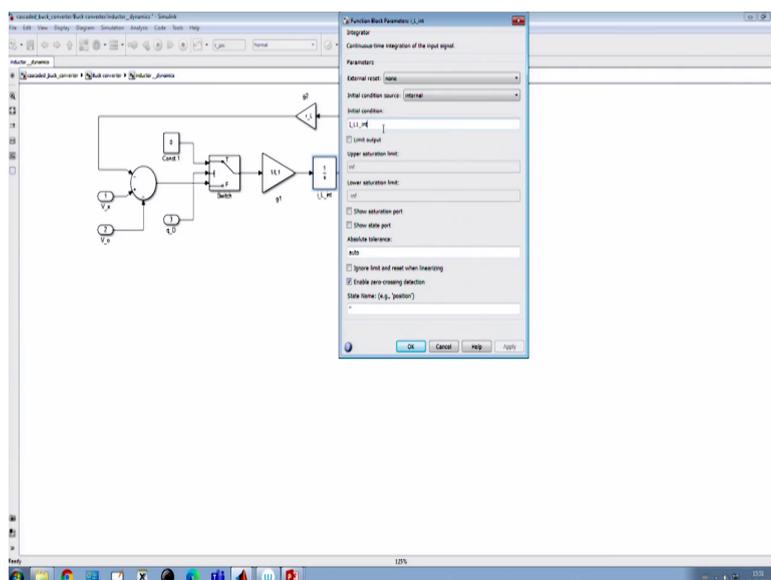
So, if they are different, then the model structurally remains same, but only we need to update the values of the inductor and capacitor and so on. So, if you go inside what it has four sub systems that we have developed, one is the inductor current dynamics, capacitor current dynamics, then a DCM logic block we have developed, then a switch node voltage block subsystem.

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If you go inductor current dynamics, only thing you have to change this L value 1 by L 1, that is the 1 by inductance value and that we have already discussed earlier. So, here we have taken instead of 1 by L I have taken 1 by L 1. That means it is the inductor value of the first stage converter L 1 for second stage I will put it like L 2 that is it.

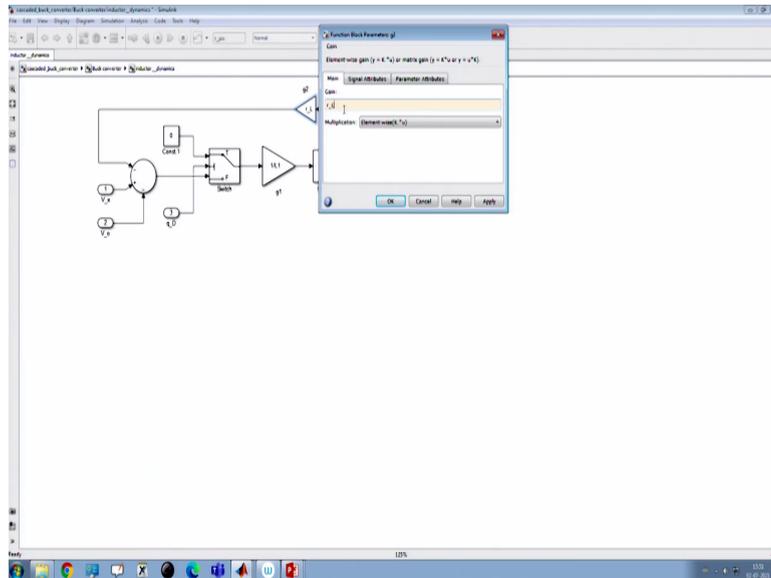
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The other thing if you go back to the initial condition. So, I want to make separate initial condition for the first stage inductor and the second stage inductor; that means, I can put

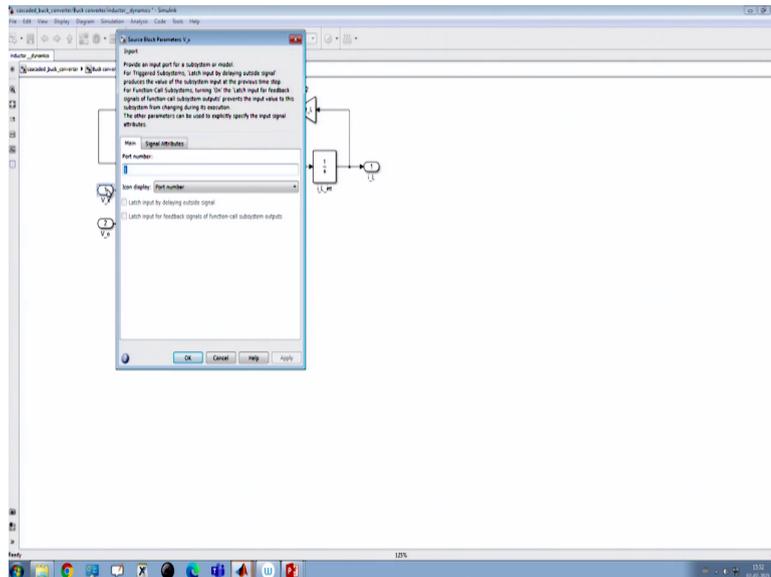
everything start from 0, but here I want to you know customize the initial condition. So, you say earlier it was I underscore L underscore initial condition. Now I just put a like a number 1 because this is for the first stage converter.

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Now, for the sake of simplicity, I have considered the parasitic DCR of the inductor same, but you can also choose a different inductor value L 1. So, this I just wanted to make it simple. So, you need to simply update this parameter value.

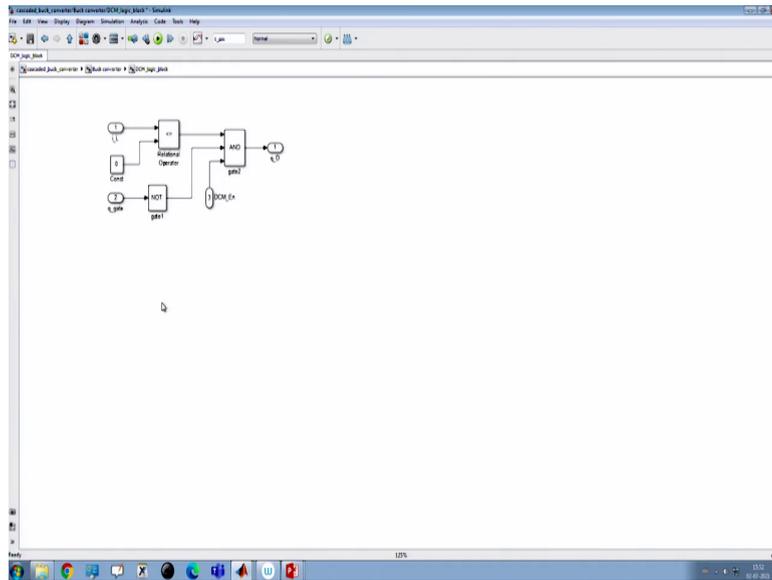
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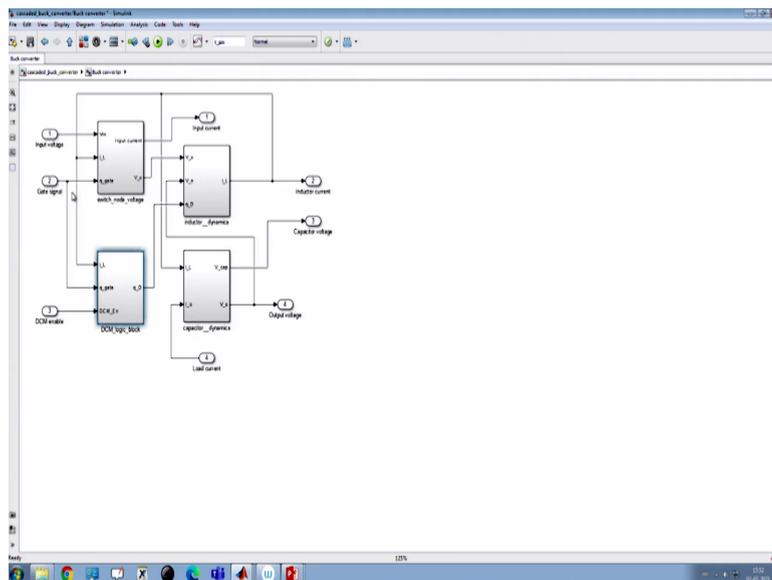
Then, so all these things are same there is no change here; that means, these things are all change put. Next, if you go to capacitor dynamics; what are we going to change? We need to change the value of the capacitor earlier. It was  $1/C$ , now it is  $1/C$  ok. Similarly, ESR of the capacitor here I kept it common, but I can change it there is no problem.

And I should also should be able to customize the initial condition of the capacitor voltage which is  $V_c$ , it was earlier  $V_c$  initialization I just put a number 1. Just to distinguish between 2 capacitor initial voltages for the first stage and the second stage.

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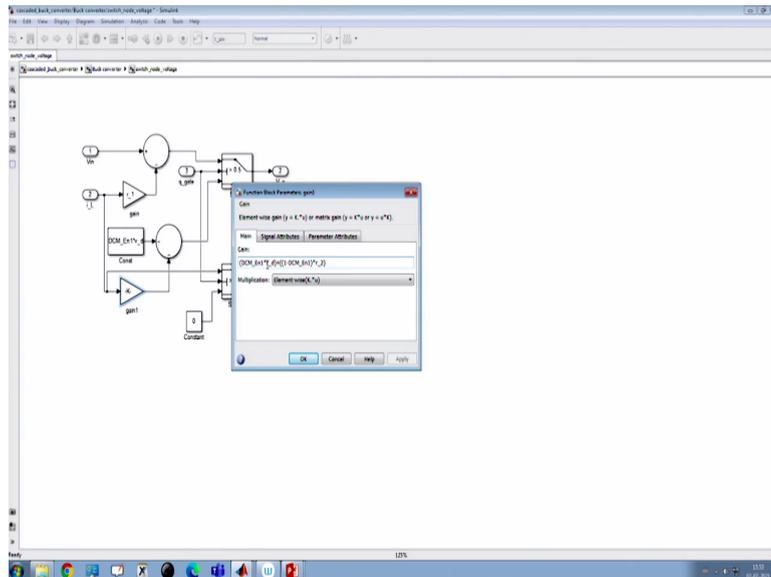


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Then what else in the DCM enable logic everything is same there is no change ok, because these are all symbol internal structure remains same, but this enable signal which is coming from outside that I want to make it different.

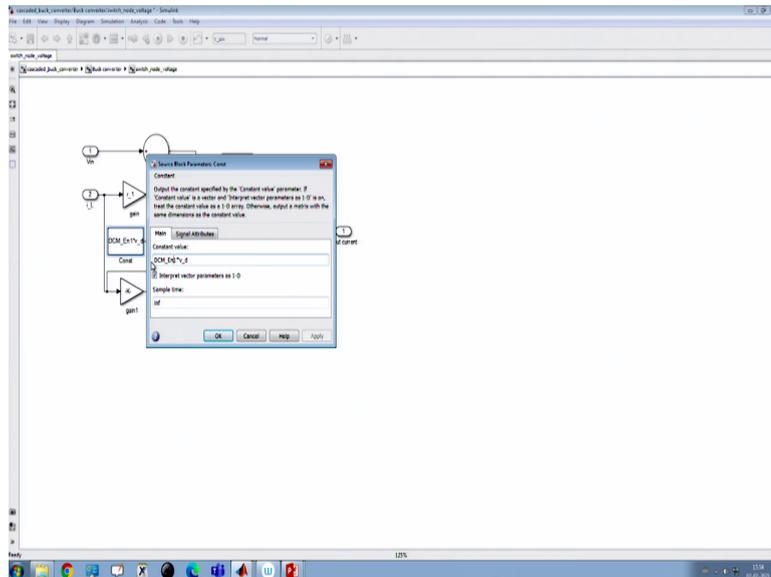
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The switch load voltage we have to be careful here, what is different here? Here, only difference is this expression that we have developed earlier. That means we have made a common expression here, which is when it is in DCM enable. That means, when it is in conventional configuration, we want to include the resistance of the diode  $r_d$  when it is in synchronous configuration. I want to include the resistance of the low side MOSFET; that means,  $r_2$ . So, that is  $R_{DS}$  on of the low side MOSFET.

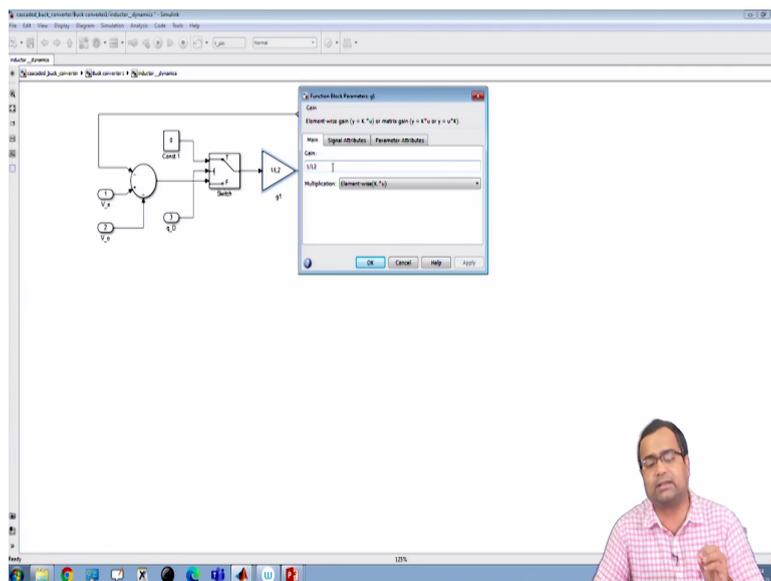
So; that means, what is the what we need to change here? I want to only change DCM to enable number 1; that means, this is the one particular block I want to customize at my dot m file where DCM underscore En enable, I want to number it number 1 and number 2. So, here it is number 1. So, I am just updating the value.

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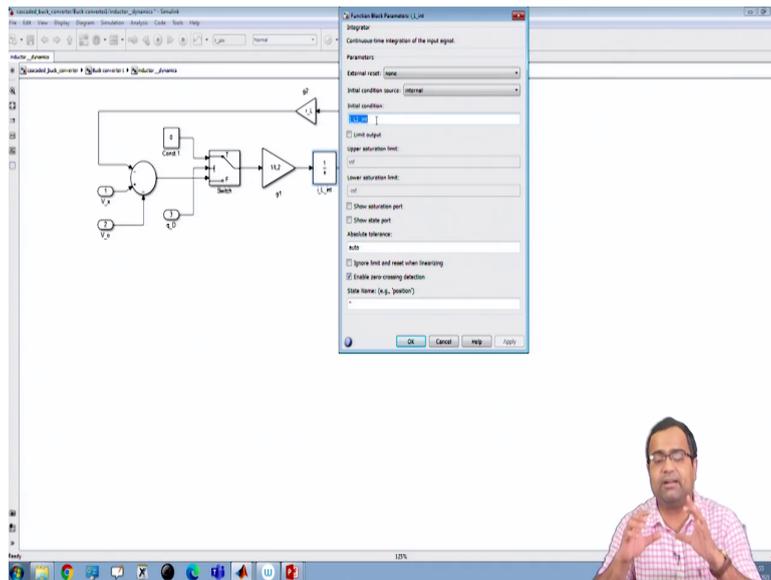
Similarly, here we can include diode drop if it is a conventional configuration, then we will include diode drop, and that is enable 1 because it is linked with the first converter diode drop and you can also make a separate diode drop for the first stage. That is it for the first stage and you can make the similar changes in the second stage. If you go inside you will see it is DCM enable 2 and you can make diode drop 2 as well.

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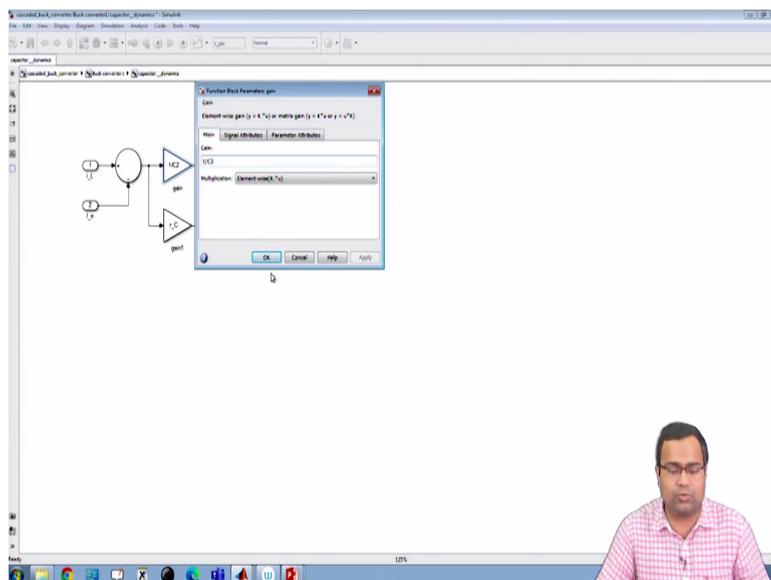


Similarly, if you go to inductor block, I want to consider 1 by L 2, because these inductors the PoL converter inductance value should be different from the IBC converter because we want to make it different. Though, we can put same value from the code, but we should make it generic so, that we should flexibly design the inductor of the two different stages.

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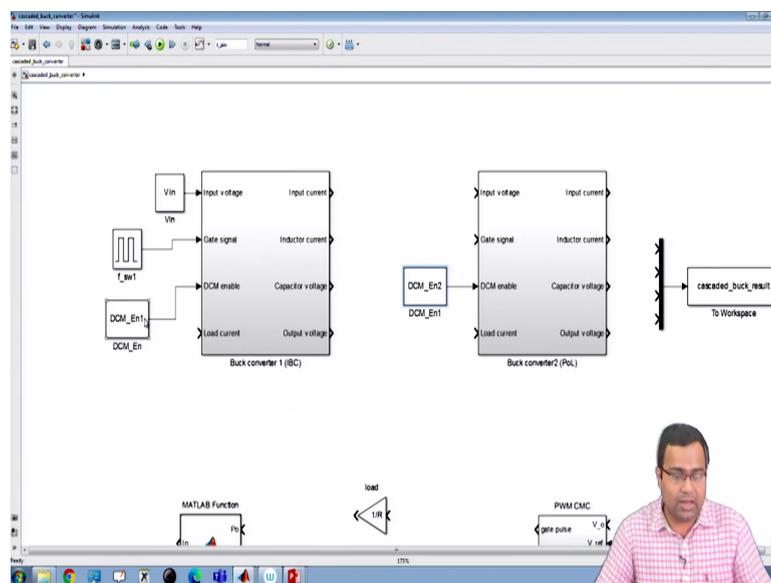
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Similarly, I have kept the different initial condition for the inductance, inductor current initial condition for the stage 2. The same thing is also applicable for the capacitor I C2 and the same thing also true for the initial condition of the PoL capacitor ok.

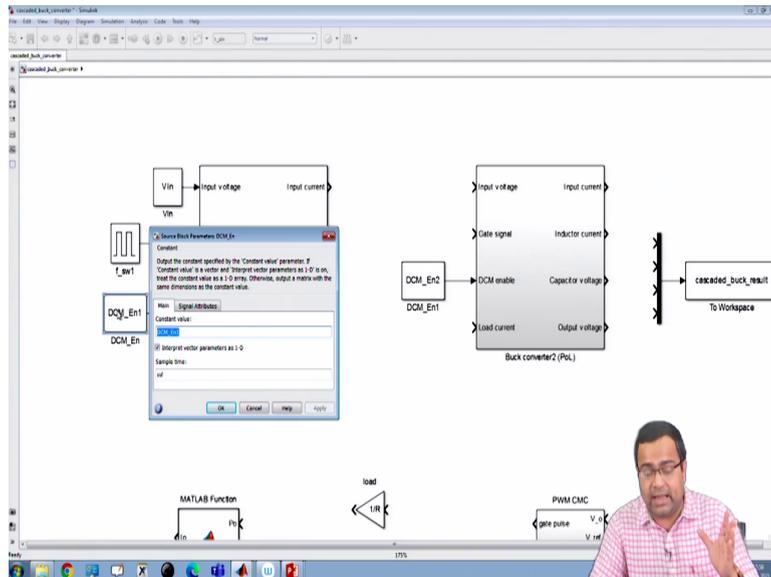
So, I can, I kept the ESR to be same, but I can make it different ok. Now for the external parameter what I am doing? I am keeping a separate DCM enable signal. Because I want to run this PoL converter which is in the output side to be ok, let us write this is buck converter 2 and this is buck converter 1; that means, 1.

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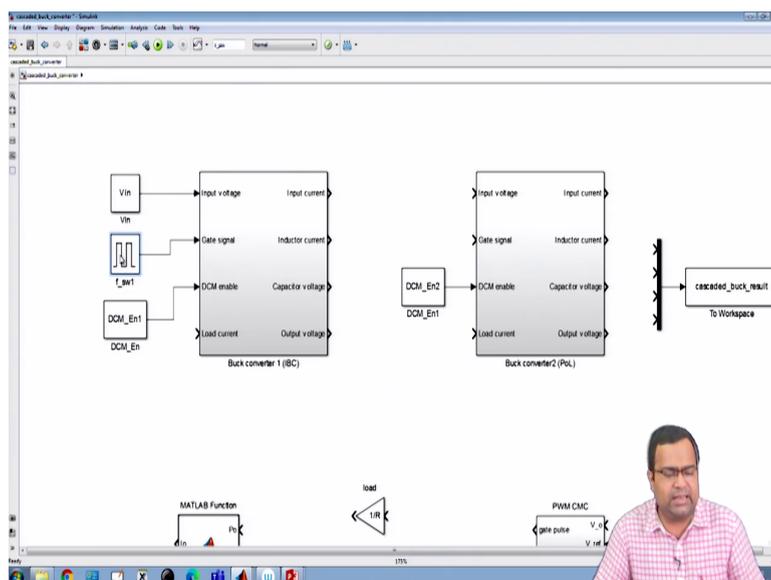
So, I call it as a IBC and I call it as a PoL, this is I call it as a PoL ok. So, for the PoL converter, I generally want to operate in synchronous configuration. So, I can separately set this DCM enable signal and I will set it to 0 so that it can run in a synchronous configuration in most of the cases except for the light load condition.

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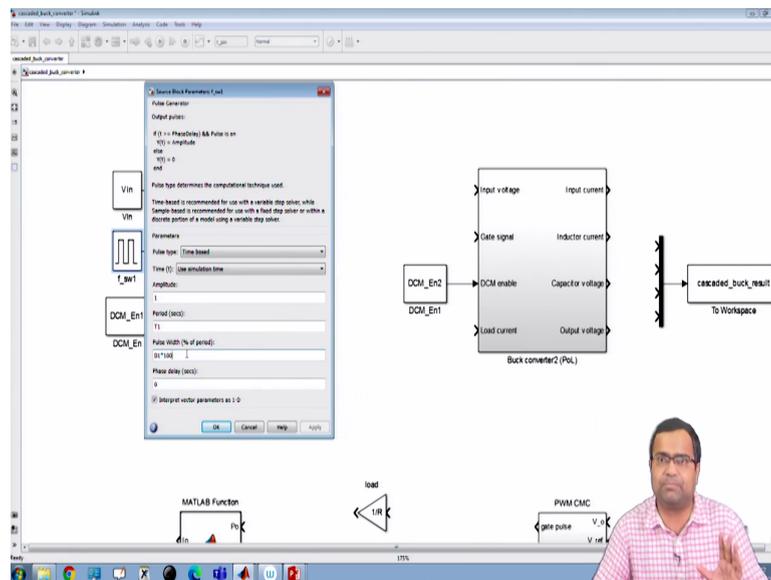


But for the first stage I probably may operate it in conventional configuration when I can keep DCM enable 1 to be 1 so, that it goes into regular buck converter with the diode and if we keep it 0 it can be synchronous configuration also ok. So, these two are different. Now, for the first stage, input voltage is our 48 volt. So, this is the V in which I will define from the very beginning stage.

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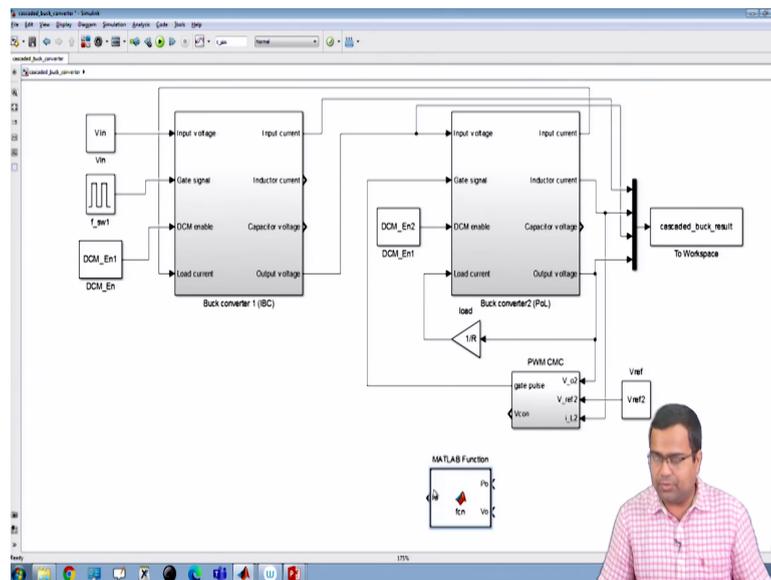
So, this is the input to the first stage. For the first stage, initially I am keeping an open loop configuration. That means I am applying a fixed duty ratio pulse; pulse width modulation signal in which the duty ratio I kept  $D_1$  to be,  $D_1$  is the duty ratio that into 100 is my percentage and the time period is  $T_1$ .

But for the second stage I want to operate in a closed loop ok. So, I think this part is clear, but now I want to connect; how do I connect? You know if we go back to the circuit ok. So, for the first stage if you look at this first stage.

So, this is the output current of the first stage; that means, this is the  $i_{o1}$ , and this is the  $i_{p2}$  that is the input current of the second stage and this is my  $i_{o2}$  that is the load current of the second stage ok, and this is the. Now for the first stage my input voltage is 48 volt, for the second first stage my output is  $i_{o1}$  which is nothing but the input current of the second stage ok.

And for the second stage, the output current is nothing, but it is the resistive load. So, it is nothing, but the  $v_{o2}$  by  $r_2 R$  it is the resistive load I can use the constant current load also ok. Now, let us go back to the MATLAB.

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So, for the first stage, input voltage is  $V_{in}$ . What is the load current in the first stage? I told you the load current for the first stage is nothing but the input current for the second stage.

So, I simply connect to this. So, it is a drag-and-drop block, then output voltage of the first stage is input voltage of the second stage. I just connect it. So, these are optional; that means, inductor current, capacitor voltage we may not connect, it need not to be connected like it is not mandatory.

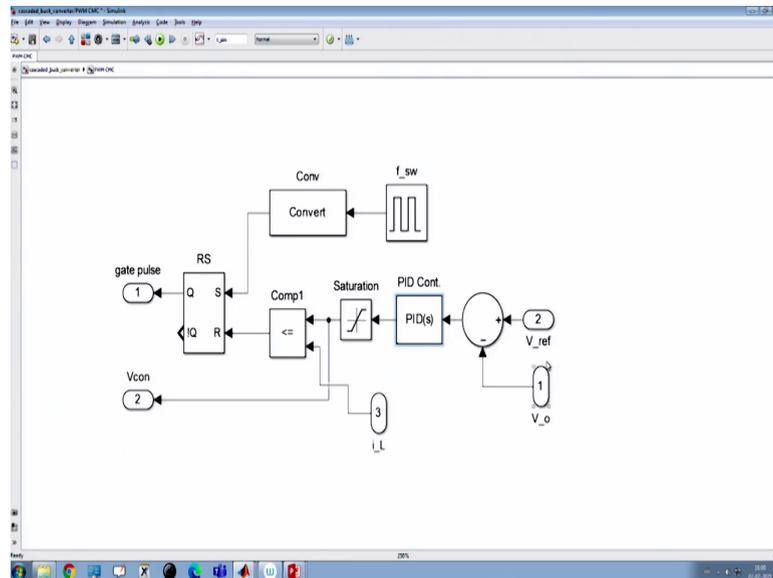
But I want to I should connect the load current for the second stage and if I use the resistive load, I can simply connect this resistive load here ok. So, resistive load I can simply connect and that we have explained in many simulation case studies in the past ok so; that means, I have connected it.

Now, what I need to give? I need to provide a gate signal for the second stage ok and what I want to observe? I want to observe the inductor current of my first stage. So, let us connect it, I want to observe the inductor current of the second stage that is my channel 2, I want to observe the output voltage of the first stage that is my channel 3, and I want to observe the output voltage of the second converter that is my channel 4 and same as earlier. What is this?

So, this is nothing, but the result that is actually getting stored into the workspace ok, that is getting stored in the workspace. Now, my connection is over. Now what I am going to do?

So, yes now I want to operate the first stage in open loop and that is already connected, but I want to operate the second stage in the closed loop.

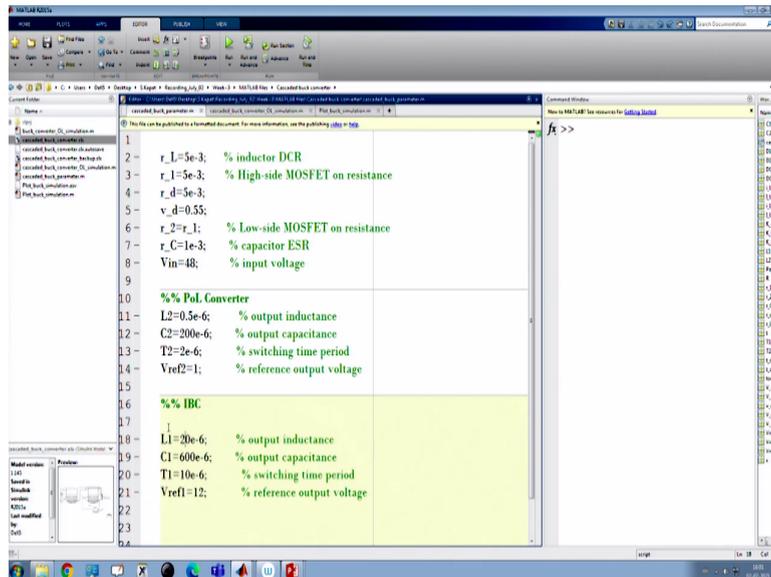
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And this is the current mode control, which I have already demonstrated in my earlier presentation. So, this is my  $V_{ref2}$  the reference voltage 2 for the second stage this is my  $V_0$  2. So, I can simply change it  $V_0$  2 and this is my  $i_L$  2 the inductor feedback for the second stage and let us connect this. So, this is the output voltage feedback, and this is the inductor current feedback ok.

So, everything is now set and the gate pulse will go to the second stage. So, now, we are operating the second stage to be a current mode control ok. Second stage is current mode control. Now so, let us do not consider this block at this time being. Now, so, first stage in open loop and the second stage in closed loop. And what are the parameter that we have set? Let us go back to the MATLAB file.

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So, we have considered a parameter file where, for the first one, first stage IBC, I choose an inductor to be 20 Microhenry because it is operated, it is operated at a lower switching frequency. So, I will come to the specification part. So, this is the interconnection part, and it is over. Now go back to the presentation.

So, we have configured a cascaded DC-DC converter, which is I B intermediate bus architecture, using our previous model. Next dynamics of the IBC converter we want to check. So, as I said the intermediate bus architecture, intermediate bus architecture it consist of 2 converter, one is intermediate bus converter another is the PoL converter.

Now, the high the IBC the input voltage is high because we are talking about roughly around 48 volt and here we are talking about 12 volt and here we are talking about 1 volt ok that is our nominal voltage.

So, for IBC compared to PoL it is designed for high voltage low current whereas, the PoL converter is designed for low voltage high current and this PoL has to cater the requirement for a processor and the current can be you know some hundreds of ampere, but since we are only using one phase. So, we will go up to 20 ampere is my nominal current for this current.

So, this is my  $i_o$  2 this is my nominal current. So, this is my  $i_o$  2 is my nominal value. So, it is low voltage high current application and the requirement of transient requirement is

extremely fast in the second stage ok whereas, the first stage is used to convert from high voltage to an intermediate voltage.

So, the purpose of the first stage needs to be very efficient. At the same time it should be reliable because it should also try to provide some clean output voltage at the intermediate bus ok. The second stage which is the PoL converter it has to be very fast because even I am just showing one phase where only 20 A is the nominal current, but typically this kind of architecture the output has to handle around more than 60 ampere or it can be several hundreds of ampere.

That is why that is why this stage has to be very fast to meet the stringent performance requirement and it is often operated under current mode control ok. So, it is often operated under current mode control because it require a very fast transient response at the same time you know when we go for multiple phases; we need to do current balancing among the phases and the current mode architecture is very popular for the balancing of current between multiple phases ok.

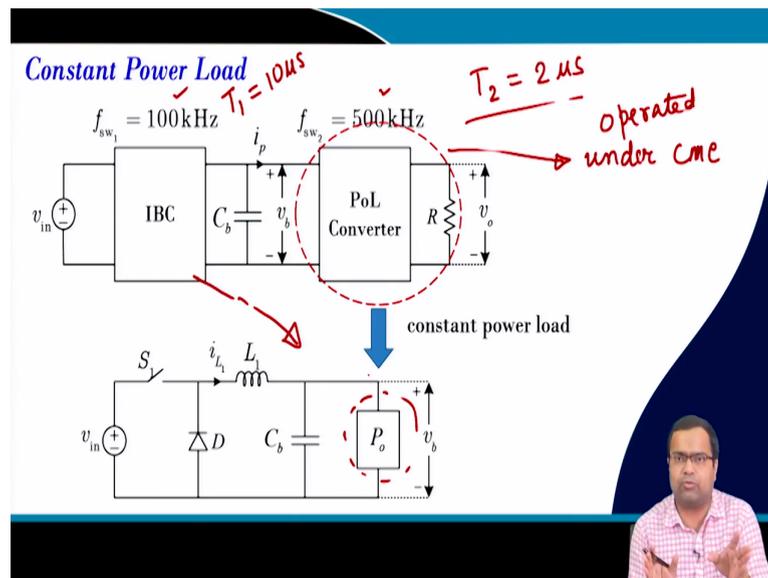
In the first stage, which is operated at higher voltage and we have discussed the losses and what we have learned from the previous lectures that if the input voltage is high, then the switching loss can be significant if the switching frequency is high.

So, that is why for high voltage DC-DC converter, we should not go for very high switching frequency because the switching loss can be very high because switching loss is proportional to the input voltage ok and of course, it is proportional to switching frequency.

So, in order to reduce the switching losses, the input side converter which is known as IBC, is operated at a relatively lower switching frequency whereas, the output side converter is operated at much lower voltage. So, you should operate at a much higher switching frequency because then we can reduce the value of the inductor, capacitor parasitic because this PoL converters are sitting very close to the actual processor where the space is also constrained.

So, we need to make sure that these converters are very high power density; that means, very smaller footprint and that is why we need to operate at a very higher switching frequency, ok.

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Now, next part I want to create a simulation case study, whereas I discussed that IBC is operated at a much lower switching frequency because it is connected to the higher input voltage. Whereas, PoL is operated at a higher switching frequency, which is in this case, IBC is operated at 100 kilohertz and PoL is operated at 500 kilohertz. So, our  $T_1$  is nothing, but 10 microseconds and our  $T_2$  we are taking here is the 2 microsecond.

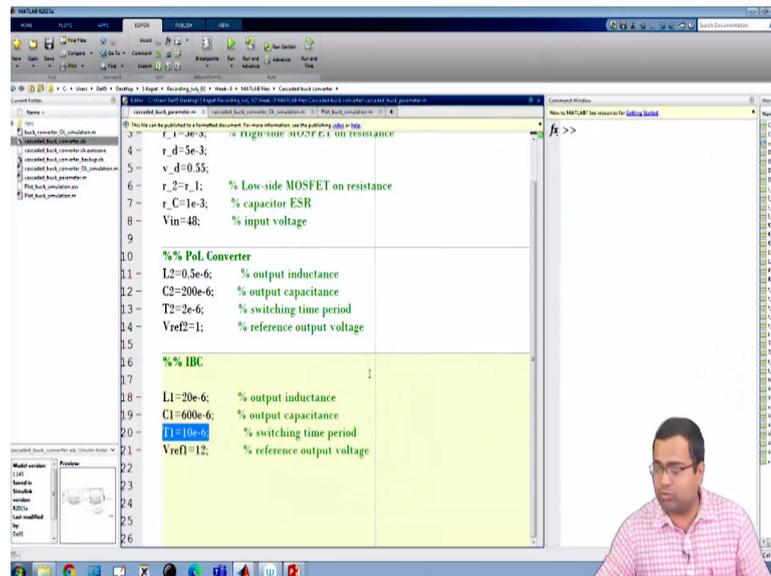
In fact, this specification is I have used which we have considered so far for a normal like a standard buck converter where we consider 12 volt input and 1-volt output. Now, I want to show this PoL converter is operated under. So, this is operated under current mode control that I have discussed. This is operated, and it is operated at a very higher switching frequency.

So, for IBC this converter is resembles at a constant power load and we want to see whether it really resembles as a constant power load or not ok. So, before coming to that; that means, before you go to the simulation, it is well reported in the literature that sometime these two-stage architecture can be simplified as by keeping this IBC here, this PoL can be replaced by a constant power load.

Because this PoL is operated at a higher switching frequency with using a current mode control. So, it is very tightly regulated, and that is why IBC we will see its like a constant

power load, where if IBC is driving a constant power load, then there can be negative incremental impedance effect and that may lead to stability problem while driving a constant power load. But we need to first verify whether a two stage full scale switching converters can resemble a switching converter driving or a buck converter driving a constant power load or not.

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Let us go to the simulation. So, as I discussed that for the first stage converter the time period is 10 microsecond and the reference voltage for its output is set to 12 volt because we want to achieve 12 volt as an intermediate bus voltage. The inductor voltage is kept inductor is 20 microsecond I have kept and the intermediate bus capacitor is set to 600 microfarad.

And we want to see if we change this value because you know this value depends on the ripple characteristics, but we can change some higher and lower value, but I want to show this value of intermediate bus capacitor has a significant strong influence on the stability of the cascaded system.

For the PoL converter, inductance is set to 0.5 Microhenry and which I kept the same as our earlier configuration the time period is 2 microsecond, capacitor is 200 micro farad which we have already designed earlier using a power stage design criteria.

But in this converter we kept the reference voltage to be 1 volt because we want to achieve 1 volt output. Overall input voltage is 48 volt, which is the input to the IBC and we kept the parasitic to be more or less same for both the converters.

This is for sake of simplicity, but I as I said that you can take different parasitic as well. Now, we want to first run that if you go to the Simulink model; we want to run the PoL converter using open loop sorry, closed loop using current mode control and the IBC converter using open loop using a duty ratio D1 and I will say what is D1 ok.

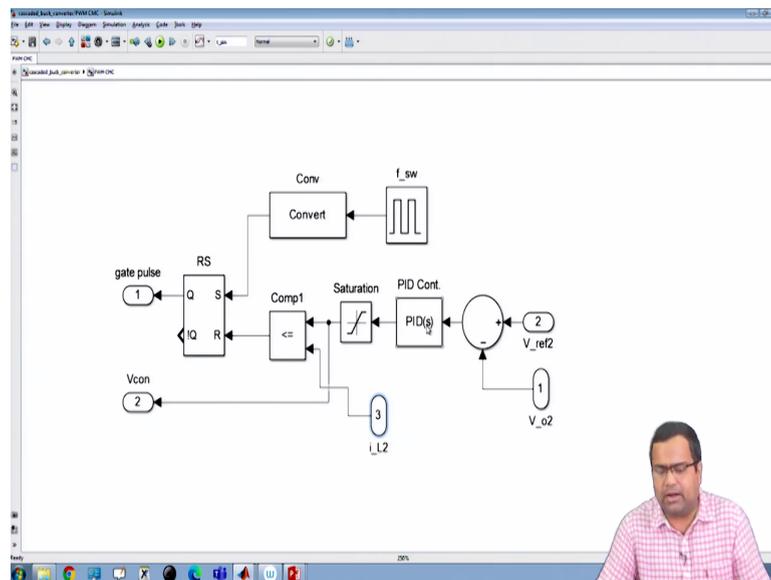
So, now, in this MATLAB file I have discussed all these MATLAB simulation files, the process is same. So, where we will call this parameter file which is stored here all the parameter values.

Then I have set D1 which is a nominal duty ratio and that is the output by input for the first stage and the output of the desired output of the first stage is  $V_{ref1}$ , which is set to 12 volt and the input is 48V which I discussed. For the second stage, though, it is not required duty ratio because we are running in closed loop, but for sake of you know completeness.

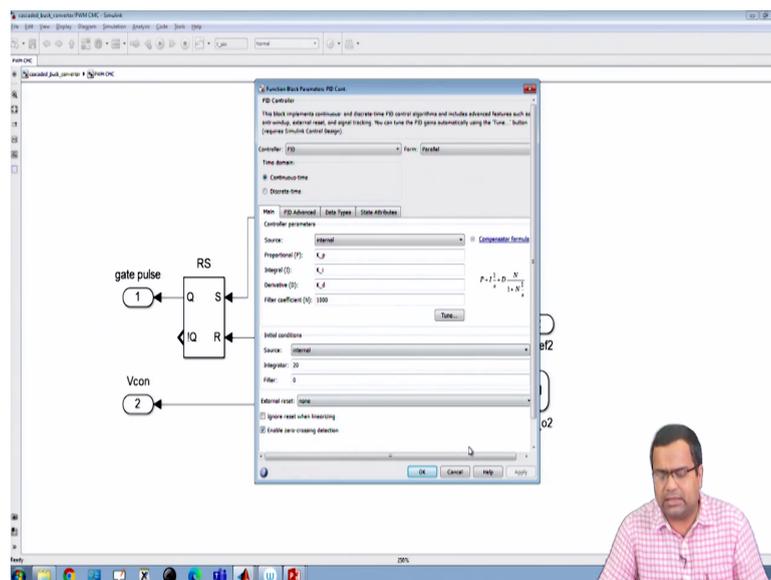
So, D2 is nothing, but  $V_{ref2}$  which is the desired output voltage of the second stage PoL converter and input to the PoL converter is nothing, but the intermediate bus, but our desired value of the intermediate bus is  $V_{ref1}$ . So, the desired output voltage is D2 desired duty ratio is D2 for the pol converter.

Now, I am considering power level of 20 ampere because my PoL output voltage desired value is 1 volt and I want to operate the PoL converter with a nominal current of 20 ampere because for single phase this is somewhat standard. So, 20 ampere into 1 volt is a 20 watt. So, what should be the resistance because it is a resistive load. So, it will be  $V_{reference}^2$  square by  $P_0$  ok.

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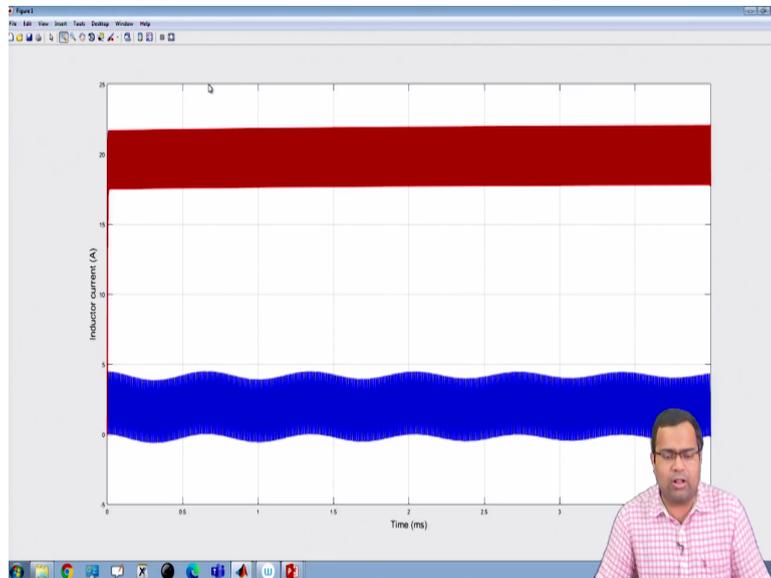


Now, if we go back inside this current mode control and this block is already explained, but we have also discussed the current mode control does not require a PID controller a PI controller is enough, but we are using a default PID structure available in the MATLAB.

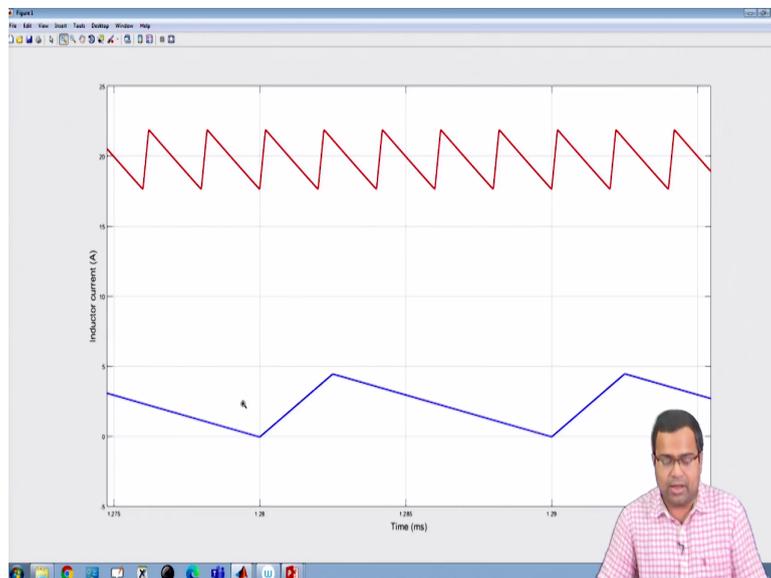
Where proportional gain integral gain we are defining from the MATLAB and the derivative gain, we are setting to 0 from a MATLAB itself and we are setting some initial value of the

integrator ok. So, you can keep it 0 there is no problem ok. Now let us run the simulation and check.

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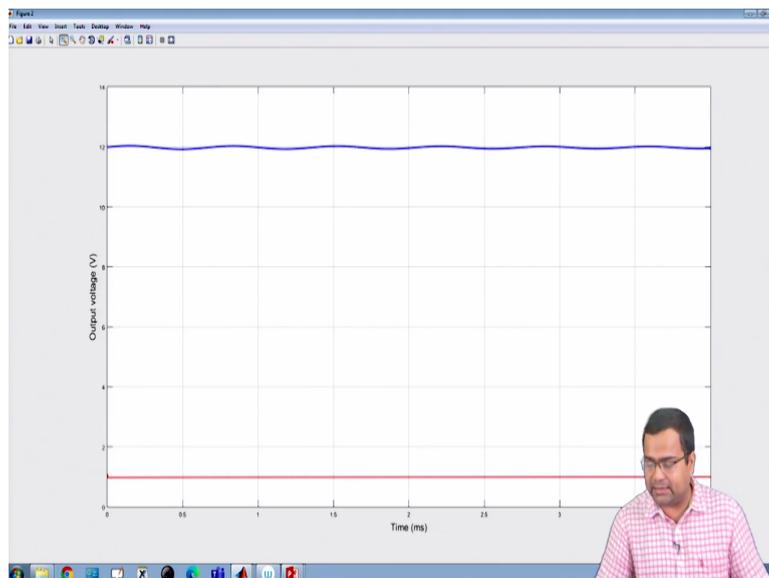
So, if I run the simulation, let us go to the simulation result and see. So, for all the simulation result traces for the inductor current, I have considered the rate trace for the PoL inductor current and the blue traces for the IBC inductor current ok.

So, let us go back and check ok. So, here I am showing you know if you see the waveform, the top one is the PoL inductor current and since I want to regulate the PoL output to 1 volt and my desired output power is 20 watt. So, my desired output current is 20 ampere.

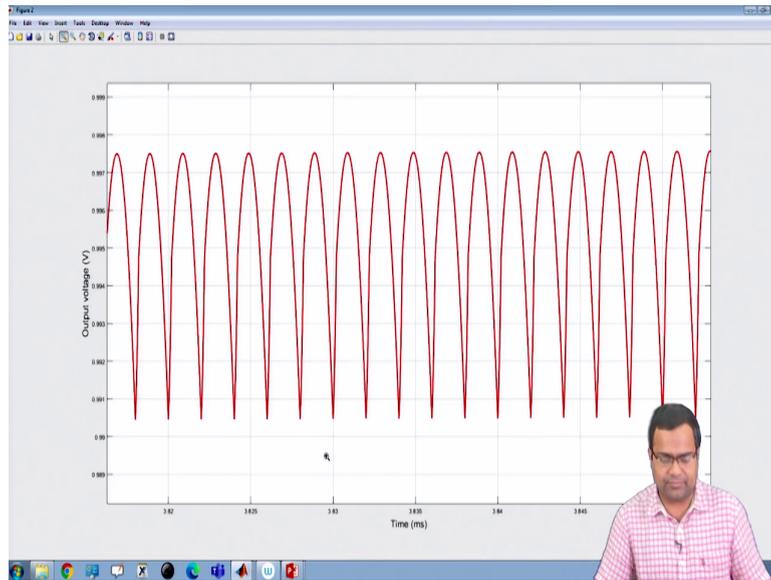
So, you can see the average inductor current is we are closely 20 ampere; that means we are achieving that desired current using this PoL converter. In the IBC converter, you can see the switching frequency or time period is 0.01 millisecond; that means, 10 microsecond.

Whereas, there are 5 such cycle within one cycle of the IBC, 5 cycle of PoL inductor current is same as the one cycle of the IBC inductor current. So, PoL converter is 5 time faster and its time period is 2 microsecond that can be shown from here. So, these are the inductor current.

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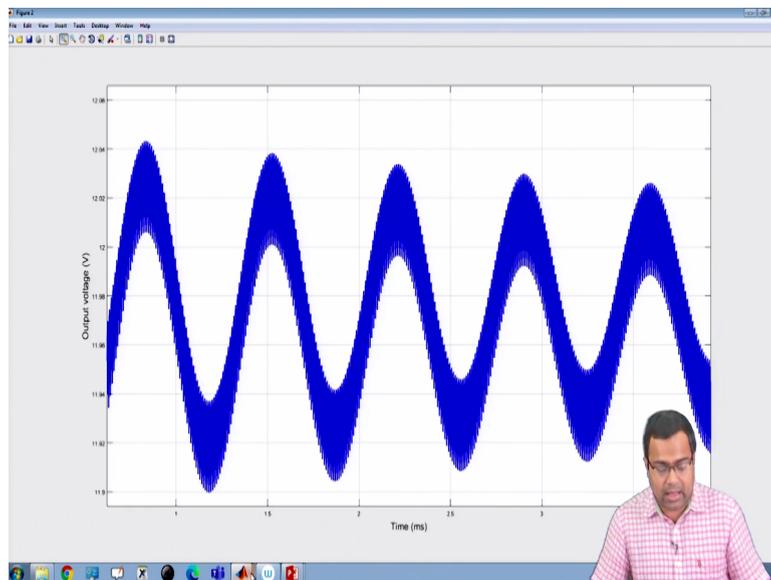


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Then if you go to the output voltage waveform, I will show you again the rate traces indicate the inductor current waveform of the IBC PoL converter, that is nearly 1 volt it is not coming it will take some more time, but it is almost 1-volt average voltage ok.

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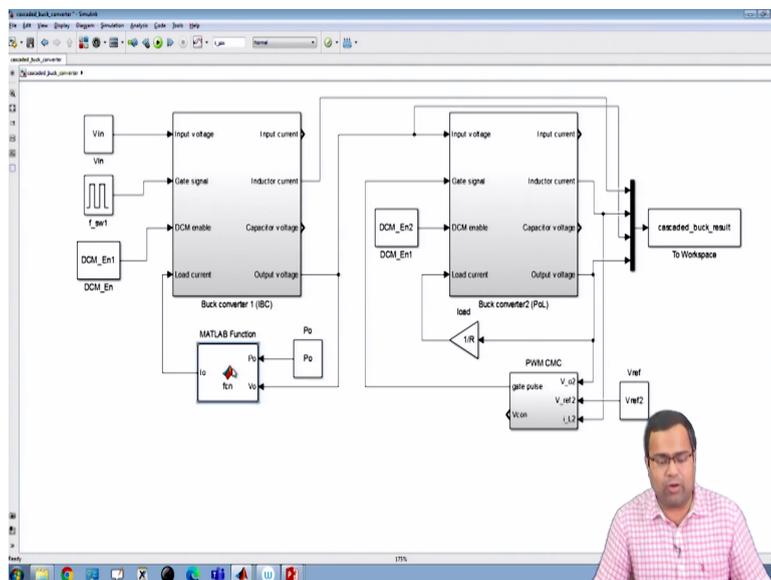
Whereas, if you see the average output voltage of the IBC converter is roughly 1-volt, 12 volt because we want to achieve to a desired voltage of 12 volt, but since it is running in open loop it may not maintain 12 volt. But what is important here to observe that the PoL converter

output voltage is somewhat oscillatory and if we closely watch this oscillation, this oscillation seems to be decaying; that means, you know the amplitude of oscillation is slowly decaying. It will take time, but it is decaying very slowly ok. So, this is one simulation configuration I am running.

Now, we want to take the second one; that means, we want to take if the second case we replace this IBC a PoL converter with a constant power load, then can we get identical result? Right now you know whatever we have simulated, we have used 2 DC-DC converter both PoL and IBC; PoL was operating under current mode control and IBC was in open loop.

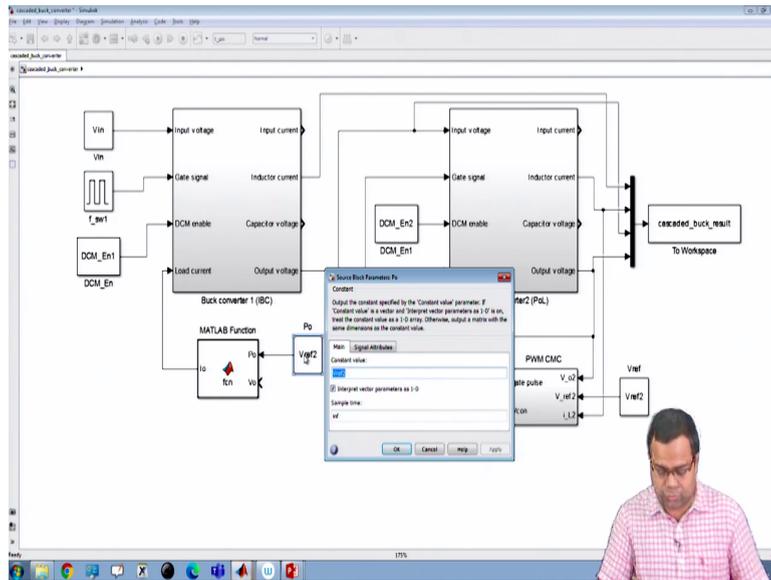
Now, I want to repeat the experiment where IBC still remains in open loop with the same configuration, but PoL converter, closed loop PoL converter is replaced by a constant power load and which is the magnitude of the constant power is 20 watt that we have discussed. So, in this case if we go back to this now, what we are doing?

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The second stage we do not want to use anymore; that means, we want to remove this load current. What is the load current? It is now constant; it is coming out to be a constant power load. What is the amplitude of the constant power? That means we want this constant power  $P_0$  this to be  $P_0$ . It is my constant power which I have already defined from the simulation file and the output voltage is here.

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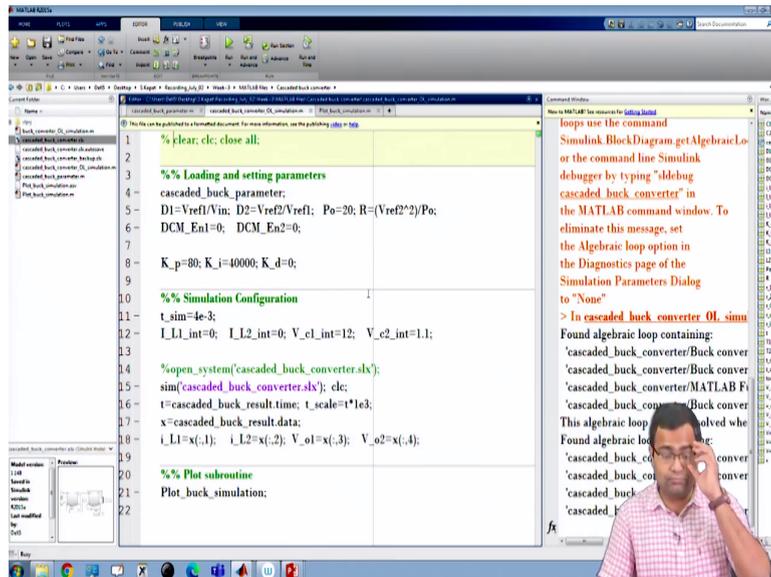
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```
function Io = fcn(Po,Vo)
%fcodegen
Io = Po/Vo;
```

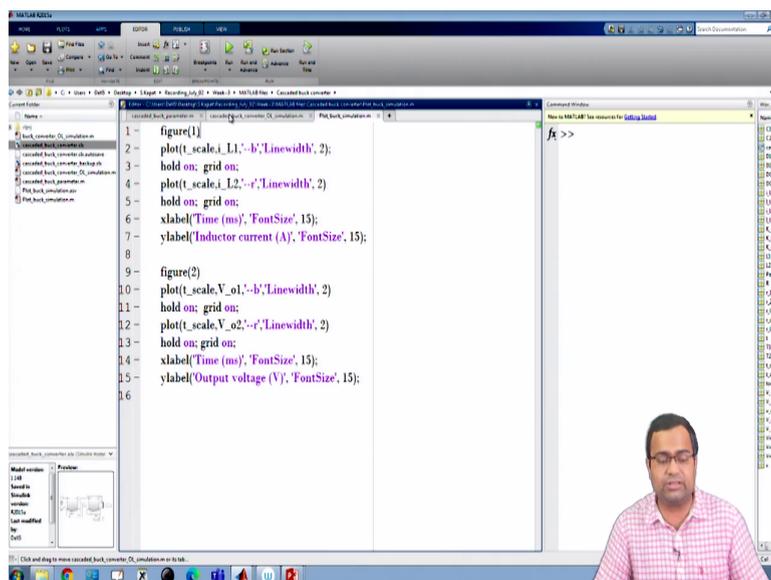
The screenshot shows a MATLAB editor window with a function file named 'Io = fcn(Po,Vo)'. The code is: %function Io = fcn(Po,Vo) %fcodegen Io = Po/Vo;. The editor also shows a list of files on the left and a command window on the right.

And if you go inside, it is just the simple MATLAB function file where the load current is nothing but power by voltage. So, since the power is constant, see if there is any variation in the voltage and then it will be current will also vary. So, it's a non-linear load ok. So, it just a function file.

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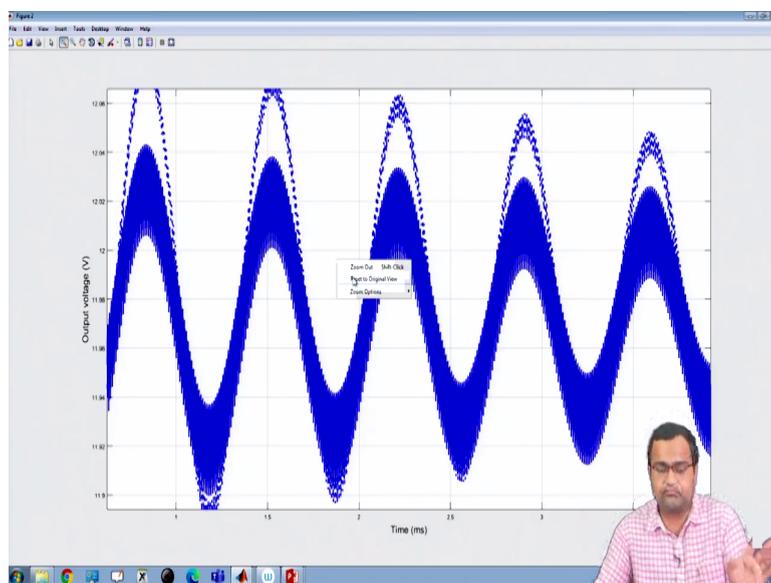


Now, for this case of simulation, we want to repeat; that means, we want to retain the earlier traces, but we want to use dotted line now, because we want to check whether they are exactly identical or not. Right now, we are not using earlier simulation. We are now considering the IBC converter open loop which is same, but PoL converter is replaced by a constant power load that we have discussed here, and now it is a constant power load.

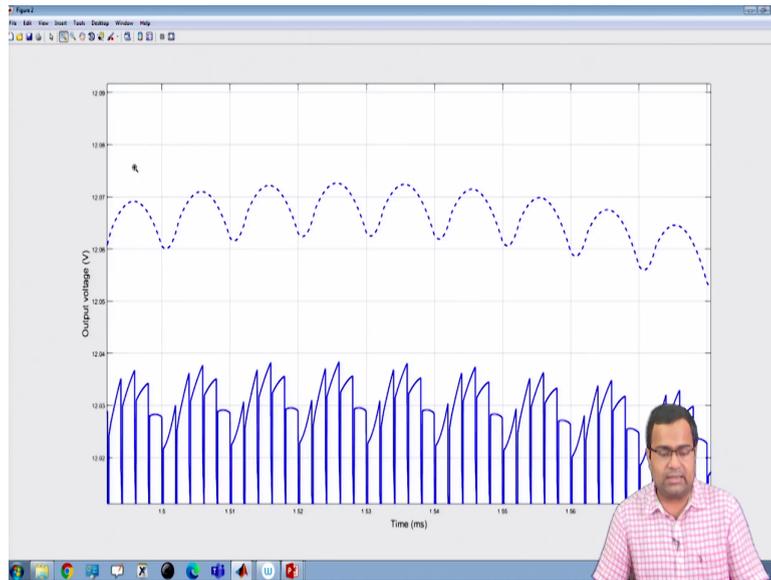
Though it is running like this converter in the second stage, but I want to evaluate the dynamics. I want to investigate the dynamics of the IBC which is not connected with the PoL converter anymore ok.

So, if I run it now with this condition, by keeping all initial conditions same, you can see the output power is 20 watt. Now it is running under constant power load and where we want to focus on the waveform of the IBC not PoL, because in this case PoL is not connected to the IBC ok.

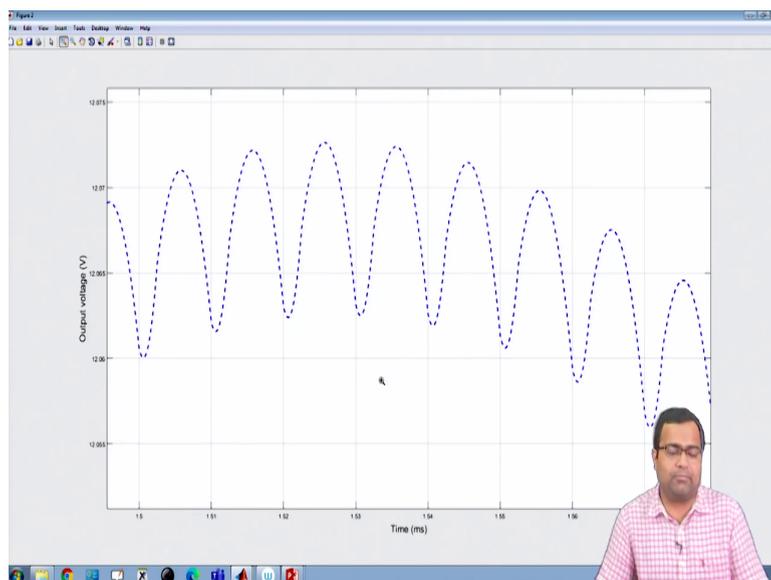
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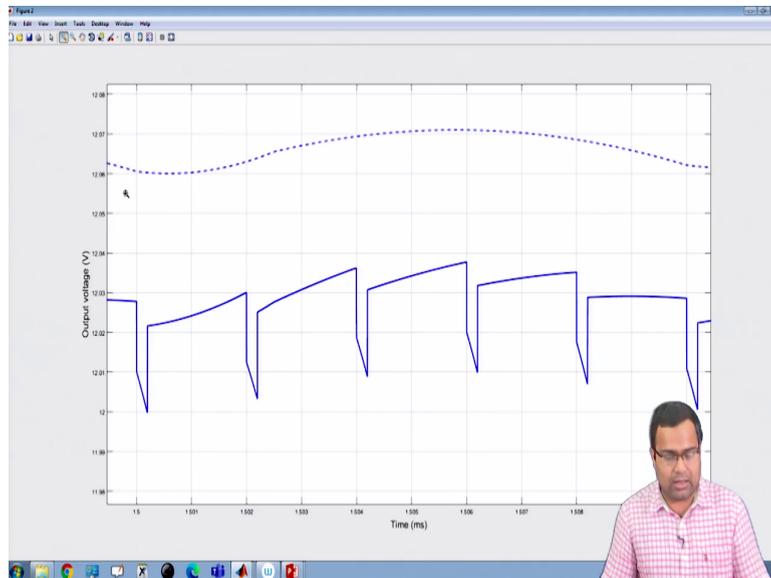


Now, let us go and check. So, here you can see there are two traces; the one trace is the; this trace is the output voltage waveform with PoL you know constant power load; that means, if I zoom it if I take one particular cycle ok.

So, if we go inside and if we take a closer look of this, you can say there are multiple switching with discontinuity. This is the case when the PoL converter was connected because the PoL converter input current was discontinuous. As a result, it actually injects some

discontinuous voltage jump because there is an ESR in the capacitor of the intermediate bus. And any discontinuous current in the capacitor current will actually cause a discrete jump.

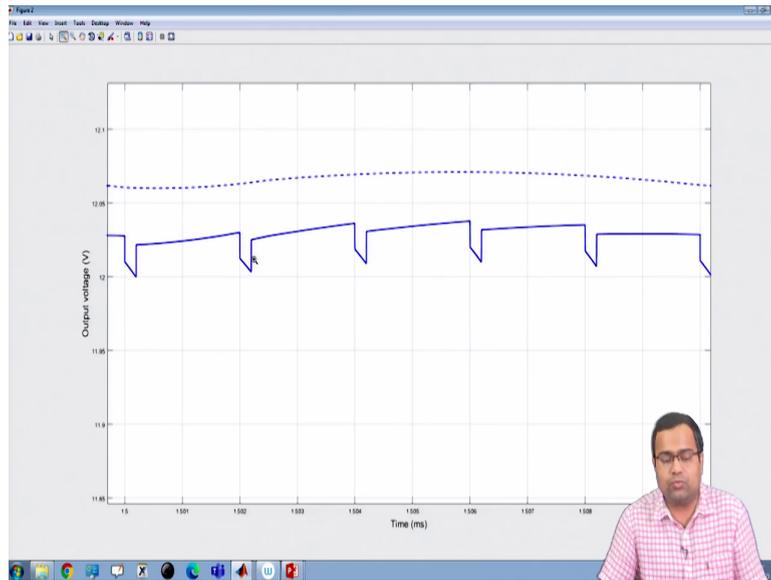
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So, that is why you can see there are five cycles within one cycle of PoL IBC. So, if you see this is the one cycle of the IBC from this 1.5 to 1.51, one complete cycle of the IBC switching cycle. In this cycle, when we are considering simply PoL converter, this discontinuous ripples are not appearing because is current is not discontinuous output current is not discontinuous.

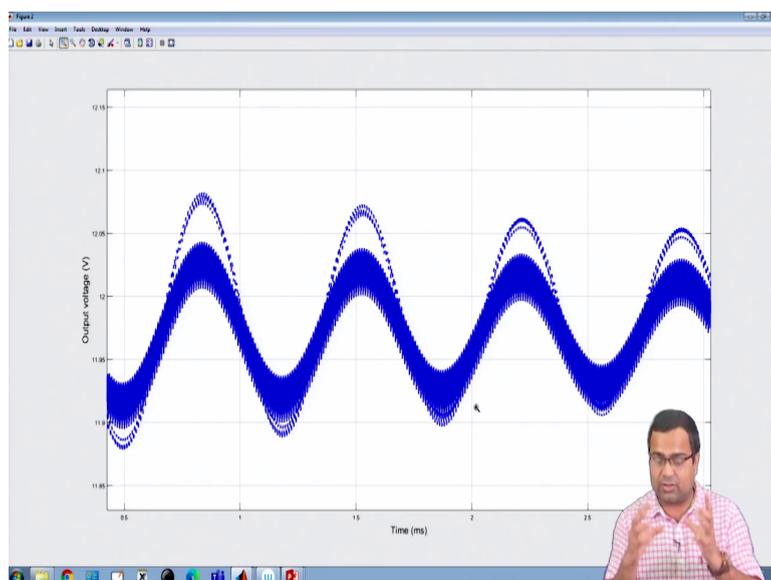
But in case of actual switch simulation when the PoL was connected, you can see there are discrete jump and these discrete jumps are due to the discontinuous current of the PoL input current and that will appear at the capacitor of the IBC and which has a ESR.

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So, there is a discrete jump which happens in every switching cycle, every switching transition of the PoL converter and that will happen 5 times in a cycle and that we can; you can clearly observe from here. If you take from here to here, there will be 5 1, 2, 3, 4, 5 and so, 5, 2 times ok.

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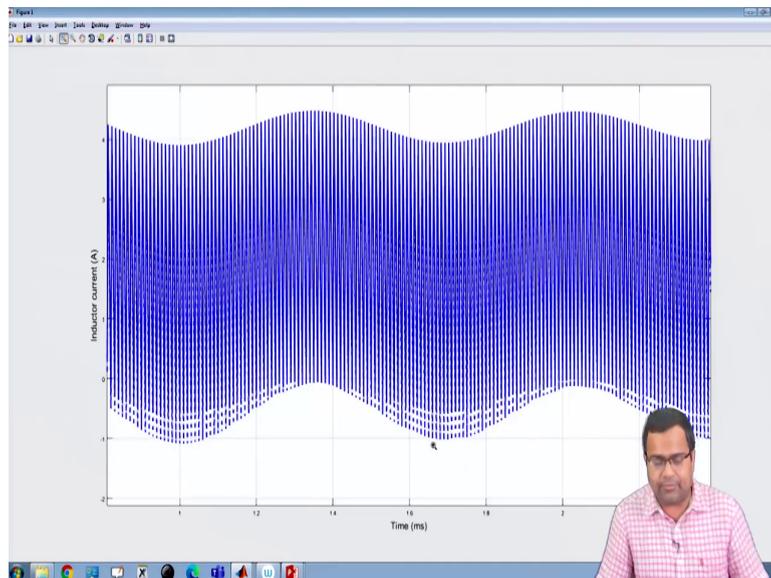


But what we want to observe that means, if we take the 2 output traces, the one with actual switch simulation of the PoL and the other PoL is replaced by a constant power load the waveforms are not exactly identical.

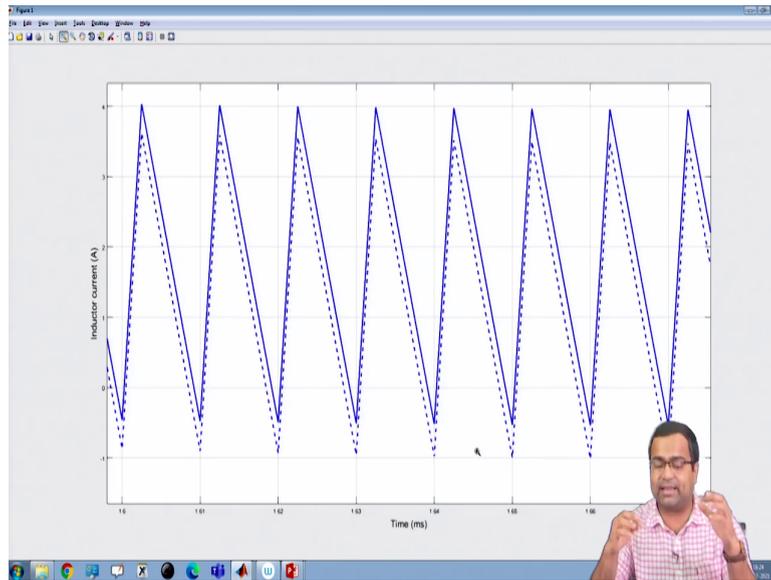
They are not exactly identical because you know it is well reported in the literature. All investigations are carried out simply by taking constant power load, but if we go to actual switch level behavior, they are very much different and in sometime the complex non-linear behavior in the PoL can cause stability problem in the IBC and which will not be reflected when we are replacing that PoL with an actual constant power load.

So, in average sense in low frequency dynamics they are somewhat you know similar that is why if you see they are average dynamic they are close, but they are not exactly identical, but they reasonably capture the average behavior you know the profile are somewhat similar but with slightly different amplitude.

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If you go to the inductor current waveform, if we go to the inductor current waveform if we are interested in this inductor current waveform. So, you can see the inductor current waveforms are not exactly identical. There is a slight difference. Again, the cycle, by cycle behavior they will be no they will not be same, but in an average sense the profile has some oscillatory property and which is also true here, which is also reflected here.

That means a current mode controlled PoL converter can be replaced by a constant power load. This is valid in the sense of small low frequency behavior. This can reasonably capture the slow scale instability of the IBC converter, but it does not capture the switching dynamics and non-linear phenomena of this two-stage converter ok.

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### Simulation Case Study

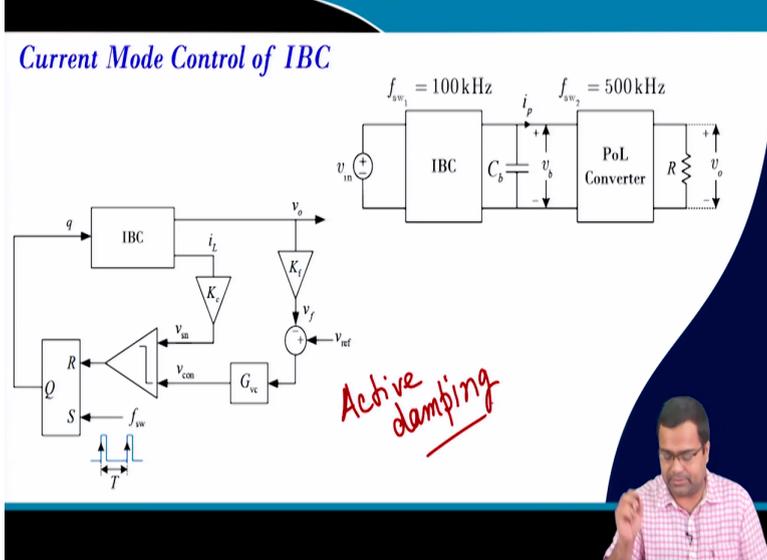
- Case 1:
  - Use two separate converters (IBC and PoL converter)
  - Operate IBC in open loop at  $f_{sw_1} = 100\text{kHz}$
  - Operate PoL converter under CMC at  $f_{sw_2} = 500\text{kHz}$
- Case 2:
  - Keep the same IBC configuration
  - Replace PoL converter using a CPL where  $P_o = v_o i_o$



So, the simulation case study, two separate converter we have operated in 100 kilohertz and 500 kilohertz, in case to keep the IBC configuration same and we have replaced a constant power load and we saw that their behavior are somewhat close in the average sense.

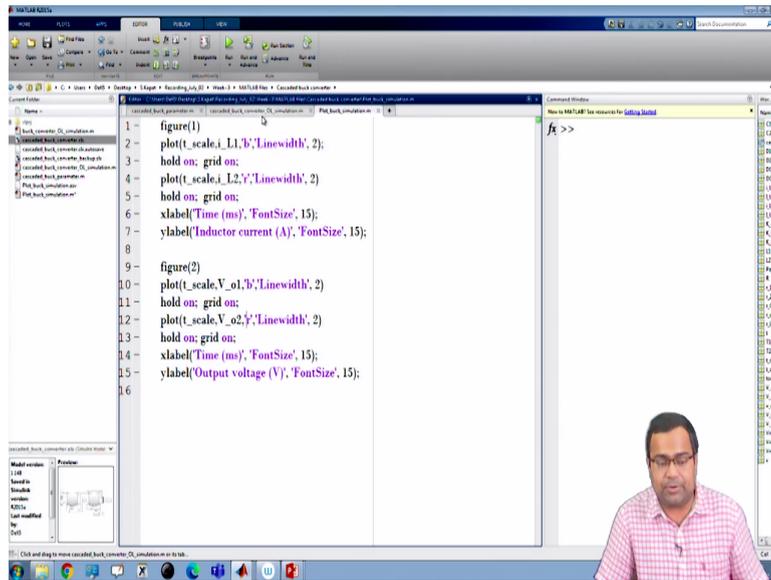
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### Current Mode Control of IBC



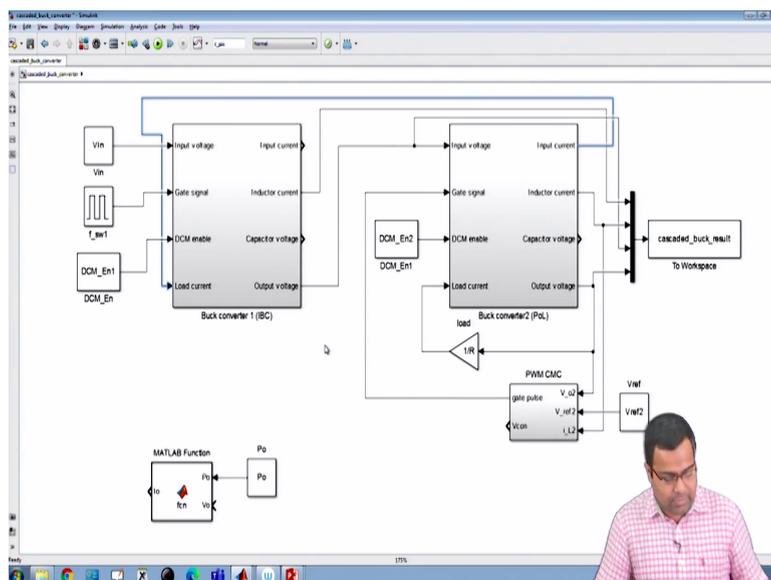
Active damping

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```
1 = figure(1)
2 = plot(t_scale,t_L1,'Linewidth', 2);
3 = hold on; grid on;
4 = plot(t_scale,t_L2,'Linewidth', 2);
5 = hold on; grid on;
6 = xlabel('Time (ms)', 'FontSize', 15);
7 = ylabel('Inductor current (A)', 'FontSize', 15);
8
9 = figure(2)
10 = plot(t_scale,V_o1,'Linewidth', 2);
11 = hold on; grid on;
12 = plot(t_scale,V_o2,'Linewidth', 2);
13 = hold on; grid on;
14 = xlabel('Time (ms)', 'FontSize', 15);
15 = ylabel('Output voltage (V)', 'FontSize', 15);
16
```

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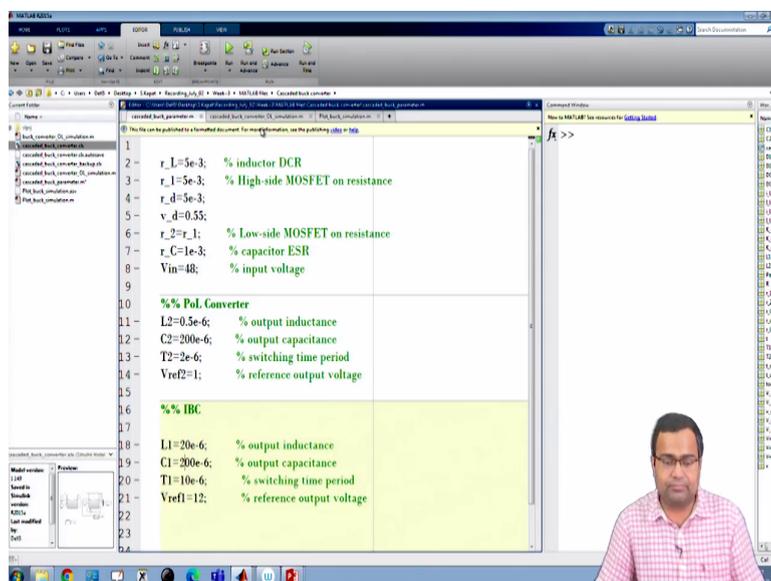


Now, one thing we want to observe before we do a closed loop control. What we found now? We want to go for actual switch simulation. Actually constant power load, this was just for sake of analogy because it is you know there are a lot of research papers where they simply consider this configuration, but we do not want to take this configuration anymore.

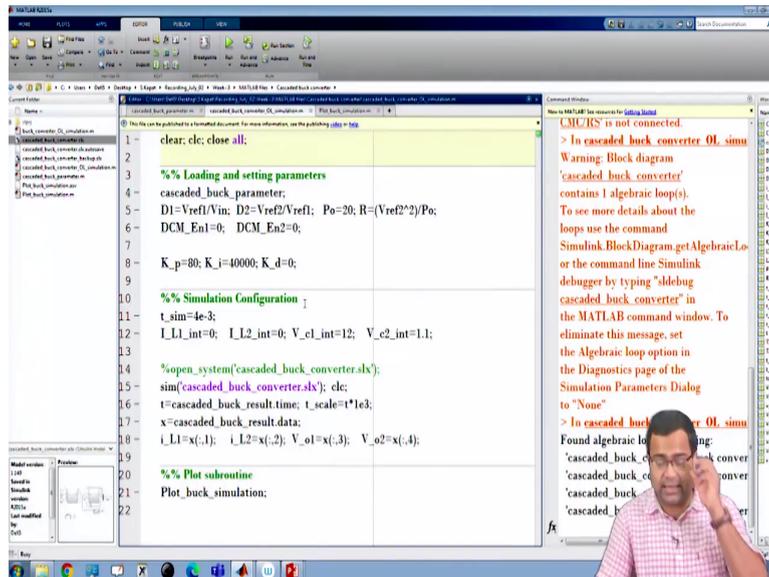
But this can be used for low frequency you know stability analysis and which can be reasonably you know reasonably which can capture the low frequency stability behavior property.

Now, we are going to actual switch simulation and we want to investigate that what will happen if what will happen if; that means, we saw using two buck converter under this configuration; the IBC was operated in open loop and we saw some slow scale oscillation, but the oscillation was dying out. But we want to change the parameter and see what is the impact.

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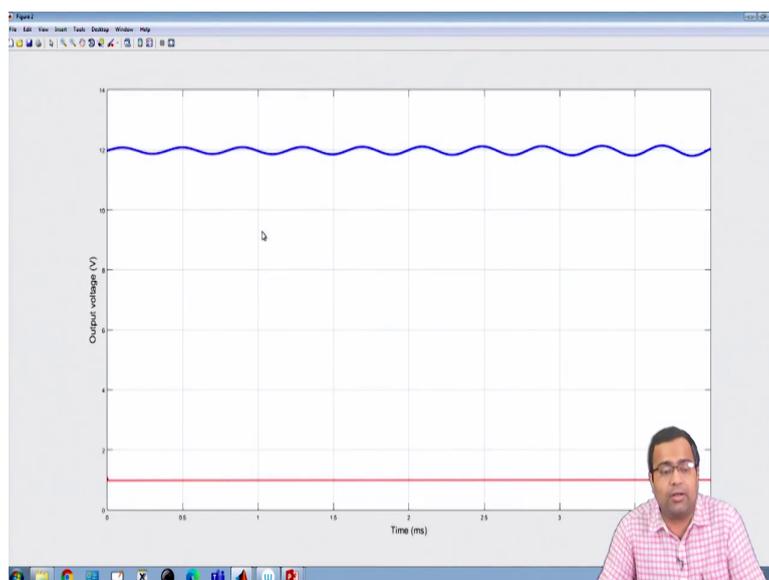


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Suppose, if we reduce the intermediate bus capacitor from 600 microfarad to 200 microfarad and if we run the simulation and see whether the change in IBC output capacitor can affect the stability or not this is important because we sometime need to keep a smaller capacity in the bus architecture because this will ok.

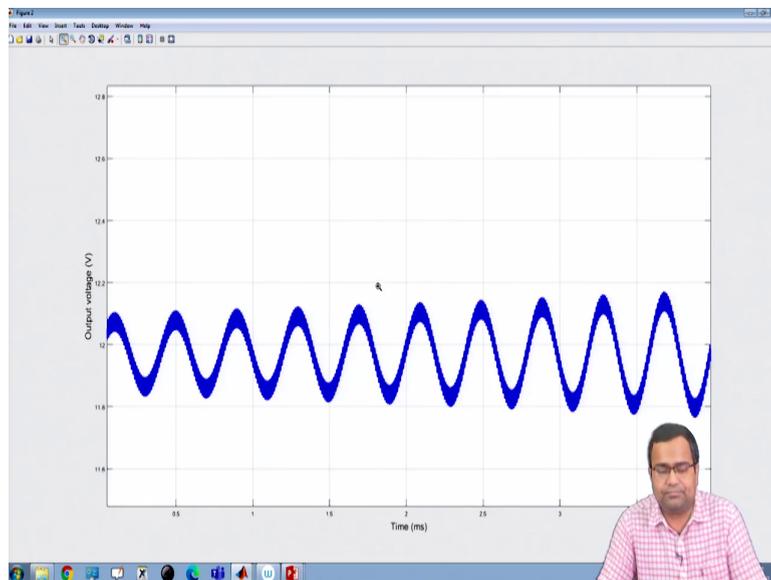
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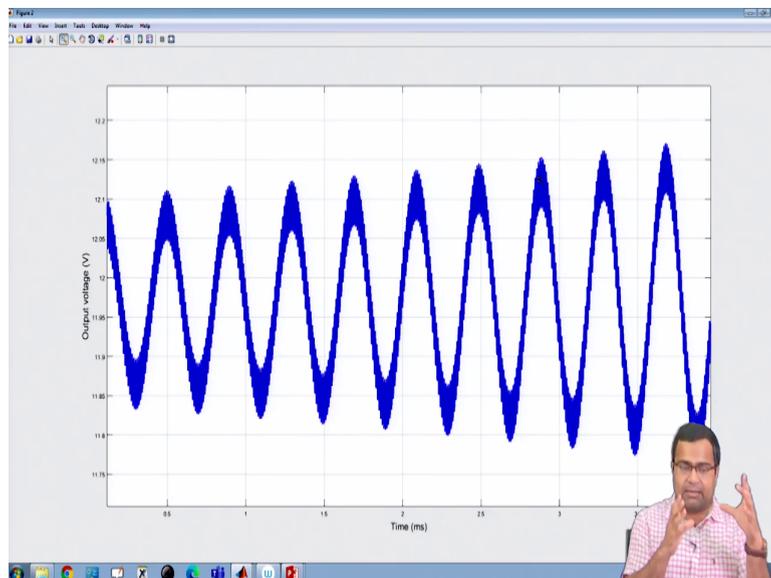
So, we will come to the discussion because this smaller capacitor of intermediate bus architecture can help to quickly change the intermediate bus voltage which can be used to

optimize the performance and the efficiency of the PoL converter this is very much useful for you know tradeoff between performance and efficiency in the two stage architecture.

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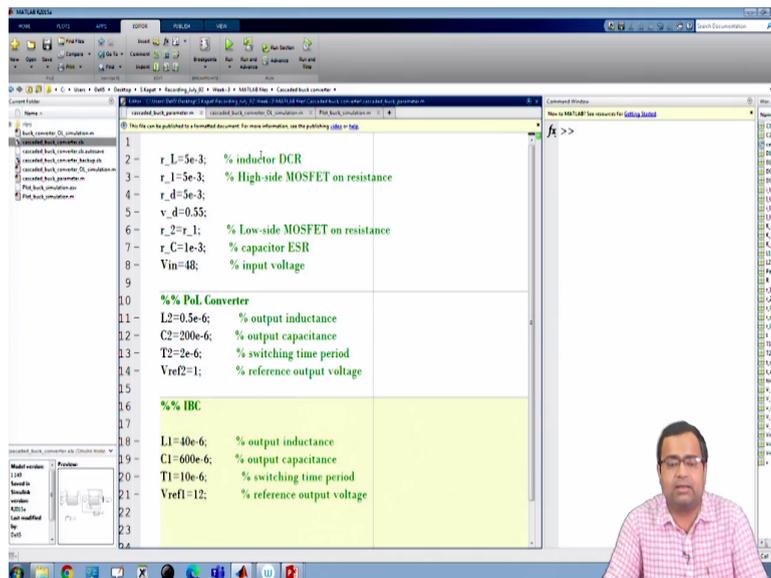
We saw if we reduce the capacitor value, then the stability of the IBC also gets affected. That means, IBC now the oscillation is slowly increasing; that means, this is the typical example, if you take the average waveform, which behaves like a linear system phenomena and the

oscillation is increasing exponentially and this is the typical case for an unstable open loop plant.

That means, here IBC is driving a PoL converter, and the PoL converter is tightly regulated using current mode control. Since it resembles to some extent the constant power load and when an open loop buck converter driving a constant power load. So, when we are reducing the intermediate bus capacitor, the open loop converter become unstable. And as a result, the output voltage is slowly the oscillation is happening and this oscillation amplitude is slowly increasing ok.

And if you wait for long time, that oscillation will grow up significantly and it can damage the converter and the device and it can lead to complete collapse of the closed loop two stage converter ok.

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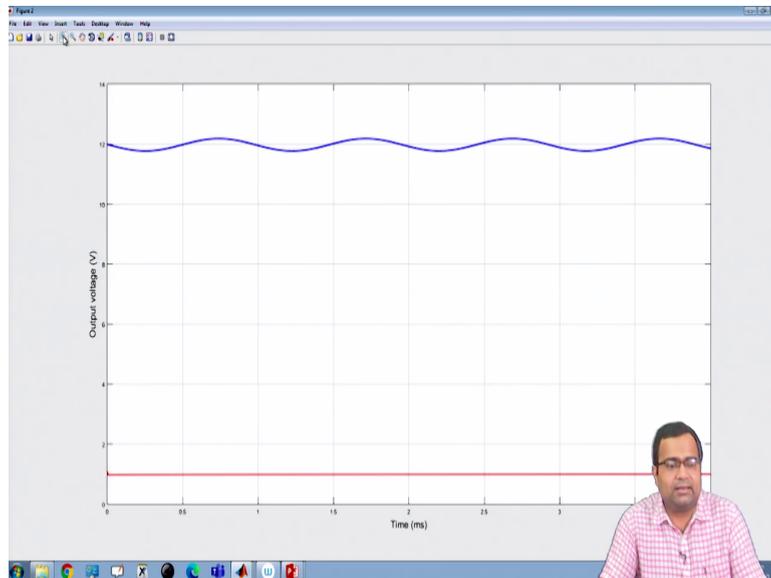


I also want to see whether there is any impact of the inductor that means. We are going back to the capacitor suppose if we increase the inductance value of the first stage because we want to further increase efficiency by increasing inductance value so, that the ripple of the current can be reduced and conduction loss can be improved.

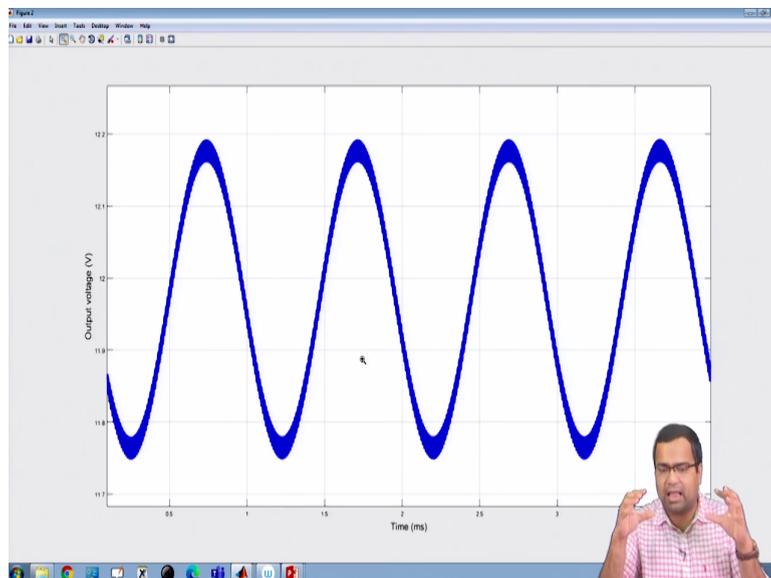
I mean, although it is not necessary, but we want to investigate whether or not this inductor has any effect. So, in this case I have changed the inductor value of the first stage from 20

microhenry to 40 microhenry where my capacitor is restored to 600 microfarad because you want to see the effect individually 1 by 1.

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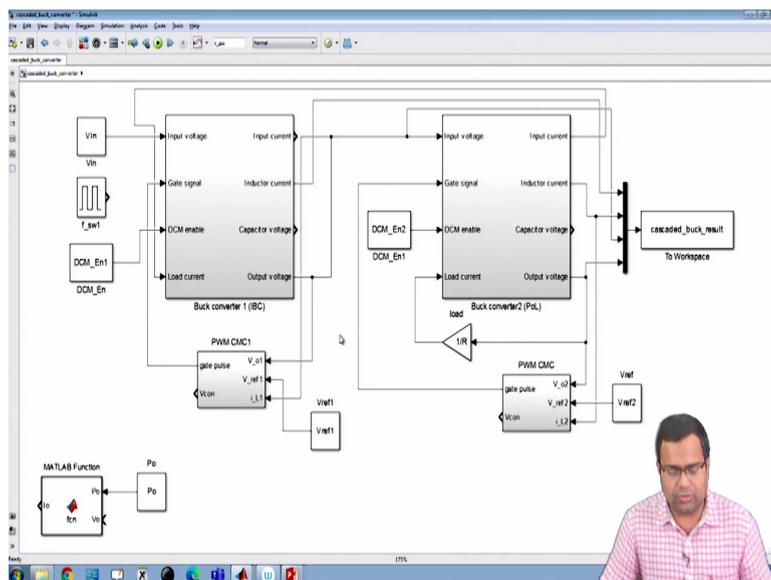


So, you can see here if we increase the volt inductor value of the first stage converter, it is somewhat oscillatory slowly increasing, but it is somewhat oscillatory and this may lead to something called limit cycle oscillation ok.

Because there is a sustain oscillation, we need to further investigate whether it is a limit cycle oscillation or the oscillation is growing up or coming down. But there is a possibility, and it is also investigated earlier, that there can be an existence of limit cycle oscillation in such cases. In this case for a larger inductance, it may end up with a limit cycle oscillation; that means, it is a sort of damping in the closed loop system of the 2 stage converter where the first stage is an open loop.

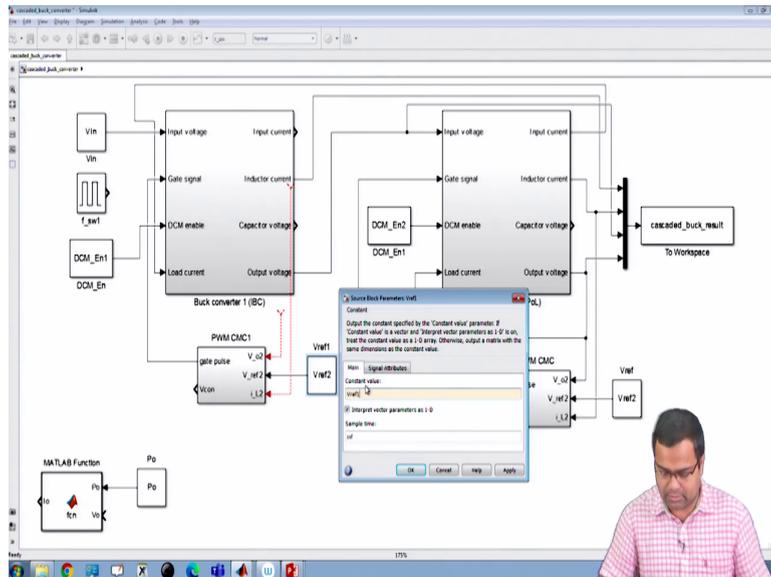
How to improve damping inject damping? So, now, we want to control the IBC using current mode control and this is also reported, you know in much literature that current mode control can provide active damping and that we have already discussed in the context of current mode control.

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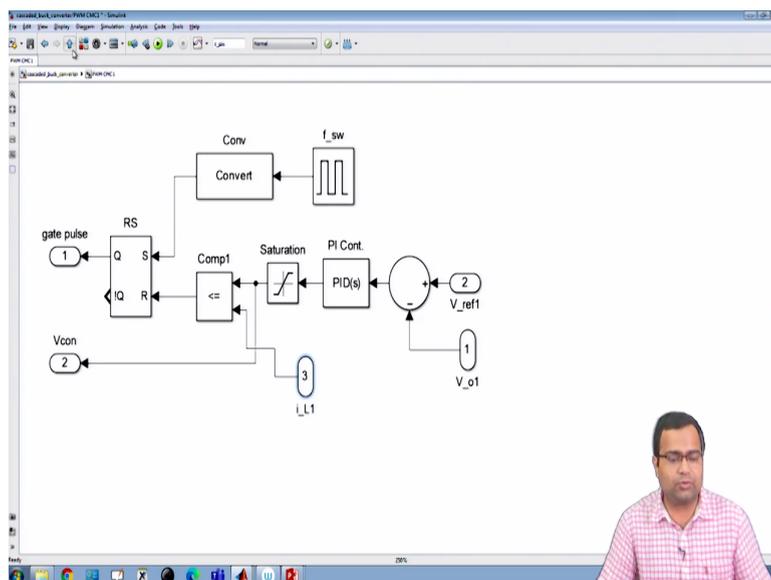


Now, if we go back to our simulation and now if we change these if we now use another current mode control block diagram; that means, we just simply copy paste we keep this you know somewhere here because this block we do not need it ok. So, it has gone down, yeah.

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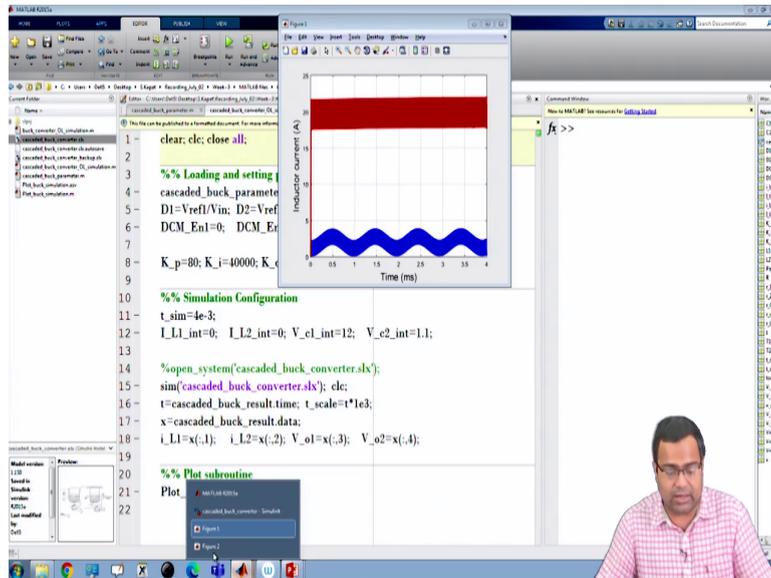
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So, what I am going to do now? I want to use current mode control for the so; that means, we need to provide this is the gate signal, and this is my  $V_{ref1}$  the first stage and I need to connect this should be my  $V_{ref}$  sorry this should be my  $V_{ref1}$  this should be my  $V_{o1}$  and inductor current 1 ok.

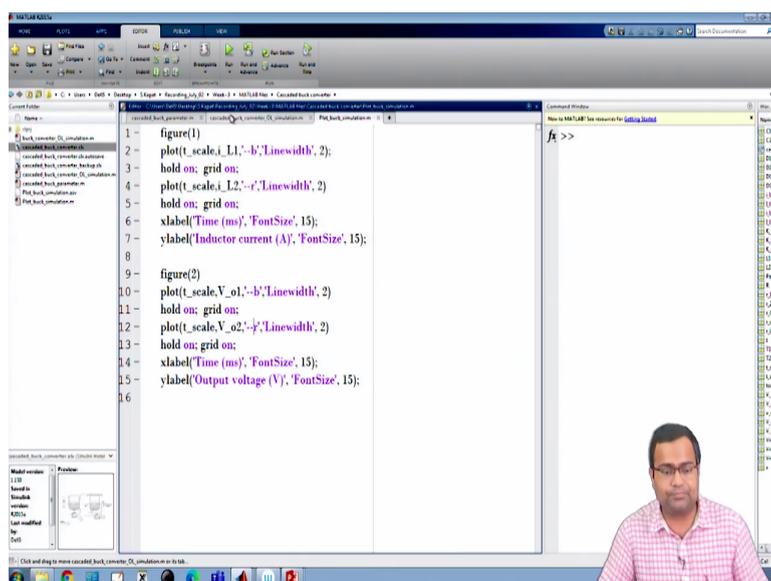
Every, all other blocks are same. So, I need to connect this to the inductor current, this is what and the output voltage ok and then ok. So, now, it is under current mode control, same configuration we are using ok.

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It is not necessary to run in same the same configuration, but now we are running for the same simulation result that we obtain which shows unstable behavior.

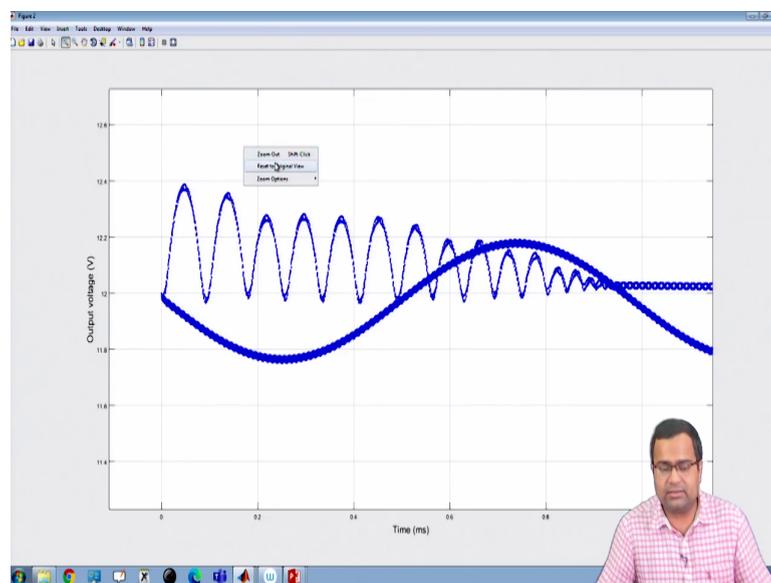
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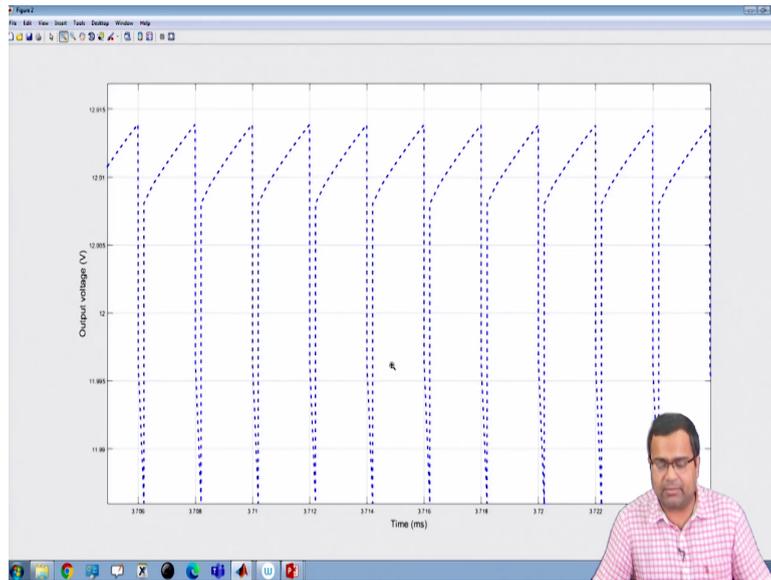
Now, we want to run under closed loop both the converter now running under closed loop and we want to overlap the two simulation results by dotted curve which is the, now IBC is running in the closed loop current mode control ok.

So, now, we are running both the converter closed loop earlier PoL was under current mode control closed loop, now IBC is also we are running in current mode control under closed loop configuration. And we want to see whether can we provide active damping by means of current mode control or not.

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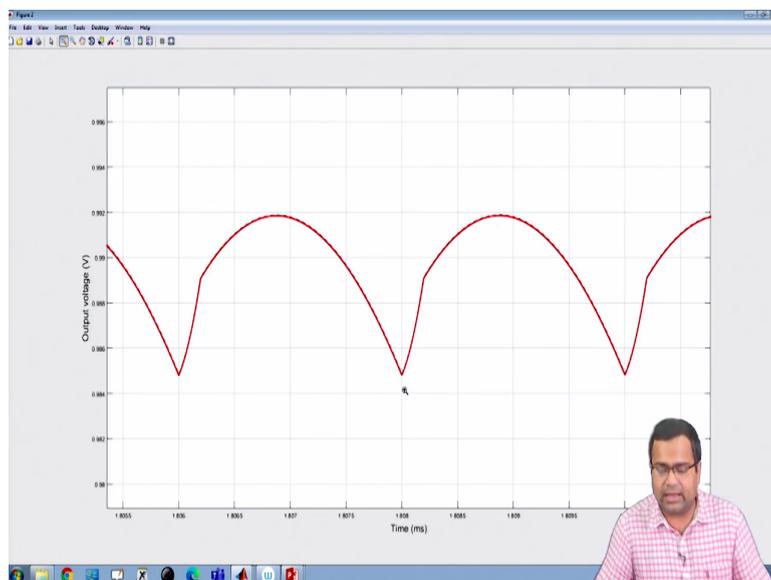


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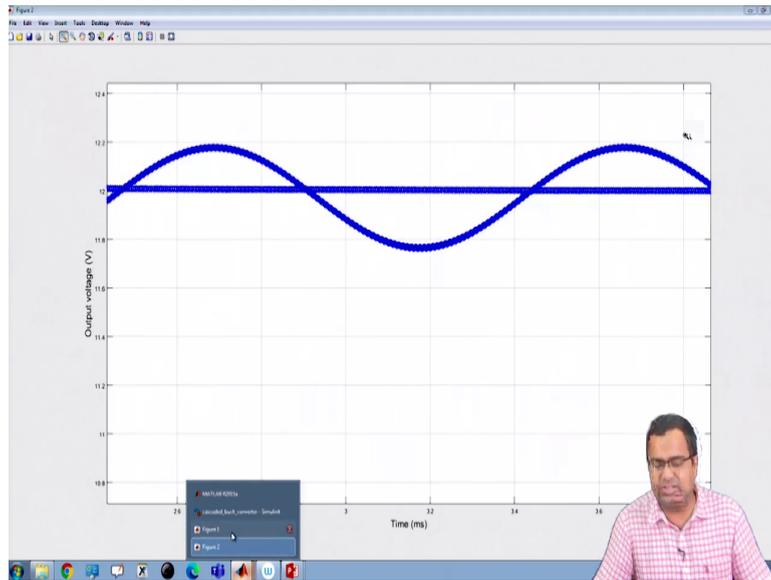


So, you can see here that initially there are some startup transient, after that. So, it become stable we can say that this is the waveform that it become stable. So, this is the dotted line becomes stable.

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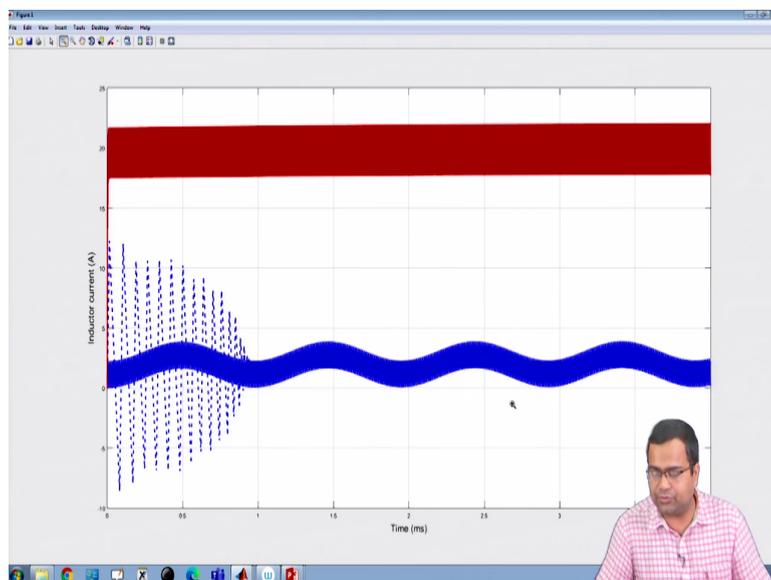


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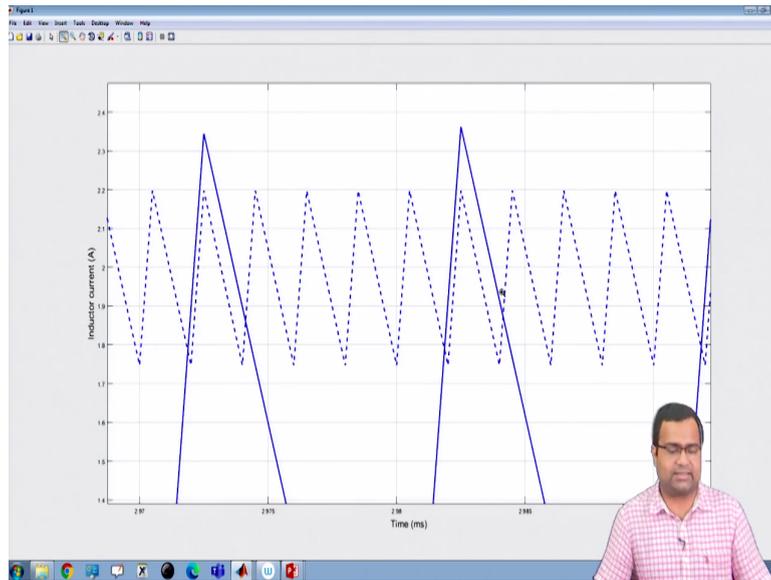


Whereas, in both cases this inductor currents are stable. So, output voltage like you know both waveforms have overlap they are overlap. So, now, the current mode control is able to stabilize this converter and if you go to the current waveform.

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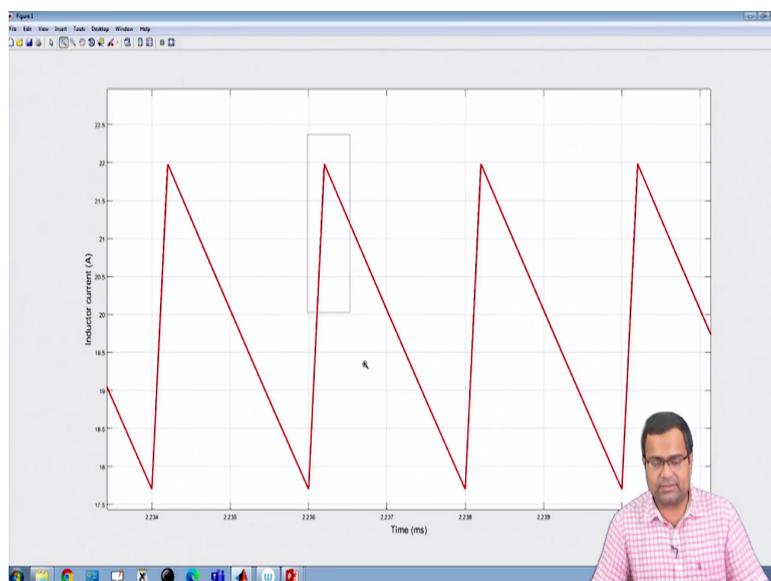


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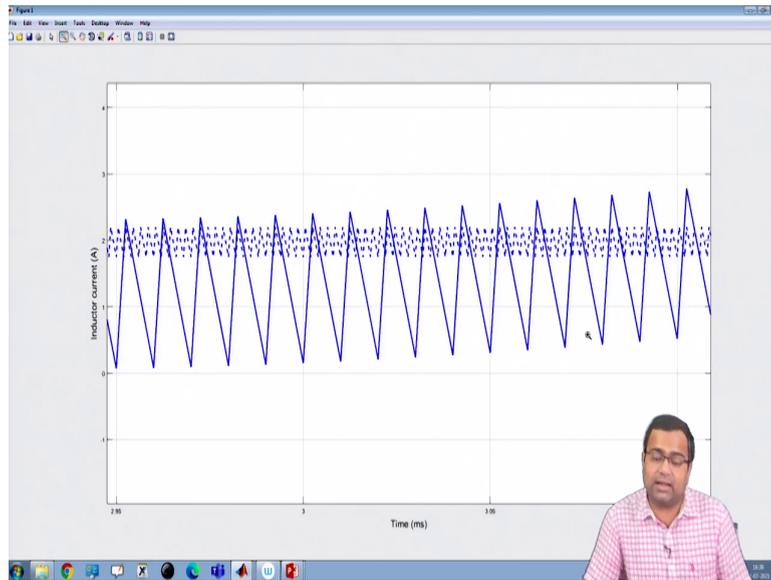


So, I will show you that if you zoom it, now inductor current become stable for this case ok.

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So, this IBC converter they are matched exactly. So, it is very hard to distinguish ok and stable, but now if it is even with a larger inductor.

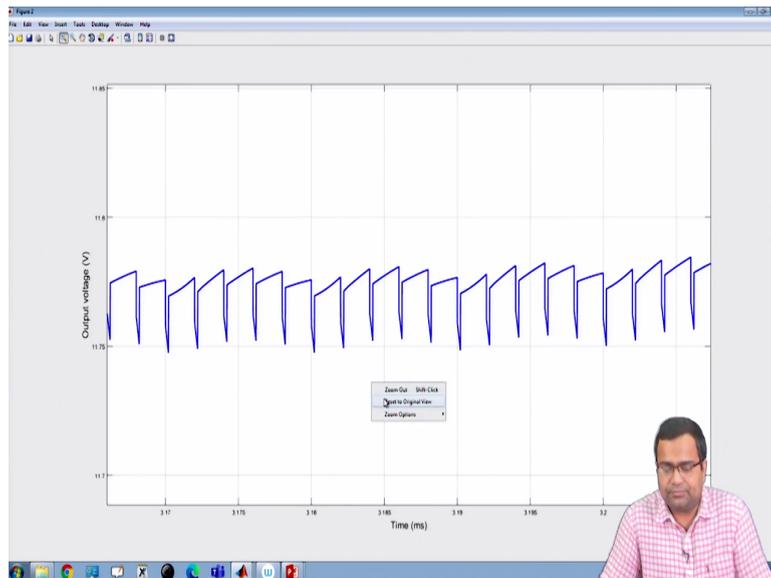
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```
1 figure(1)
2 plot(t_scale,i_L1,'-b','LineWidth',2);
3 hold on; grid on;
4 plot(t_scale,i_L2,'-r','LineWidth',2)
5 hold on; grid on;
6 xlabel('Time (ms)', 'FontSize', 15);
7 ylabel('Inductor current (A)', 'FontSize', 15);
8
9
10 figure(2)
11 plot(t_scale,V_o1,'-b','LineWidth',2)
12 hold on; grid on;
13 plot(t_scale,V_o2,'-r','LineWidth',2)
14 hold on; grid on;
15 xlabel('Time (ms)', 'FontSize', 15);
16 ylabel('Output voltage (V)', 'FontSize', 15);
```

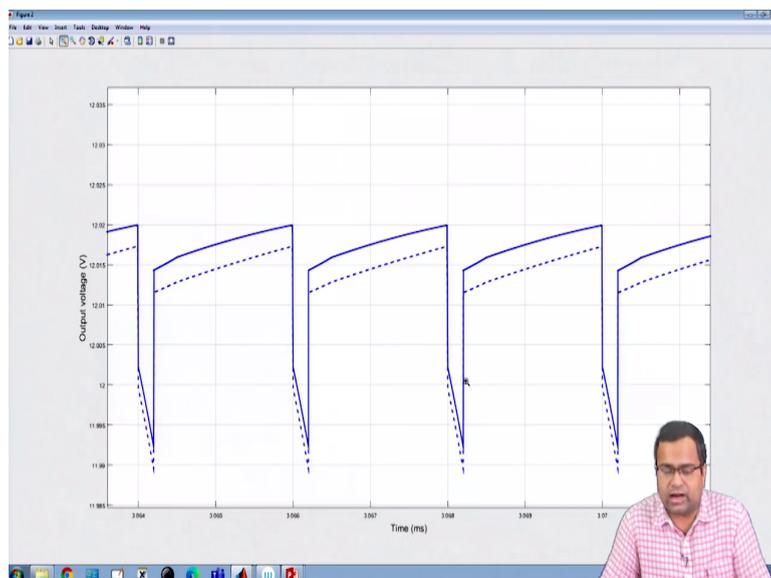
So, even if we reduce the inductance value, the stability property will also increase because we have increased the inductor which became. So, now, if we reduce and if we use a dotted line curve now and we want to run the simulation again.

So, now, there are three traces ok. This is also a closed loop, but now with a smaller inductor which is you know which should provide more stability because open loop was stable with 20 Microhenry inductor. And now we want to do the closed loop and we want to see that all three waveform together ok.

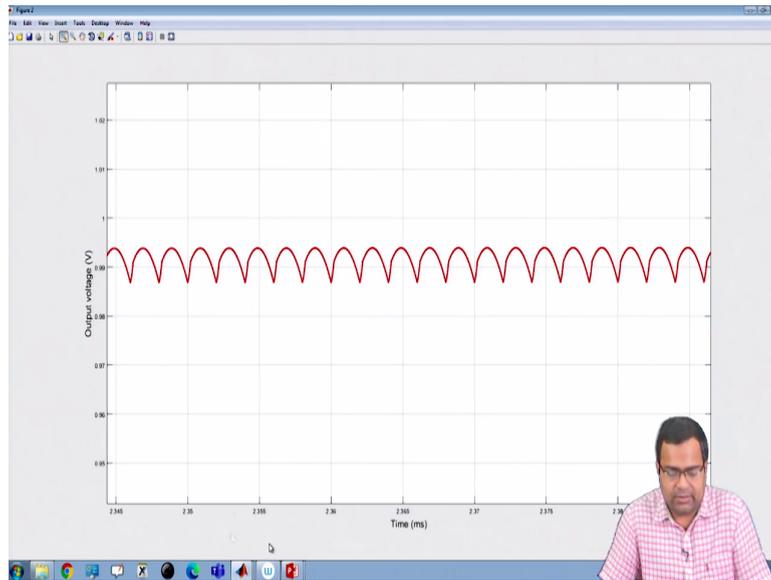
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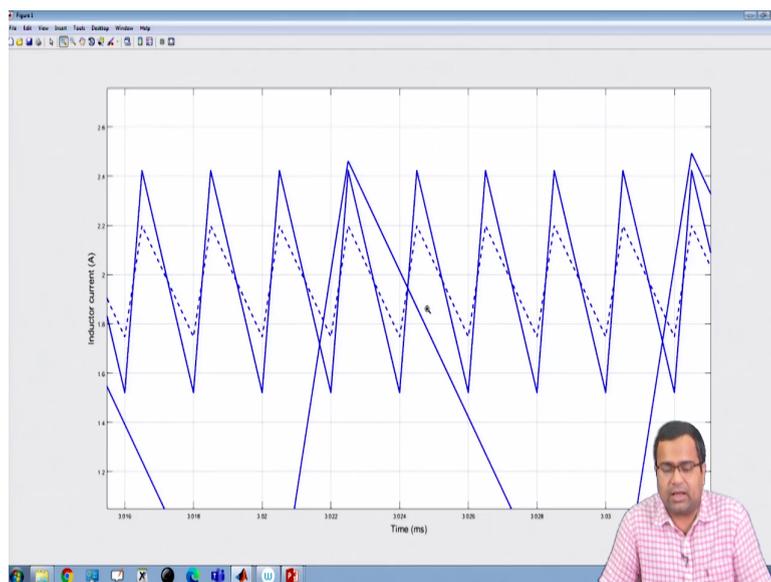
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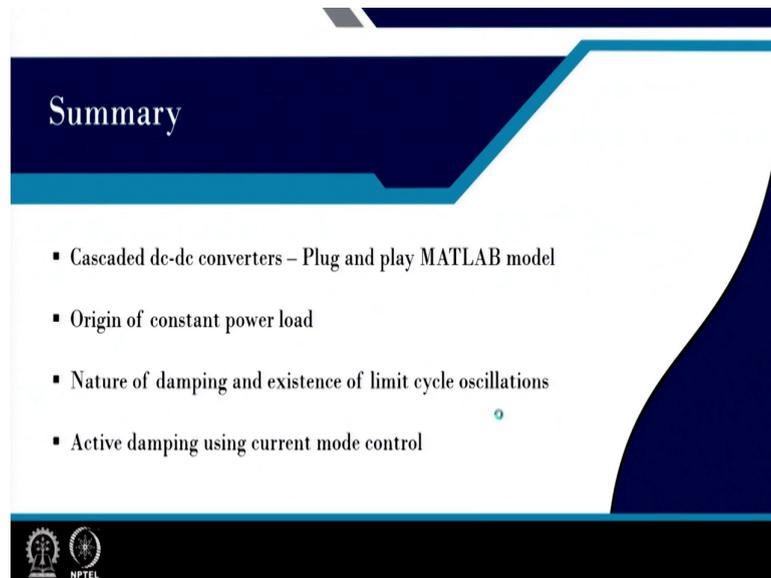
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So, you can see that it is perfectly stable. Both are again overlap, perfectly stable and currents are also stable. That means, yeah, the current ripple has increased because we have reduced the inductor value. So; that means, now we conclude that so both the converters are running in you know stable periodic behavior ok.

So; that means, we can provide active damping by means of this closed loop control by current mode control. So, current mode control provides active damping and that actually stabilizes the whole system.

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So, in summary we have discussed cascaded DC-DC converter. We have used our plug and play MATLAB model to create cascaded converter from our individual DC-DC converter. We have also discussed origin of constant power load and we have also discussed the nature of damping and also existence of limit cycle oscillation whether it is an unstable open loop system that also we have discussed and some possibility of limit cycle oscillation also we have discussed.

And we have also discussed that the damping active damping by current mode control can be used to stabilize the overall system ok. So, with this we want to finish here.

Thank you very much.