Digital Electronic Circuits
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Lecture - 38
Application of Shift Register

Hello everybody. We have been discussing Shift Register. In this class we shall consider certain Applications of Shift Register.

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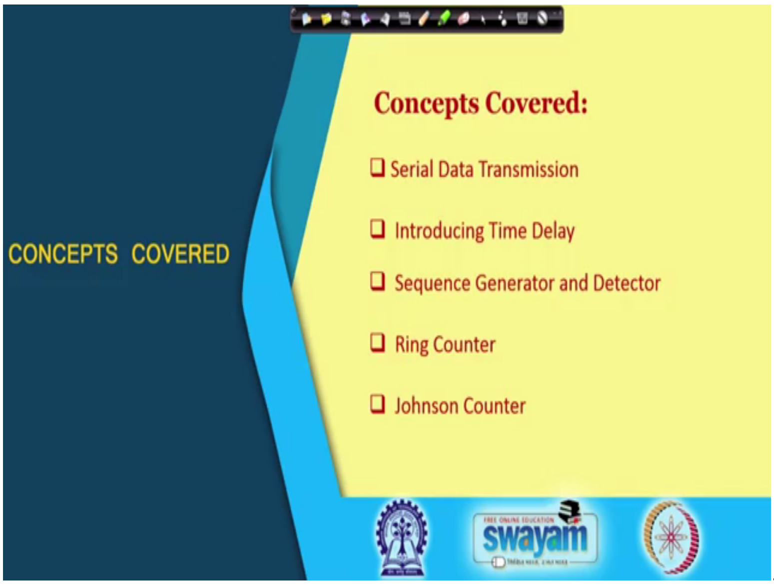

So, these are the few things that we shall have a look.

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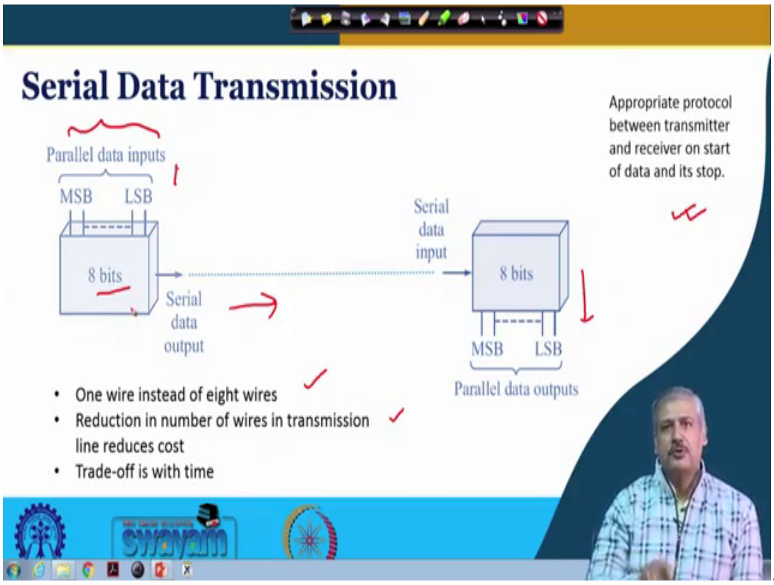

So, the first of all what we see is as one application of shift register is parallel to serial conversion that we do through shift register that can be used for converting a parallel stream of data that is getting generated. For example, in some process say 8 bit data is generated, samples are generated which is coded encoded by 8 bits. So, that is generated one sample means 8 bits are getting generated and it needs to be translated to some other place.

So, one option is to have 8 transmission channels ok, so that at the other side those 8 bits will be appropriately collected, but having those 8 wires or 8 channels is a bit costly and if the data rate with which this is generated is such that we can make a parallel to serial conversion and quickly we can at a higher rate, we can send it to the other side and there we can collect it and convert through a serial to parallel conversion serial input to parallel output that kind of a shift register. Then we have a this data 8 bit data appropriately received at the other side.

So, this is one thing that can reduce the cost of transmission by converting parallel data to serial and having a serial communication between transmitter and receiver and of course, which need to have an appropriate protocol to find out start of the data message or the information and this top of it, so that next 8 bits again appropriately be picked up, ok. So, the issue here is trade off is with the time that the rate with which you generate and the rate with which you transfer with which you transfer is transfer rate need to be as many times more depending on number bits that is getting to converted clear. So, this is one thing that you can see on reduction of cost. So, parallel to serial and then, serially it is pushed out through a shift register.

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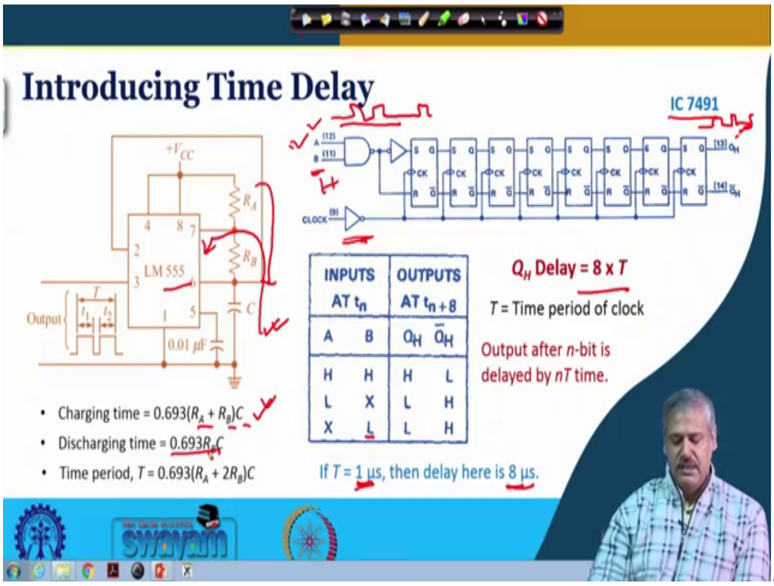

Next we can use shift register to introduce time delay and the input data stream somewhere here IC 7491. We have already seen this is AB is the control input, ok. When we are keeping it at high, then whatever is the input at A, right.

So, at that time sorry when B is at low whatever is been put at A, we have to go by this truth table. So, whatever is the input at that is getting transferred to the output after 8 clock delay, right. So, that is IC 749. We can have 4 bit shift register then it will be after 4 clock delay. So, the same variation that you see over here, so that will also be available here. Is not it right and this clock the clock time period multiplied by number of flip flop units that is there in the shift register will be giving you the total delay between this input and output and that will give you the time by which the binary data stream is getting delayed, ok. So, if the clock is of time period is of 1 microsecond duration, then by this arrangement we will get 8 microsecond. If there are 4 shift registers 4 flip flops in the shift register, it will be 4 microsecond.

So, if the clock time period is 2 microsecond, in this case it will be 16 microsecond delay. Is it clear? So, how you can you know having clock generated which is of different time period? One convenient option is that of using IC 555, ok. Suitable triple five time timer is very much used and this is A in a stable multi vibrator more in which are RA and RB through RA and RB this capacitor gets charged for which the charging time is 0.693 multiplied with RA plus RB. This is resistance values and capacitance and for discharge happens like this. So, discharging time is 0.693 multiplied by RB into C. So, total time period is like this.

So, with appropriate choice of R RA RB and C you can fix the T value time period and accordingly the delay can be introduced clear, right. So, next we will look at application of a shift register in sequence generation, ok.

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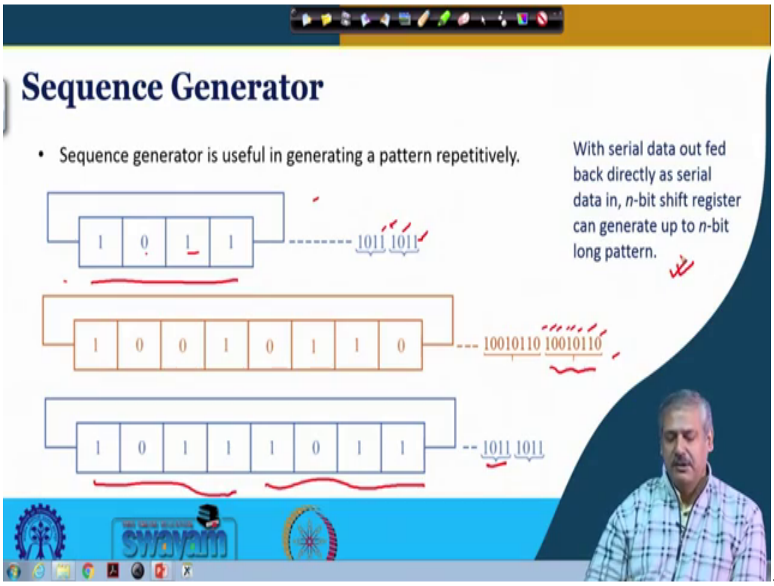

So, here we are thinking about we are that a particular sequence will be generated repetitively ok. So, there could be an application where we are looking at a particular pattern coming say 3 times or 4 times which cannot be random. So, basically that serves as a pilot or a header or something else to follow, ok. In a random message somewhere a pattern like a particular pattern may come, but it is getting repeated number of times it is unlikely, it is unlikely ok.

So, that could indicate that certain events are to follow or just after that, ok. So, there could be other applications as well for a sequence getting generated repetitively. So, for that we can think of a shift register and a shift register like a 4 bit shift register over here. See it is loaded with 1 0 1 1, initially and after the output of it is feedback to the input of it the way you see here and if you now clock it, then what will happen this one will go out right. This one is going out and after that this one will come out and this one is giving feedback feed here after that 0 will come out and after again another clock 1 will come here. So, another clock. So, this one will come up. So, this is the way it will keep circulating and this pattern 1 1 0 1 will keep getting generated. Is it?.

Instead of 4 bit if you have got a 8 bit shift register and say we have loaded it with 1 0 0 1 0 0 1 0 0, right. So, again the output of it is feed back as input of this one. So, 0 1 1 0 1 0 0 1 it will it is getting generated. So, one cycle is getting completed. So, other one will the next cycle will start with another 0 at this particular pattern will get repeated ok. So, a 4 bit you can get 4 bit pattern, 8 bit 8 bit pattern ok, but if you say in some case you are loading it with say 1 0 1 1 again 1 0 1 1. So, what will happen of course 1 0 1 1 will come in one cycle of 8 twice. So, basically you are generating a 4 bit pattern, ok. So, if you appropriately load it, then you can get n bit pattern out of n bit shift register. The way we have configured it is fine. So, that is what has been mentioned over here.

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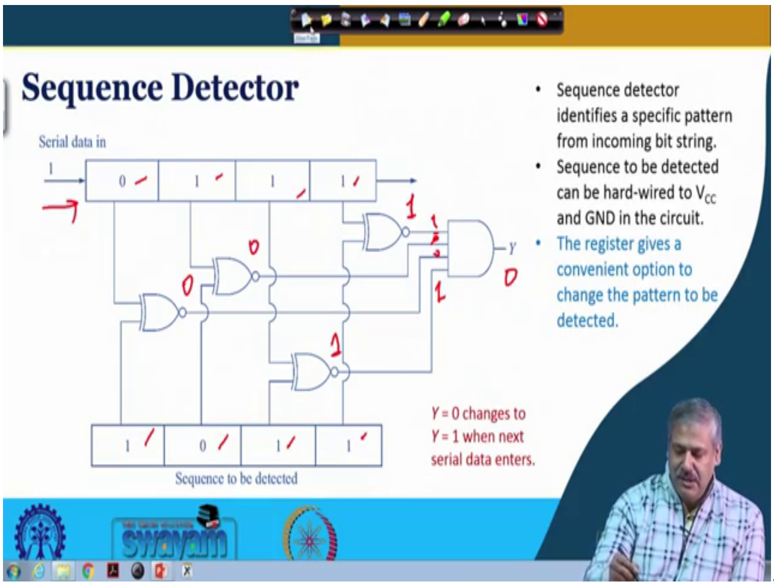

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Now, comes sequence detection. There also shift register can be useful, ok. So, by a sequence detection what we what we mean is that identifying a specific pattern from the incoming bit stream, ok. So, here this is the serial data in the bit still it is coming, and which is made to go through a shift register and this shift register is used for the pattern matching sequence detection, and the sequence to be detected we can store it in another register, right. So, for example if we want to detect a pattern in the incoming stream 1 0 1

1 we can store it over here in a register, otherwise we can connect it to V cc for 0. You can connect it to ground 1 again to V cc and one to ground. So, that is hardwired ok, but if you want to change the pattern that we want to detect, then again we have to physically disconnect and connect this V cc and ground alternative is to use a register like this. We can load the register with another a 4 bit number which will be detected for a different operation so required.

So, that is the advantage of having a register in place of hardwiring the bit values that we want to detect and here what is happening. So, look at a particular case. The outputs of this bits that are to be detected they are made to go through x nor gate each of these are going through x nor gate x nor gate you know if at the output indicates a equality of the input. So, if 0 0 and 1 1, then the output will be 1 x or if 0 1 and 1 0 the output will be 1. So, x nor is just opposite of it. So, when the input is 0 0 and 1 1, then the output will be 1. So, that means it is actually given the logic for equality equal whether it is 0 0 or 1 1. In either case the output will be 1 and all 4 bits when they are equal these and gates output will be 1 indicating a match or detection of the specific sequence.

So, the example in this example at this point of time 1 0 1 1 is to be compared and we have got 0 1 1 1 in the incoming stream which is stored in this shift register, ok. So, what we see 1 and 1 this one and this one it is compared. So, it is generating 1, this and one compared. So, this is generating one. Now this1 and this 0 will give you 0, this 0 and this 1 it will give you 0. So, these and gate 1 ok, then this is 1, this is 2 or 0. So, the output is 0.

Next what happens this one gets c, ok. So, what will be the modified values of this shit register because it is getting shifted as whole to the right.

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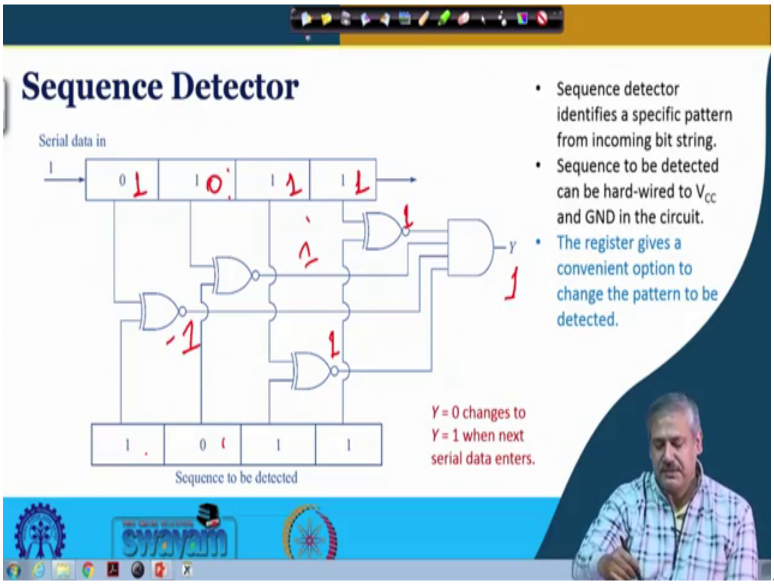

So, now this is 1, this is 0 this is 1 and this is 1 is not it 2. So, all these now x nor gate having same you know equal values 1 1 here. This 0 0 over here 1 1 over here. So, all of them will give you an output which is 1 and the and the and gate output will be 1. So, that is this sequence is detected. So, that is you a we can make use of this shift register, get where the incoming this bit stream will pass through a shift register.

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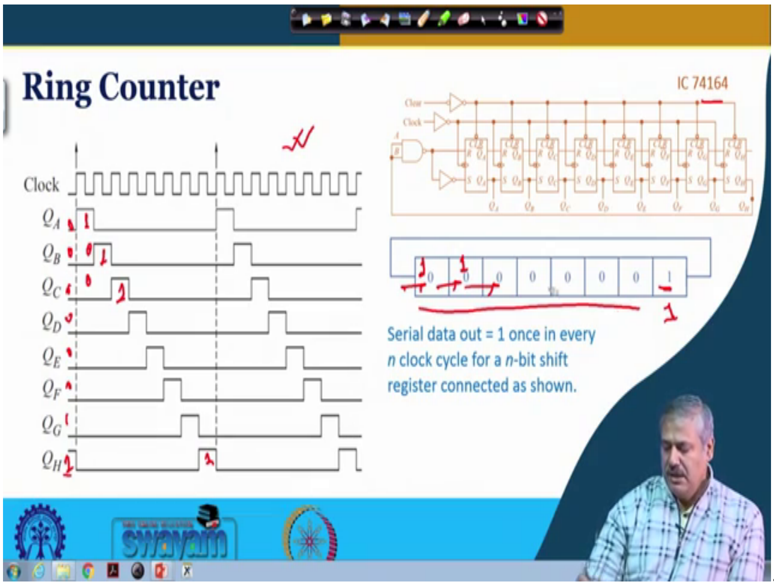

Next we can see use of shift register what is the called getting ring counter, ok. What is a counter? Counter keeps count of a particular event. In this case the clock trigger if this particular example ok, but it that event that trigger can come from some other place also. So, when it reaches a specific number, we say they count of something has taken place, ok. So, if we say counter which is giving a value modular value of 8, modular 8. So, it is counting 8 and when the count of 8 is completed, an output is triggered and output signal is made active. So, that is how the counter works. So, it keeps a count of the input that is triggering the circuit in certain manner and internally the state change takes place in such a manner that it gets incremented and when the count a specific count has been achieved, an output is activated. Is it clear? So, that is what we understand as a counter circuit more about counter we shall discuss next week.

So, when we talk about this shift register as a counter, so we are using the shift register again. You know in a feedback mode and in this case unlike this sequence generator where we are putting a specific sequence, we are putting in one example. All of them are zeros and only one value is 1, ok. So, this is how we are starting and then when so that when one. So, this is the case over here. So, this is 1 and all these values are 0 and then with one clock trigger. Clock trigger is getting now counted here as I said. So, what will happen this one will come over here. So, this is the 1 right and rest of the values will be 0. So, this pushed here, this 0 is pushed here and this 1 is getting in it is becoming 1. So, that is what you can see that rest of the values are 0 1, this is 0, this is 0, all of them are 0 and one more clock what will happen.

So, this one will come over here. That is what we know as shift register operation we have discussed in the previous classes, ok. So, next time it will this one will come here, right. Next time next clock this one will come here and after 8 clock you will see that this one is again appearing over here. Is not it. So, if you have connected an led or some output action and also from this point another time when it is getting it is getting a high input and say the led is glowing, then you under you have you have you can very well say that 8 clock trigger has taken place in between say count of 8 has been completed, clear and this can be achieved by any shift register with 8 such flip flop like 7 4 1 6 4 you can take and then, the feedback can be taken from that. You can achieve the way we are achieved a mod 8 counter.

So, in this case the flip flop output directly the last flip flop output the way we have seen it itself indicates the count of 8 has taken place, right.

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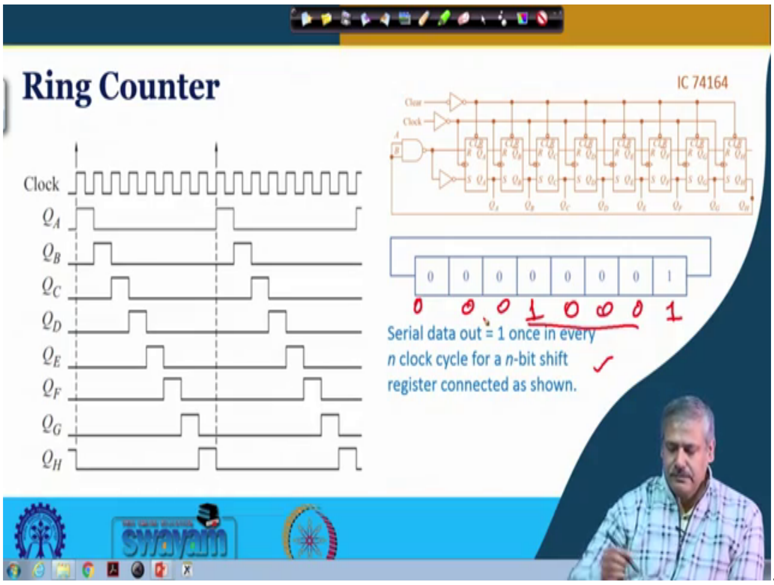

So, if we have instead of this one, right so 0 0 0 1 and 0 0 0 1 initially then what will be the account by this particular shift register. So, 1 is coming here, again 1 will come here after 4 clock pulses, right. So, it will be a mod 4 counter right, but with this ring counter arrangement as many number of flip flops if it is n bit shift register maximum, we can get a mod 8 mod n count, ok. So, that is what is mentioned ok, but we can get less you know depending on how we are initialising the flip flop, clear.

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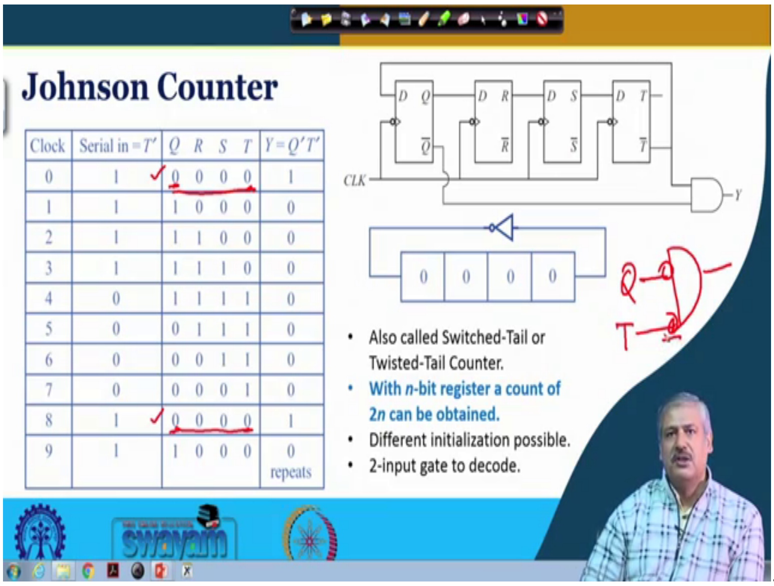

Next we look at another type of you know feedback by which what we get is called Johnson counter, ok. So, in Johnson counter this is the flip flop right and this is the shift register. So, the output of it is inverted and send as input to the first flip flop. Is it clear? So, serial data out is inverted and fade as input to the input of inputs serial in input. Now, if the arrangement is such that shift register is such that inverted output is available at the serial out a serial out, then you do not need this extra inverter. So, that inverted output you can feedback as serially.

So, this is the making of it because of which it is also called switched tail counter or twisted tail counter, right. Popular name is Johnson counter, but it is also called switched tail counter or twisted tail because tail is twisted when it is inverted that is that is the meaning of it.

Now, how this particular circuit works. So, if you initialise it with say 0 0 0 0 then it take this example. So, this T prime is getting feedback as an a serial in ok. So, 0 is coming here as 1, right. So, 1 will go as input and rest this 3 0 3 come here as this three 0s clear. So, now it is 0. So, what will be coming as input serial in is 1. So, this one is coming here and this one is getting in. So, this one and this two 0s will be becoming has two 0s still it is 0. What will be feedback is 1.

So, this one is coming here. So, three 1s, this is 0 again still it is T is 0. So, what is feedback is 1 T prime. So, this one is coming here and all three 1s it is following this three 1s. These three 1 is coming here as this three 1. So, four 1s have become after that wat will happen this one now feedback as one prime which is 0. So, 0 gets in this these are three 1s, then 0 0 gets in. These are two 1s, then 0 0 0 gets in. These are 1 and what makes this 1 we will come back. So, it is 0. So, all 0. So, this is all 0 means again it will get repeated. Is it fine?.

So, what we see in this case that we can we are getting the it is getting repeated. The sequence state is getting repeated after 8 clock pulses, ok. So, it can give a count of 8 clock pulses, right and this is this is a in that scenes with four search flip flop, 4 bit shift register we are getting a count of 8. So, modular number is 8. So, that is the Johnson counter providing you. So, with n bit shift register, it can be extended. So, if it is 5 bit shift register or 8 bit shift register, it will be 10 or 16. This count that can be achieved

OK. Now as I said we the external world tips to know that when that count of 8 or 10 or 16 has been completed, isn't it.

So, it is the internal states that are getting circulated that are getting repeated after 8 clock pulses as we have seen, but outside world need to know right for that it need to be what is called decoded and the states need to be decoded and made available to the outside world, ok. So, in ring counter we saw that no other external circuit is required. The output flip flop directly is made can be made available to the outside world and whenever it goes high the means count of 8 has taken place is not it, but in this case if you consider a similar scenario say T is 0 over here over here over here it is 1, but it is remaining 1 again. It will become 1 after 4 clock pulses. So, if you only take it from T, it is not going to work. Similarly form from S from R from Q if you try in none of the cases you can see that a modular count of 8 can be ensured, but what you can see what you can see right that if you take only say Q and T prime right Q prime and T prime.

That means both of them are 0. That is occurring again over here, right. In between in any of these states, it is not your 0 and 0, is not it. So, if you take a logic like this and then is this output, it will become 1. Once here again over here after a count 8 has taken place after 8 clock trigger has taken place. Is it clear ok? It is possible to have all these four that means, Q prim R prime S prime T prime right, but that will require a four input gate. So, that is a more complex circuit we are talking about the minimal requirement. So, earlier no external gate is required. Here we need a gate with that is two input a logical gate, and we can see other than this Q and T, a prime you can have other combination also.

So, for example this 1 0 ok. Q is 1 and R is 0. So, this is again occurring over here. So, once it occurs right, it will again occur after 8 clock pulses. So, that could also be a decoding logic. Is it clear? So, decoding logic for Johnson counter as you have seen in the case requires a two input logic gate. Now interestingly you can work out it is for 4 bit shift register, you can work out for 5 bit shift register, 8 bit shift register, any other and for Johnson counter you will see that every case what you would be requiring a only a two input logic gate more than that is not required, more than that is not required OK. With a two input logic gate, even 4 5 bit or 8 bit shift register work in Johnson count counter mode giving you modular 10 16 or whatever I mean depending on that number twice the shift register size a two input logic gate is sufficient for decoding, ok.

So, this is the way we can see that it works and you cannot think of other kind of initialisation also and we can see that it is it progresses in this manner, ok.

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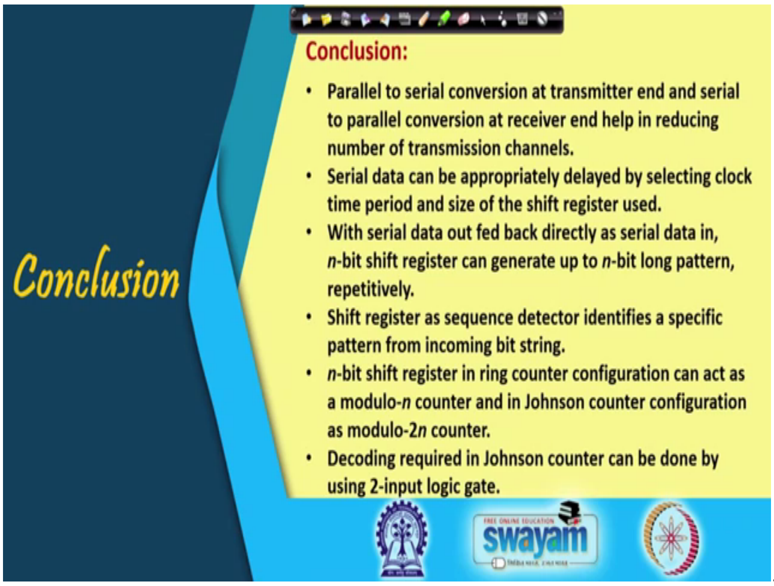

So, with this we come to the conclusion of this class. What we have seen is that parallel to serial conversion at transmitter end serial to parallel conversion at receiver end help in reducing number of transmission transmitter channels and shift register comes useful there because after parallel to serial conversion then the data is made serially out and their lies utility and you also. So, that single data can be appropriate appropriately delayed by section of clock period and also the size of the shift register used, Ok. If n bit shift register and T clock of t time period is used, then n T is this delay in this case with serial data out feedback directly a serial data in which shift register can generate n bit pattern repeatedly repetitively.

So, there you can use shift register as sequence generator and shift register can be used as sequence detector also to identify a specific pattern in the incoming bit stream where we are doing a bit by bit comparison, x nor gate is used and x nor gate outputs are to a multi input and gate and that and gate output is if when it goes high. That means, the pattern is detected and n bit shift register in ring counter configuration can act as a modular ring counter and in Johnson counter configuration as modular 2 n encounter and for ring counter configuration we do not need any decoding logic, extra decoding logic, but for Johnson counter we need 2 input logic gate for decoding purpose.

Thank you.