Course name- Analog VLSI Design (108104193)
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Okay, so now let us now, that we have figured out what P1 is, let us also figure out what P2 is and P2 is what? P2 is minus b over a, right? So, if I know what is b, what is a, so if we simply find, we simply plug that in, so what we will essentially get is and if we do some manipulation, some algebraic manipulation, so this is what we will get. In the denominator, we will get c2 plus cgd c1 by cgd plus c1. So, if I go back here, so what I am essentially doing is we recognize the fact that we have this term, we have this term divided by the a term, right? So, what we are essentially doing is we are dividing the numerator and the denominator by c1 plus cgd, okay? So if we divide the numerator and denominator by c1 plus cgd, we are going to get this thing in the denominator and in the numerator what we will get is gm5 times cgd by cgd plus c1 plus gds5 plus, what was it, gnot5 not gds, right, we are not using gnot, this is gnot5 plus gnot1 times c cgd plus c2 by cgd plus c1, right.

$$p_2 = -\frac{\frac{g_{m5} C_{gd}}{C_{gd}+C_1} + g_{o5} + g_{o1}\left(\frac{C_{gd}+C_2}{C_{gd}+C_1}\right)}{C_2 + \frac{C_{gd} C_1}{C_{gd}+C_1}}$$

So, again this seems to be a bit complicated, right, so we would like to make sense of it, right? So given the fact that we were focusing on gnot on the pole associated with vnot1, right, let us not use this, here we have gnot5 and c2 and this is co. So, the earlier pole that we were, that we were, the P1 was based on the pole time constant associated with that node vnot1, right? And when we were trying to figure out time constants, we can desensitize the inputs, if I desensitize the gm, so this goes off, this is no longer required and we, what we essentially said was the P1 node, the pole P1 associated with g1 was whatever we got.

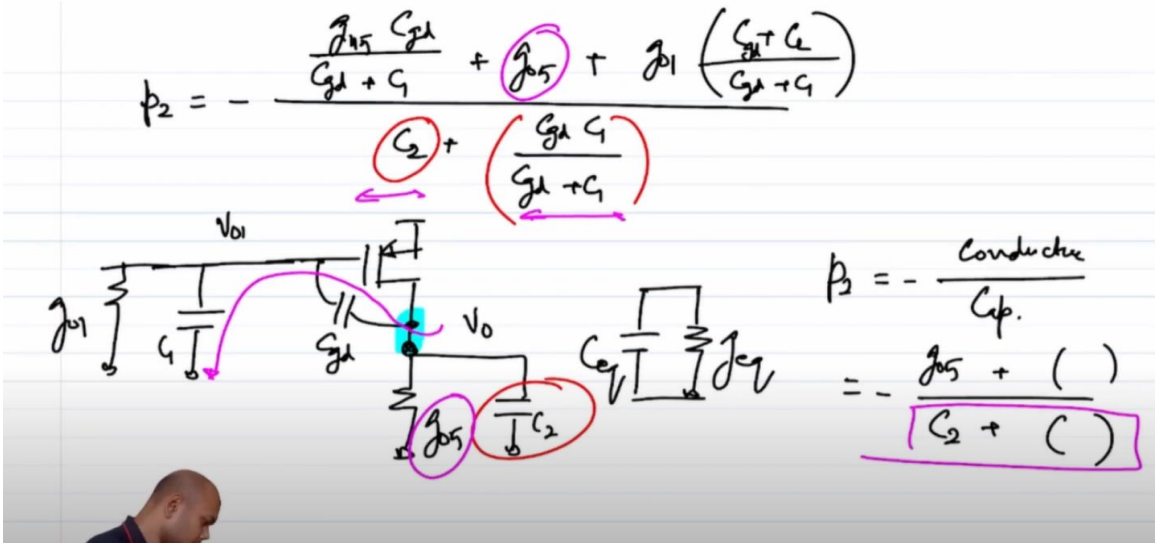
Now, what we are doing, what we are saying is that the pole P1 associated with, let us say this node vnot, ok. See the pole, if we are trying to figure out the pole associated with vnot,

what we will see, the P2 will be some conductance by some capacitance. Now, in the conductance term, what should I see, I should definitely see gnot5 and I should see some additional stuff. In the capacitance term, I should definitely see c2 and I should see some additional stuff, right? If I can express P2 in terms of some equivalent conductance, so essentially what we are trying to do is we are trying to see if we can express the conductance and capacitance associated with the node vnot to be of the, of some g-equivalent and some c equivalent, ok.

So, let us see if we can, if we can figure this, figure this out. So, what about, let us start with the easier one, let us start with c equivalent. So, what is c equivalent? C equivalent should be at least c2 should be there, which is here plus we have some additional term and what is this additional term? This seems like a series combination of cgd and c1, right? So, in this case, do you see any series combination of cgd and c1? Starting from vnot, do you see any series combination of cgd and c1? We can see, right? So, it looks like there is a series combination of cgd and c1 and that is what it, that appears in the denominator, right?

We have c2 and we have this, right? So, essentially the denominator makes sense, ok. But let us switch to the numerator. In numerator, I should have what? I should definitely have gnot5, gnot5 appears here. But what is the dominant term in the numerator? Whenever you have gm times something, then you have to take notice.

In this case, since all the capacitance we assumed are of the same order, then obviously that first term is should be the dominant term. And what is that first term? What does that first term remind you? It seems like, it seems like gm has been, the conductance of gm has been scaled by certain factor, right? And the factor is cgd by cgd plus c1. So, what does that remind you?



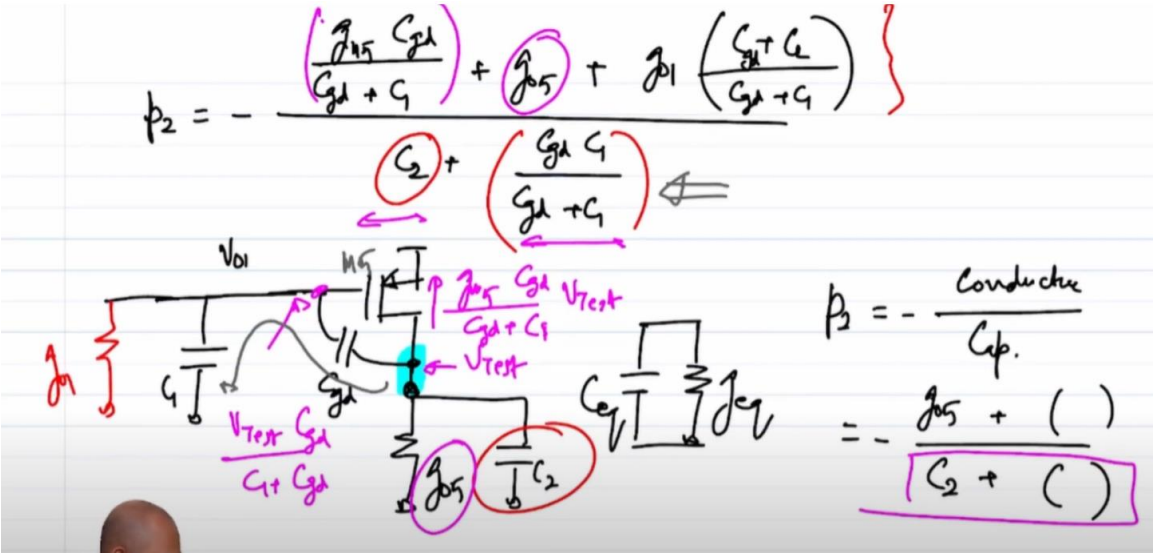
So, let us for the time being, let us ignore. So, let us ignore this gnot 1 for the time being, ok.

And let us try to figure out what is the impedance, what is the impedance of this node looking in, right? If I apply a Vtest here, right, if I apply a Vtest here, what voltage will come, will appear here? This voltage will be Vtest times cgd by c1, cgd, right. If that voltage appears here, what current will m5 draw? m5 will draw current of gm5 of that times that, right, cgd by ggd plus cgd plus c1 times Vtest. So, what will be the equivalent resistance or equivalent conductance? The equivalent conductance will be gm5 times cgd by cgd plus c1, right? So, that is what that appears here.

Essentially, the feedback around m5, the feedback around m5 is increasing the output conductance, right? You see that the feedback around m5 is increasing the output conductance and that makes sense, right? Because at higher frequencies, if P2 is supposed to be a high frequency pole, right, which was our initial assumption. If P2 is supposed to be a high frequency pole, then the conductance of cgd, cgd cannot be treated as an open circuit anymore, right? So, which essentially means that any excitation at the output node will, part of it will keep into the gate of m5 and it will excite the gate of m5 and in turn it will draw a current and that current will be in phase with the excitation, which means it is a resistive or a conductive, it is a conductance not a capacitance, right?

There will be a capacitance effect, the current through the capacitance will be there because of the c1 and cgd and that appears in the denominator, ok. Now, you might as well say why did not we take into account g01 and obviously g01, we should ideally take into account, but again this is an approximation. Because we did not take in this into account, so this P2 approximation that we are doing is not exact and because of that you get some extra term here, right. But fortunately that extra term is not dominant, so we can essentially

say that that is because of the so many approximations we are doing, but the key thing to notice is that we are getting, we are essentially getting a, we are essentially getting an intuition or a hang behind the locations of the of the poles, ok.



So, now if we assume that, if we assume that the dominant terms are gm5, right and dominant terms are c2 and cgd, c1 plus cgd all these things then what is P2 then, what does P2 become? P2 becomes gm5, cgd by cgd plus c1 that is the conductance and in the capacitance I get c2 plus series combination of cgd and c1, c1, right.

This is great, this is P2. So, what was P1 quickly? P1 was what? P1 was the conductance which was g1 and the capacitance, the capacitance was the amplified version of the cgd capacitance, right? So, that is 1 plus gm5 by gnot 5 times cgd. I am approximately, I am neglecting the other terms, I am only keeping the dominant terms into, in the picture, ok fine. But note that in our transfer function, we also have a, we also have a zero.

So, this is zero that we have been avoiding for a while, but what is the location of the zero? The location of the zero is that value of s for which the transfer function goes to zero, right. So, what value of, for what value of s, what is the root? Root of the numerator, the root of the numerator is s equal to gm5 by cgd. So, zero is plus gm5 by cgd. Note that this is a positive half, this is a positive, this is a right half plane zero, not a left half plane zero, right, ok great. So, now let us see in the presence of cgd in the, or rather let us see what is the effect of the poles and zeros in the presence and absence of cgd, right.

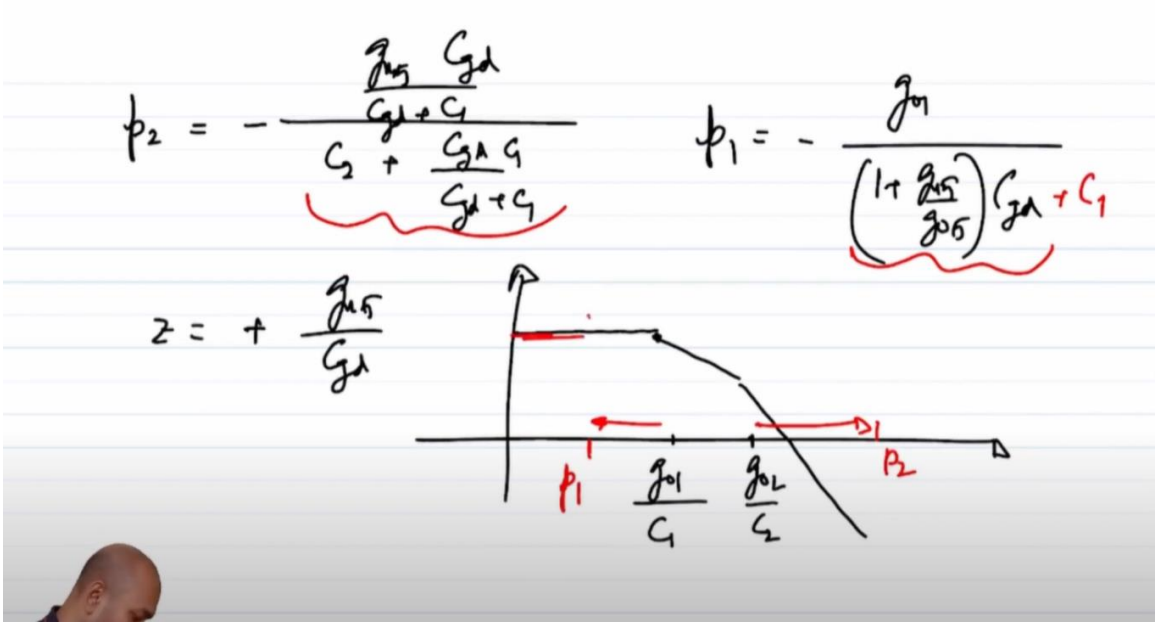
In the absence of cgd what was the pole P1? P1 was at gnot 1 by c 1 and P2 was at gnot 2 by c2. Approximately if they are of similar order they are close by, right? So, these are in

absence of cgd, right? So, if we did not consider cgd so which means that the pole locations would have been something like, something like I mean the transfer function would have been something like this. But in the presence of cgd, right, in the presence of cgd we see that these approximations I mean these locations are and not only presence of cgd, in the presence of a significant amount of cgd.

I mean cgd can be there, but can be very insignificant, but not there. In the presence of cgd and cgd becomes significant, see if cgd becomes comparable to P1, right. So, in the presence of cgd where is P1? P1 goes from gnot 1 over c 1 to gnot 1 by I mean there is obviously plus c1 term here. So, this moves to the lower frequency, this moves further to the lower frequency, right? So, it goes somewhere here, right?

So, it goes somewhere here. So, this becomes a P1 in the presence of cgd. What happens to P2? A very interesting thing happens to P2. The new denominator of the P2 more or less remain same, right. Maybe the denominator is increased from c2 plus something, but what has happened to the numerator? The numerator is now a function of gm 5, right?

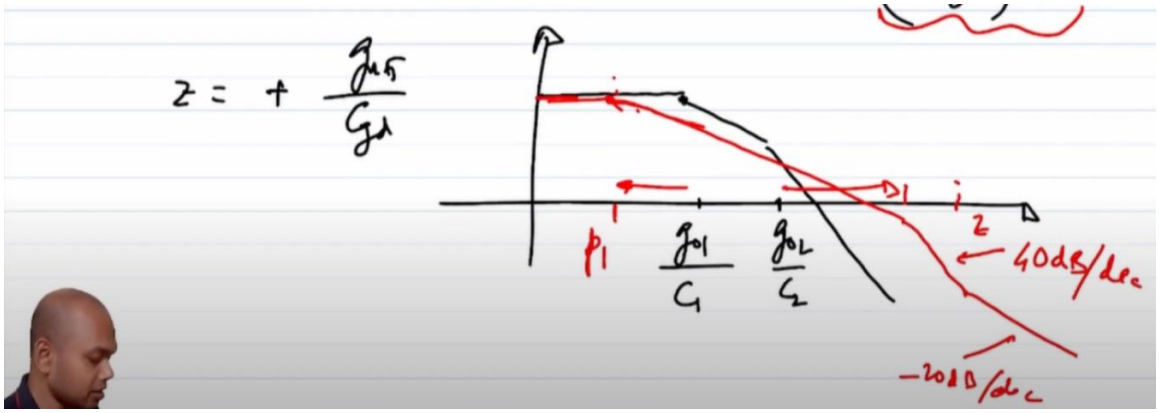
And if cgd and c 1 are of the same order the numerator is approximately gm 5 from alpha times gm 5. Earlier the numerator was gnot 2 which means that what P2 has shifted to the higher frequency. See the poles splitting is happening automatically, right. So, we do not have to do much suppose by the virtue of cgd the poles splitting has taken place automatically, right?



So, your P2 has come here. So, which means that our transfer function, new transfer function will be the DC gain does not really change the new transfer function becomes a

new, yeah. So, new transfer function becomes something like this, ok, alright. But now what about now that we have a 0 what about the 0 why do you think is the location of the 0? Again if cgd, c1 and everything are of the same order so clearly 0 is at a higher frequency than P2. So, we will probably have a 0 somewhere here and when you hit a 0 what happens to the slope? So, this is sorry, I should sketch it properly. The slope gets restored back to 20 dB per decade, right.

This is minus 40 this is minus 20 dB per decade, ok. So, good things are the poles splitting happens naturally. If the poles splitting does not happen naturally you can put an additional capacitance, you can put an additional additional this is called the Miller capacitance you can put an additional Miller capacitance to split the poles, right. And but the bad thing is that we have a zero. Why is it a bad thing?



By the way is it a good or a bad thing? Is it a good or a bad thing? It is bad thing because it is a right hand side zero and if it is a right hand side zero what will be the phase at UGB? So, the angle at omega u will be what will be the angle due to P1? The angle due to P1 will be minus tan inverse omega u by P1 which is approximately minus pi by 2, right.

Because P1 is anyway much lesser than omega naught omega u then you will have minus tan inverse P2 by sorry omega u by P2. This is good because in the sense that P2 has moved to a higher frequency than before. So, this is even better. But now we have a right-hand side zero inside a right-hand side zero this gives me an excess phase lag, right? This gives me an excess phase lag of tan inverse omega u by C.

So, this gives an excess phase lag which means this degrades the phase margin, ok. So, what I would like ideally expect is to move this zero to as high a frequency as possible. But you see that in order to do that I have to increase gm5, right. It is good if I can increase gm5 it can also move P2 away. But increasing gm5 comes at a cost of more power because you have to burn lot of power you have to burn excess power at the output.

So, that is why people try to I mean people have tried to find out architectures where we

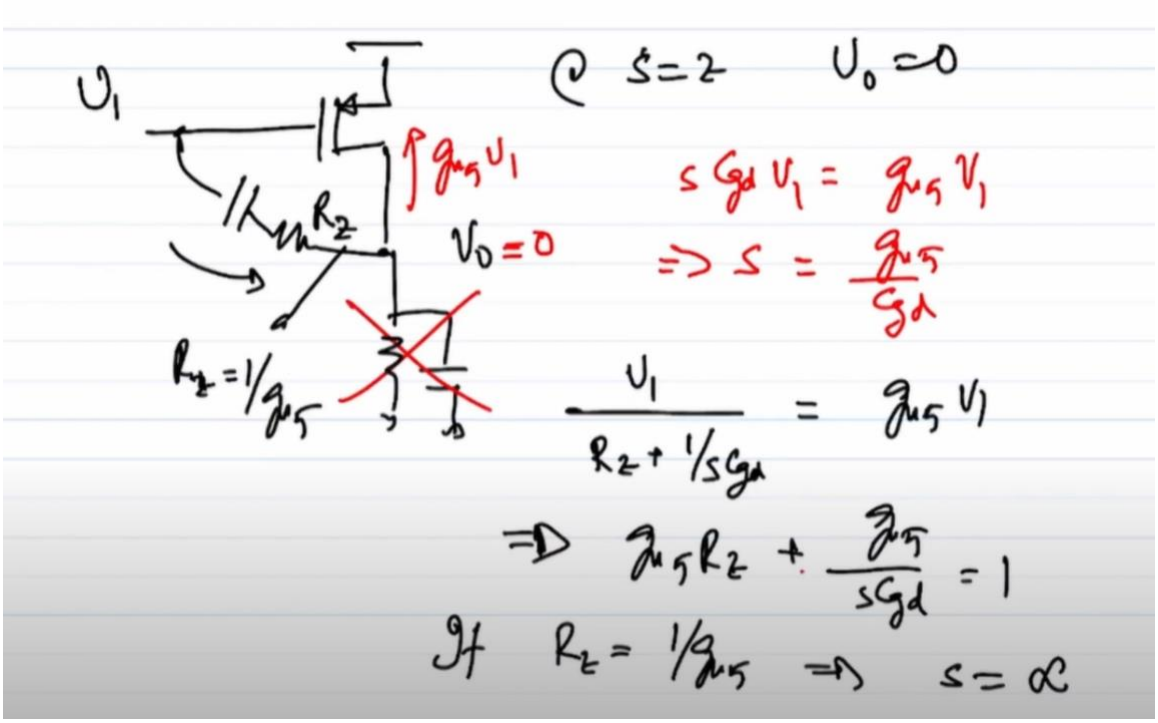
can probably not use extra power and let us see if we can cancel this right hand side zero, right. So, how do we cancel right hand side zero? So, by the way what is the genesis of a zero? The genesis of a zero is the fact that what is a zero? zero is a root of root of the transfer function, right, where the transfer function goes to zero. So, in other words in other words so, if I sketch this we find out we have bunch of stuff connected here, right. This is V0, this is V1. So, at zero, right, at s equal to z V0 has to go to zero, right that is by definition, right.

So, if V0 goes to zero, right, if V0 goes to 0 I do not have to bother about this stuff connected here, right. So, this is equal to 0, if this is equal to 0 what is this current? This current is gm5 times sorry this current is cgd s cgd times V1, right? Where will this current flow? This current will flow through the m5 transistor. What is the current flow through the m5 transistor? This is gm5 times V1. So, the location of the zero is essentially the, if you solve for KCL at V0 the value of s that you get is the location of the 0.

So, s cgd times V1 becomes gm5 times V1 which means s is gm5 by cgd. This becomes a location of the zero, right. So, by intuition you can figure out the location of the zero by simply by setting the output to 0 and solving for KCL and KVL. So, whatever solution of s that you get will be the location of the zero, right. So, now what we are looking for is to ensure that the zero vanishes.

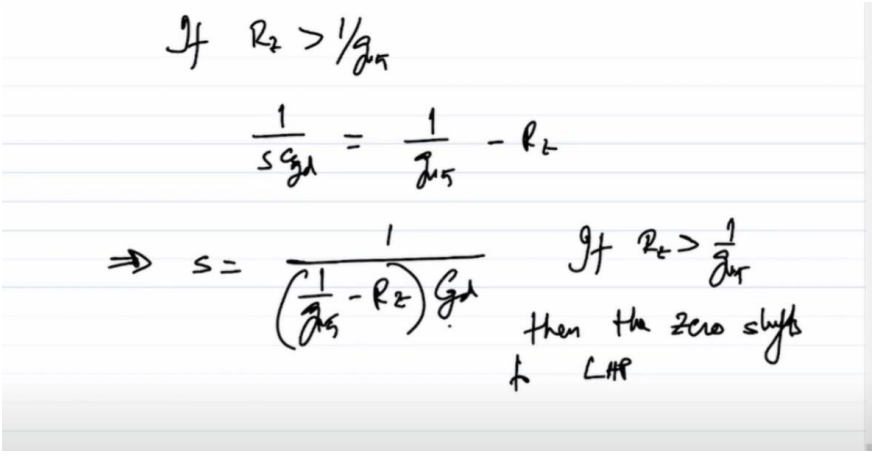
It can be shown that if you just, if you I will not get into the derivation of it, but if you if we put a let us say a resistance here, let us say put a resistance R here, let us call it Rz, this is cgd, right. So, what if I use the same condition what will I get? What is the current through, what is the current through this branch? This current through this branch is V1 at

the 0

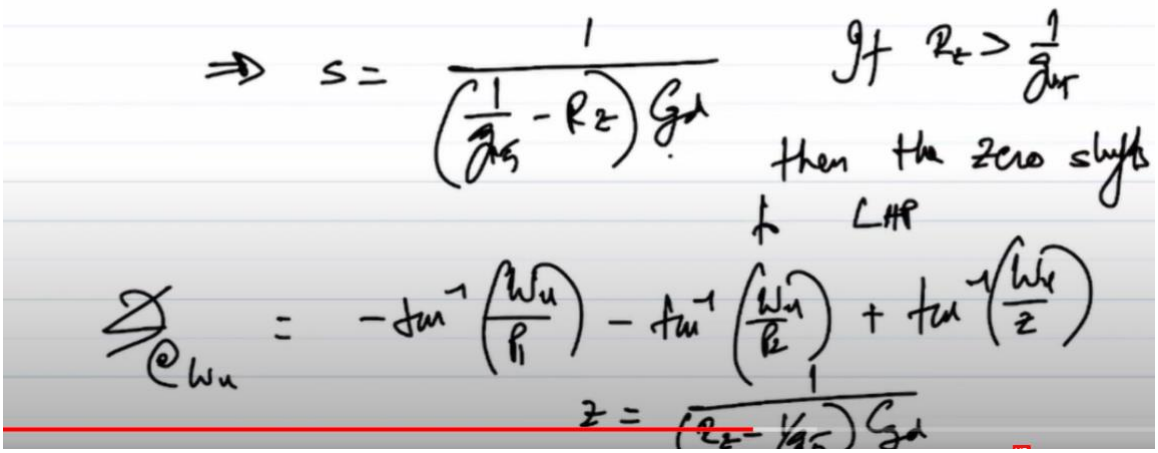


frequency the current through this branch will be V1 plus Rz plus 1 by s cgd. This should be equal to gm5 V1 which essentially means that gm5 Rz plus gm5 by s cgd is equal to 1. So, if Rz equal to 1 by gm5 then the solution is s equal to infinity, right. So, in other words, if Rz is becomes exactly equal to 1 over gm5 then the right hand side zero vanishes, right.

In fact, we can do even one better the right hand side zero causes a phase lag, but left hand side zero causes a phase lead, right. So, if we make Rz to be greater than gm5, right, if Rz is greater than 1 by gm5 then what is the location of the zero? Then we see that basically solve that above equation. So, we get 1 over s cgd becomes 1 over gm5 minus Rz. So, this becomes s is equal to 1 over 1 by gm5 minus Rz times cgd, right. And if Rz is greater than 1 over gm5 then the 0, right zero shifts to left half plane, right .



So, on the left half plane zero instead of giving a phase lag gives us a phase lead which means which means what? Which means whatever you see here this is minus tan inverse omega u by z terms that in this case this will become plus tan inverse omega u by z where I am talking about mod of z obviously in this case. So, your phase the total phase lag will be so angle at omega u will be minus tan inverse omega u by P1 minus tan inverse omega u by P2 plus tan inverse omega u by z where of course z in this case is 1 by Rz minus 1 by gm5 times cgd, right.

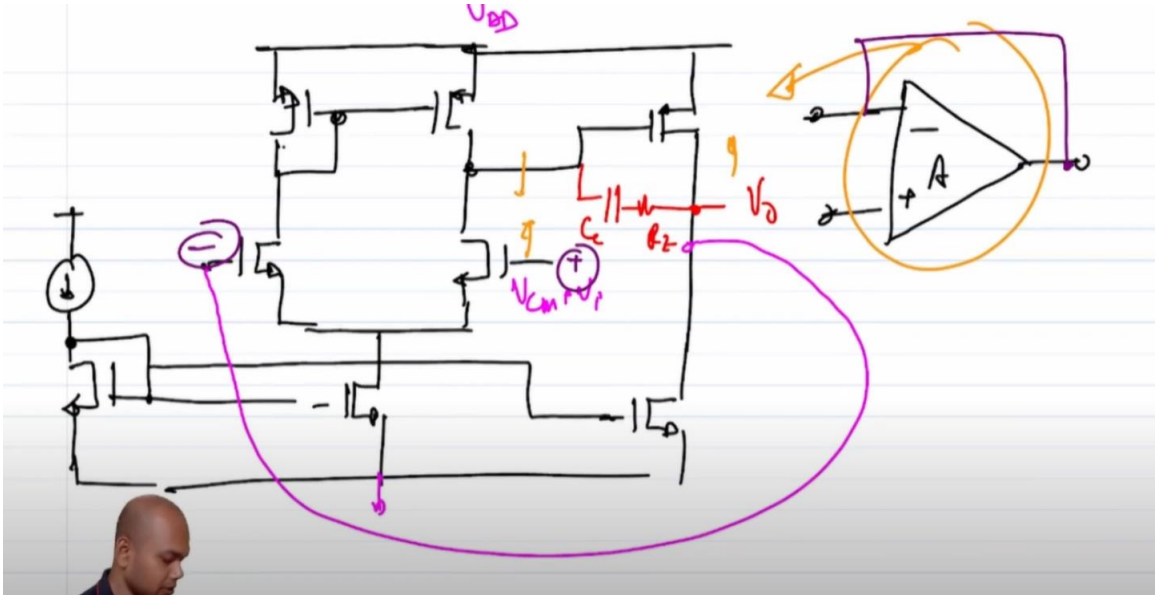


So, very often that is why this trick is often played in order to improve the phase margin, right. So, in a nutshell what does the total final architecture look like? The final architecture of our two-stage operational amplifier is the following. So, maybe we have a current source here which was mirroring our transistor which was current mirroring, right.

So, we had this and then we have a cgd capacitance but instead of cgd if we have to put an additional capacitance we can put the additional capacitance let us call this cc. If the cgd capacitance is small we can put an additional capacitance cc and put a Rz here and this becomes the V0 and if we have to close the loop all we have to do is connect this guy to V0 and this can be Vcm plus Vi, this becomes V0, right. So, note that this is the if we go back to the first lecture in the introductory lecture and if you see that schematic of the op-amp that we promised, right. So, this is the schematic of the op-amp that this is the schematic of the two-stage op-amp that was the motto for this course, right. And more popularly this is often when we say that we have a op-amp of sin minus plus a what we generally mean is this is this structure, ok, where the plus terminal is which one in this case.

How do you know what is plus terminal? That the input terminal which if I raise that voltage the output should increase. So, if I raise this voltage this voltage decreases. So, this voltage increases essentially this becomes a plus terminal, this becomes a plus terminal,

and this becomes the minus terminal, right. So, when you connect anything in negative feedback you essentially connect it like this, right.



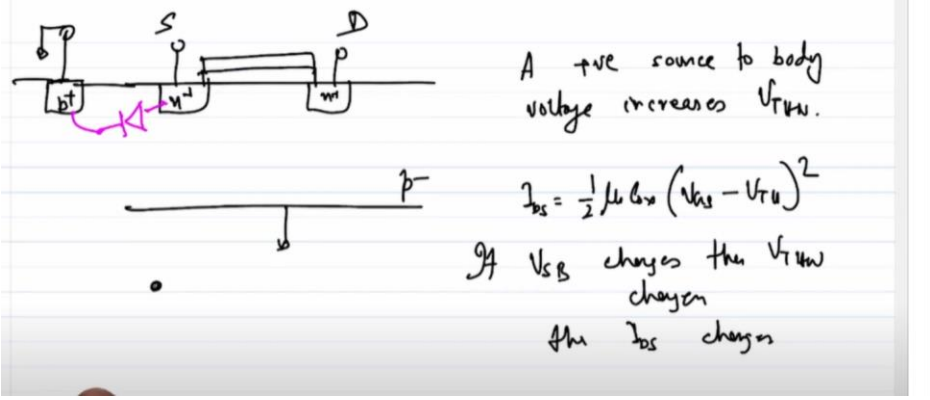
So, this is the equivalence of this of these two. Of these two structures, ok. So, essentially we have kind of come to the end of the course, but before I wrap up there is one thing that we did not touch upon at all. I will be amazed if I do not refer to it, we will not be using it in this course because I mean we essentially ran out of time, but we should at least know about this effect and that effect is often called as body effect, right. So, what is a body effect? As we saw that our transistor is biased on a substrate, right, is biased on a substrate or it is built on a substrate and it is not necessary that the drain, the source and the body terminals will be always, will always be shorted, right. It is not necessary because if you have a cascode transistor as you can see the source is at a higher voltage than ground, but our body is always rounded, right, our body is always rounded, E minus this is always rounded, ok.

So, since this is always rounded there is a difference in voltage between the body and the source which means that there is a reverse bias, this is the reverse bias PN junction that has that, this is the reverse bias PN junction along with the drain side you have a reverse bias PN junction on the source side which we have kind of neglected, right. What is the effect of this? The effect of this that there will be a depletion region around the source and overall the effect of this will be it will increase the, it will change the threshold voltage, right. So, this changes threshold voltage, right. So, higher source to a positive source to body voltage increases Vth. So, if it changes threshold voltage then obviously the transistor parameters change, but fortunately it does not change the threshold voltage significantly, right.

It is only a small fraction of threshold voltage it changes. So, that is why we kind of

neglected it throughout the course. However, anything that changes threshold voltage can also affect our incremental model, right. So, because our threshold voltage is a, our current your Ids is half mu n Cox Vgs minus Vth whole squared. Now, if the threshold voltage, if the source voltage changes with the signal, right.

So, if Vs changes then Vthn changes then Ids changes, right. Which means that, which means that or rather in this case if not Vs, if Vsb changes this voltage between source and body changes, which means that their current, there should in the incremental model there should be a, there should be a term of something times Vsb, right.

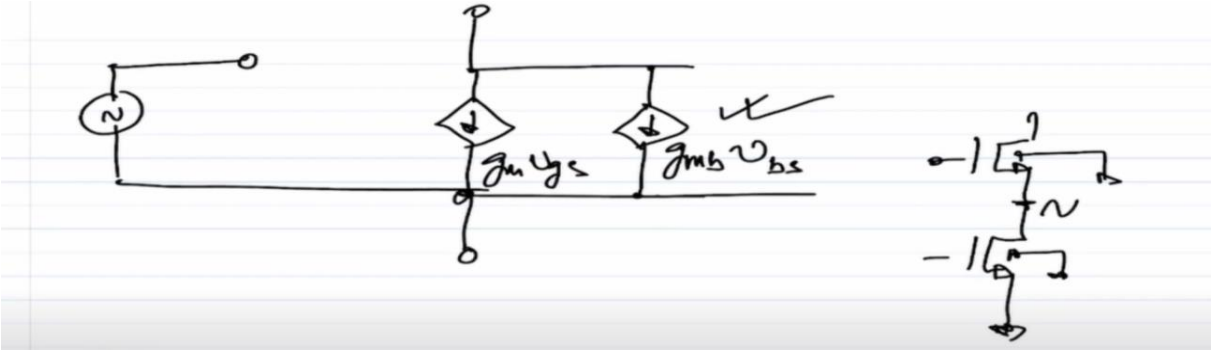


So, that is what is also used and you will see the literature in some cases where, where on top of GMVgs you also have a additional current source, this is called GMVvs, ok. So, our transistor model remains whatever it was, but on top of that we have a, we have an additional, additional current source. But note that if the source is always rounded or if the source does not move, right, then Vgs is essentially 0.

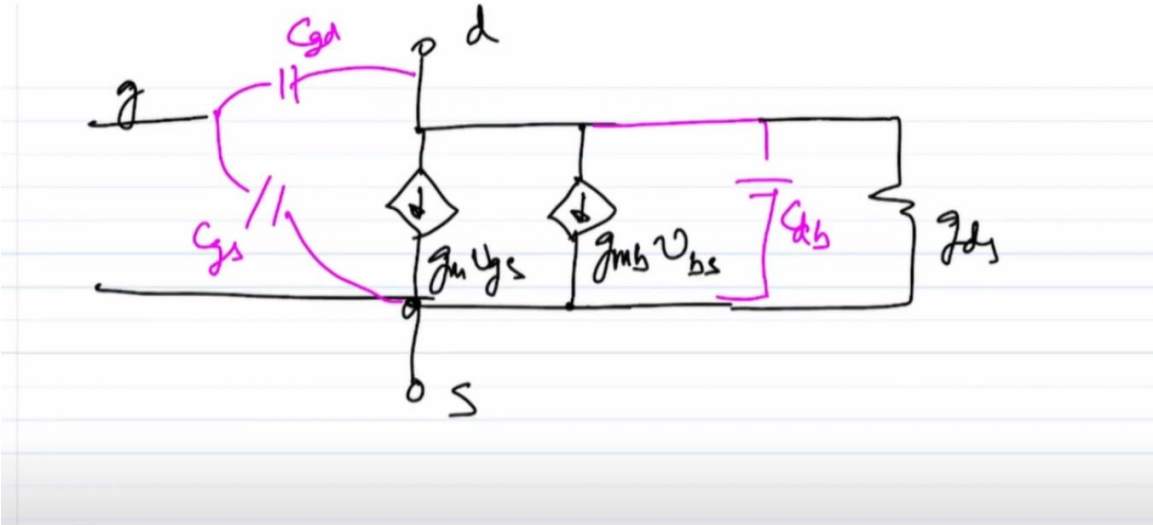
For example, in a common source amplifier, in a common source amplifier the source is fixed. So, the body is also fixed. So, the, this, this does not come into picture, right. But again in let us say a cascode transistor, if you have a cascode transistor, if you have a cascode transistor then the source is moving, but the body is grounded, which means this will come into picture, right. So, it is a minor adjustment of the small signal model that you should keep in mind.

In this course we will not be using, we will not solve any problems using body effect, but this is something that you should keep in mind when you do, when you are doing design because your small signal parameters can change slightly because of, because of this,

because of the body effect, right.



So, if we include body effect, what is the, what is the final structure of the MOSFET that we ended up with? So, the final structure of the MOSFET now becomes, we have a capacitance dG s, we have a capacitance dG d, we have a capacitance dD d, then we have a G d s, right. So, this becomes a drain, I do not need to use this because we are doing only the MOSFET model, this becomes a gate and this becomes the source, right. So, this is the, this is kind of a rudimentary transistor model that we often deal with, but now that we have gone through the entire course, we would know that, we know that it is not necessary that all the components need to be in place while doing our analysis. For example, if you are doing DC analysis, we can forget about the capacitances, right.



So, if we are doing, if we know that, if we know that the source is rounded, for example, then the CGS capacitance goes to ground and it only loads the previous stage, right, it gets clubbed into the previous stage. Similarly, CDP gets clubbed into the next stage capacitance, right? So, we can play around, we can play around this, we can play around with these models and we can make simplifying assumptions as we proceed, right? Okay, so, yeah, so with that, it is time to wrap up the course. I mean, I hope that we all learned something in this process, I hope you found this course valuable, right?

So, if there are any questions, please feel free to post your queries in the forum and we would be happy to, be happy to answer them. My name is Imon Mondal, as you must know, as you might know right now and it is time to sign off. Thank you. Thank you.