**Course name- Analog VLSI Design (108104193)**
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**Week- 12**
**Lecture- 35, Module-1**

Welcome back, this is lecture 35. So, up until now we have been discussing different topologies of amplifiers using single transistors, multiple transistors, then we graduate it to differential amplifiers. We saw multiple topologies of differential amplifiers also and we now know that we the reason we are doing all these things is because we have to put things in negative feedback right. So, before we proceed with the consequences of putting things in negative feedback, let us focus on something that we have been avoiding till now. So, if you might have noticed that we kind of have avoided the capacitances associated with the MOSFET right. The way the reason I am saying we have avoided the capacitance with associated with the MOSFET because we have treated the MOSFET as a as a voltage control current source right with some resistance at the output that was the basic treatment of the MOSFET.

Yes, we had put capacitors at different places in order to couple the signals and make them AC shorted and so on right, but those are intended capacitances that we had used for our use. However, however we know that however, you know that what is a MOSFET? By its very definition a MOSFET is a metal oxide semiconductor right. So, your MOSFET if this is a p-type substrate on top of that p-type substrate we had an oxide layer and on top of that oxide layer we had a metal layer and obviously, here we have n plus n plus right. So, this is metal, this is gate, here this is oxide and here we have I mean we can connect this call this drain, we can call this source right and we have another terminal which is body right.

Let us do the other way around let us say this is drain, the other one is source, this is drain, this is source, call this body and we have we kind of assumed that source and bodies are tied together and when we did our analysis we assumed that they are they are all rounded that is fine, but in our all our analysis what have we done? We have essentially said that when the transistor is on then we have this is n MOS transistor. So, we have a battery Vgs, we apply a battery of value Vgs right and what does it do? It essentially creates a sea of electrons here right, it creates a sea of electrons. So, these this is a sea of electrons that is that is something that we call a channel right. I provided obviously, I mean the way I have drawn it is assumed that V d s is almost equal to 0, this

is under the assumption that V d s is almost equal to 0 right. So, the in other words the transistor is in deep linear region ok.

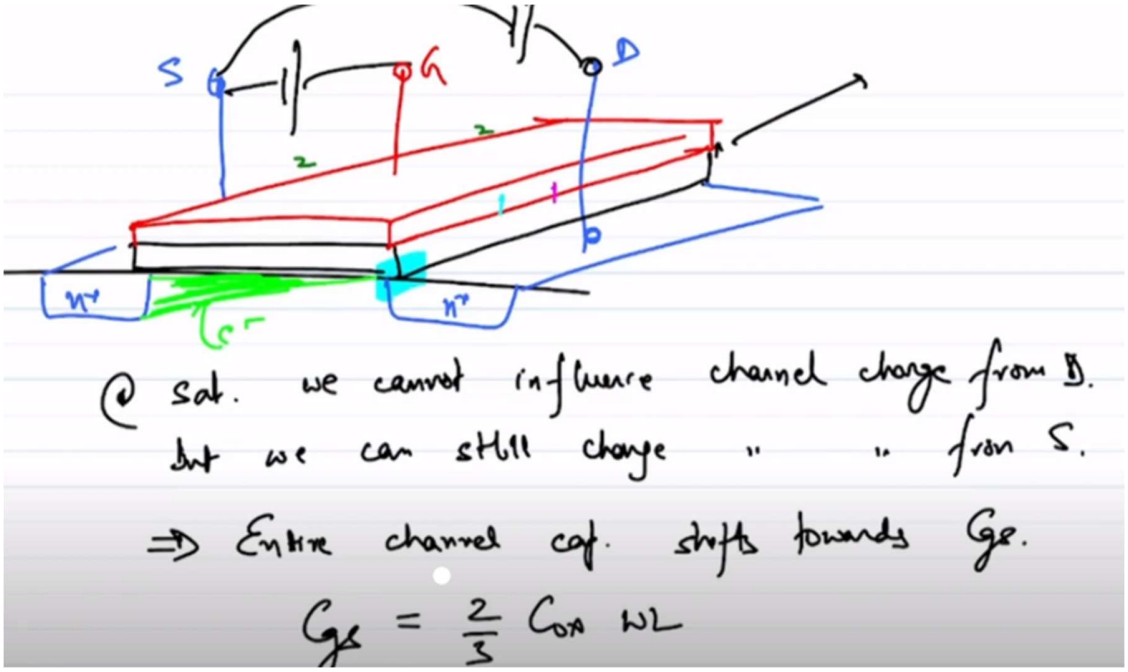
So, if that is the case what is the what is going to happen right. So, let me just say that we have electrons here. So, what is going to happen ok. So, let me short these two also like just for sake of clarity right. So, what is going to happen if now I change the gate to source voltage right, what is going to happen? So, this is a capacitor essentially your in your MOSFET, this is a capacitor right.

So, this is gate and this is a channel, this is this is a channel. So, essentially we can think of this as the distributed capacitance between the gate and the channel correct. So, so essentially you have capacitance between the gate and the channel and also you have this source and drain contacts on either side right. You also have source and drain contacts on either side. So, this is a distributed capacitance and you have channel charge here.

So, if you change the gate to source voltage you are able to change the channel charge right. So, what is the value of this capacitance? What is the value of this capacitance? Note that this capacitance whatever we have done right that your Ids in the Ids equation in linear region the current expression is mu n Cox W by L then Vgs minus V threshold voltage times Vds minus half Vds square. What is this Cox? This Cox is capacitance per unit area. Which area? Is the area of the area of the total area of the gate right. So, if I sketch the gate area right.

So, if I sketch the gate area properly this is what it will look like. So, on if I make it like a three dimensional structure. So, essentially this is what it looks like we have seen this structure before when we introduced the MOSFET right. So, you can assume that this is drain and there is a source contact somewhere there, there is a gate contact somewhere there and what is L? This is L and what is W? This is W right. So, if that is the case what is the total area of this entire of this entire plate total area is W times L.

So, under linear region. So, in linear region when the channel charge is uniformly distributed. The total capacitance between gate and channel will be what? Will be equal to Cox times W times L. Cox was the unit area capacitance per unit area we simply multiplied by the area and we total capacitance right. But note that the issue here is that even though we can we have we can define this capacitance between the gate and the channel, the channel is not accessible to the designer right.




However, what is accessible the source and the drain contacts are accessible. So, if I can express the capacitance between the gate and the source and the gate and the drain then it will make our life easier right. It will make it the capacitance will be useful to a designer. So, what we generally tend to do is to say that we understand there is a we understand there is a channel charge. We understand that there is a channel charge right, but we also understand that this channel charges will ultimately get influenced by the terminal voltages right by the gate source and drain terminal voltages.

So, what we tend to do is to say that we will split this capacitance into two parts because this is like a uniform charge distribution. We split the capacitance between two parts and we will say that half the capacitance will apportion towards the between the gate and the source side and half the capacitance will apportion between the gate and the drain side. So, essentially what we are saying is instead of assuming the capacitance exists between gate and the channel we will say that the capacitance exists between gate and the source and gate and the drain ok. And we will say that this gate and this between the gate and each of them are identical because there is no way to distinguish a rectangular slab of charge whether it is more towards the source or more towards the drain. So, we will just simply say that CGS will be equal to Cox times WL by 2 right and between the gate and the drain it also will be Cox times WL by 2 right.

So, in linear region so, your CGS becomes Cox times W times L by 2 and Cgd so, becomes Cox times WL W times L by 2 ok fine. But this is also not enough because what you will notice if you look carefully you will notice that there is a there is certain amount

of overlap in this around this junction right there is certain amount of overlap between the physical overlap between the oxide and the angular region right. They say there is certain amount of physical overlap and that has to be there because if that overlap is not there your channel there will be a region where the channel cannot be formed right both towards the drain and the source side and your transistor action will be lost right. So, there has to be an overlap, but because of that overlap there will be a physical capacitance and extra capacitance also associated between the different color between the gate and the drain and on the other side also between the gate and the source right, but this capacitance right. So, similarly we will have an what so, similarly we will have a plus C overlap capacitance on both sides right.

Now, just like Cox is expressed in terms of capacitance per unit area C overlap is expressed as capacitance per unit length because how does a C overlap change does C overlap gets change with respect to length if I increase the length of the transistor and do not increase the width we will see will this overlap capacitance change clearly not right because ultimately it looks like if I increase the width of the transistor if I go this way then I will have more overlap capacitance and however if I even change the length L overlap capacitance will not change right. So, essentially which essentially means that this C overlap or we express that this as C g s overlap. So, this C g s overlap is often in expressed in terms of per unit length right. So, this will we call it C g s overlap times L sorry per unit width times W and similarly C g d overlap will also be expressed in terms of per unit length a per unit W. So, this is this will be C g d overlap times W.

Note that this overlap capacitance will be same for towards the gate and the source and the drain side, but just that we are used to using different terminologies. So, we use right. So, to quickly recap C g s. So, C g s overlap unit is farad or I mean capacitance per unit length and C ox unit is capacitance per unit area ok. So, why is this critical? This is critical because we need to know this because for some reason let us say we double both the width and the length of the transistor right.

So, if W and L increases by let us say alpha times then what will happen to what will happen to what will happen to C g s cap? What will happen to C g s? So, in this case C g s will increase by approximately by C g s will approximately increase by. So, before I proceed I should also I should also make a comment that this capacity instead of saying C g s capacitance let me call this channel capacitance right. So, this is a channel capacitance and this is the other one the overlap capacitance right. So, if we say this then we can say that the channel capacitance channel capacitance increases by alpha squared and the overlap capacitance increases by alpha. So, they do not scale similarly.

So, this will this can have design impact right ok fine that is something that is good to

know, but another interesting thing that happens is what happens when our transistor is in is in saturation region right. So, this is this is this is this is kind of triode regions operation that we are dealing with, but let us say our transistor is in saturation region then what happens. So, let us see. So, in saturation region we get rid of this stuff what changes. So, what changes during saturation region? During saturation region we have a battery anywhere between gate and the source, but the drain is at a higher voltage than source right because pinch off and all right.

So, when pinch off happens what changes? When pinch off happens the channel charge distribution changes right. So, the channel charge distribution changes and what does it look like then the channel charge distribution essentially then at pinch off looks like something like this right. So, we have so this is the electron concentration right and what happens at the drain gate junction drain channel junction at the drain channel junction there is essentially no no channel right we have pinch off. So, if that happens right so this is let us say at saturation. Saturation we have something between the drain and the source also otherwise saturation condition will not be will not be ascertained.

So, at saturation we cannot influence channel charge from drain because of pinch off correct. So, which means that the entire charge now if I if I change the if I change the gate to drain voltage this channel charge is not going to is not going to change right. So, which essentially means that all the influence right all the influence is now between the all the influence of changing the channel charge falls on the shoulders of gate to source right. So, but we can still change channel charge from source right. So, another effect of this we saw earlier the impedance looking into the source is low right because we can change the channel charge and hence change the current, but the impedance looking into the drain is high because we cannot essentially change the channel charge we cannot change the current right.

So, that was another manifestation of that I mean the similar things can be argued in terms of channel charge in terms of capacitance we cannot change anything since we cannot change the channel charge by moving the drain voltage. So, I mean if we only move the gate to drain voltage and keep the gate to source voltage constant then we will essentially will not be able to change the channel charge right. So, however the channel charge can still be influenced by changing the gate to source voltage which means that entire channel charge which was initially equally split right the entire capacitance that was initially split between the gate and the source and the gate and the drain is now shifted towards the gate and the source right. So, which means that which implies entire channel capacitance shifts towards CGS and what is CGS now? CGS is again Cox times WL, but not by 2 and not also C ox times WL it is a apparent I mean as it turns out is two-third because I mean I will not get into the derivation why is two-third you can look

up in a device textbook, but the intuition is the area of this channel charge right the area of the channel charge has reduced and if you talk about the center of gravity of the channel charge right then you can say that it is like two-third towards one side then the other right. So, since the total charge has also reduced.

So, we assume that the capacitance is also reduced and then essentially CGS becomes two-third Cox times W by L. So, this is the two-third Cox times WL this is a channel charge right. However, the overlap capacitance still exists because that is a physical capacitance because it was physical overlap between the gate and the drain. So, which means that I still have that overlap capacitance. So, this will be CGS overlap times W and what is Cgd now? Cgd becomes we don't have anything any diffusion capacitance.

So, diffusion capacitance goes to 0 right. So, essentially this becomes 0 plus whatever we had Cgd overlap times W right ok. So, as it turns out as it turns out generally the channel capacitance is much much greater than overlap capacitance. Therefore, we approximate CGS to be approximately equal to two-third Cox W times L and we disregard the overlap capacitance. However, Cgd has only overlap capacitance it does not have the channel capacitance which means that you cannot neglect that.

So, this remains C overlap or Cgd overlap times W which essentially means that which essentially means that if W and L increase by a factor alpha right then CGS increases by alpha squared and Cgd increases by factor alpha right fine. So, so this is so what is the impact of this? What is the impact of this on a circuit designers life right? So, let us go back to the very good old common source amplifier and see what is the potential impact right. So, let us go back to the rudimentary circuit that we started off with quite a few weeks back right. So, let us say this is this is our circuit right ok. So, what is the impact of that CGS capacitance? So, why will that CGS capacitance come that CGS capacitance will come here right.

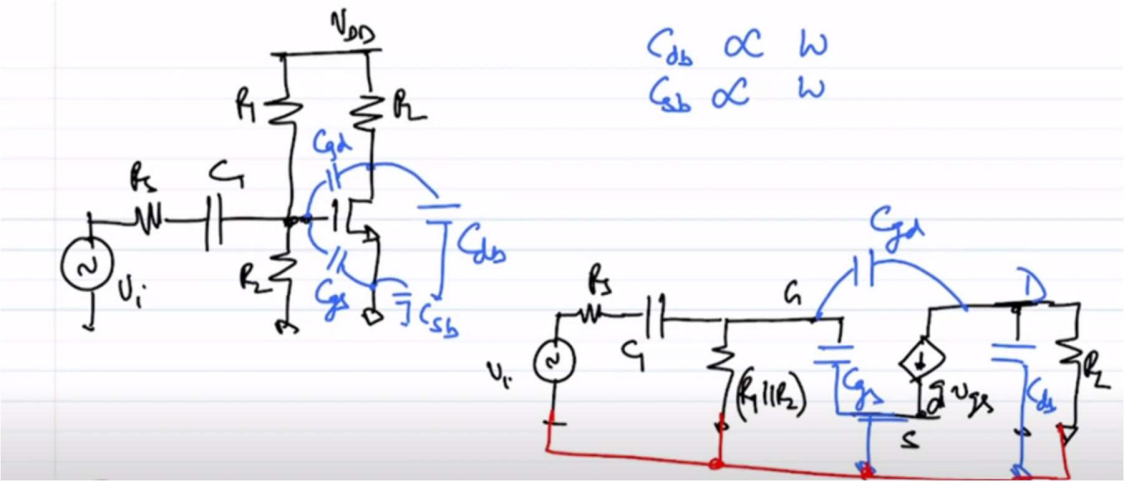
So, this will be the CGS where will that Cgd capacitance come that Cgd capacitance will come here right. Is there any other capacitance that you can relate to? So, let us go back to this structure is there any other capacitance that you can relate to? There will be other there will be other capacitances and what capacitances? Note that this is a I think this structure is better suited to make that point. So, let us say this is the P substrate right. So, note that what this drain body junction is reverse biased right. So, what is body? So, this is a PN junction here, this is a the body is P and the drain contact is N.

So, it is a PN junction in order for the transistor to act properly operate properly what do you expect that PN junction to be? Do you want it to be forward bias or do you want to be reverse bias? We obviously want it to be reverse bias because we want all the drain

current to flow into the source and not into this PN junction into the body right. So, we want it to be reverse bias. So, if you reverse bias a PN junction what happens? If you reverse bias a PN junction then again there will be some depletion charges that will get that will get formed and because they will have depletion charges essentially it is a diode reverse bias diode which means that you will have also have some capacitance associated with it and where will the capacitance come from? That capacitance will be between the between the drain and the body. Similarly, you will have a capacitance between the source and the body correct. So, essentially we will have additional capacitance between drain and the body and we will also have a capacitance between the source and the body and what will this capacitance be proportional to? What will be Cdb proportional to? Will it be proportional to the length? Will it increase with the length or will it increase with the W? Really this also will increase with W right because length does not really affect Cdb right.

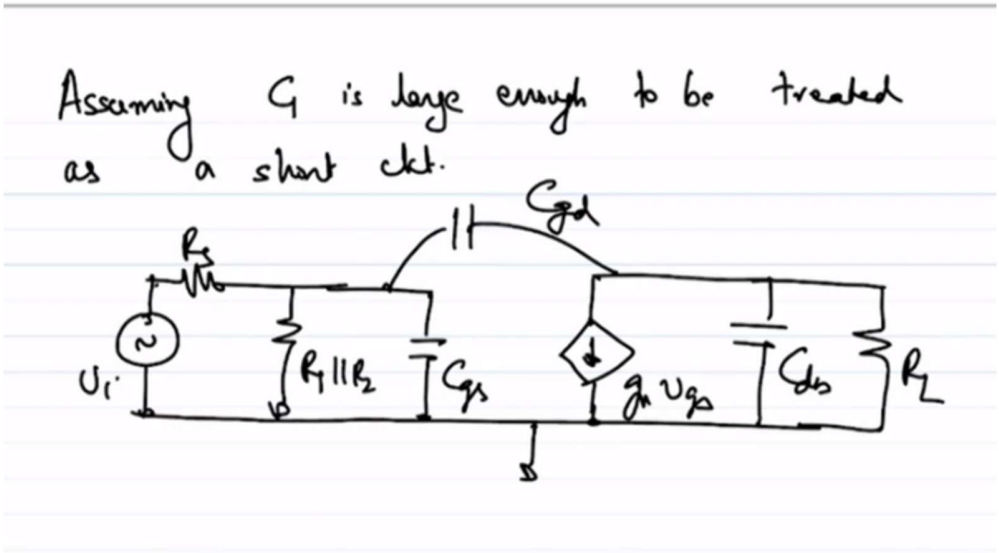
If we increase the size of the transistor by increasing W Cdb increases right. So, Cdb is also Cdb is also proportional to W and Csb is the same thing it will also be proportional to W right. So, we should also keep that we should also keep that in mind ok. So, what is so this is this is all good. So, what is the now clearly you can see that we have more components to deal with right.

So, what so how should we go about analyzing this? So, what we will do is so let us split this let us use the small signal equivalent of this of this architecture right. So, what is the small signal equivalent of this architecture? Let us further assume that these sizes of R1, R2, Rs, C1 have been adjusted in such a way that they do not load the input right. We have been doing this forever now even if we do not assume that let us assume that so let what is the small signal equivalent of this structure let us sketch the small signal equivalent of this structure then we will make the assumptions. So, now the small signal equivalent now changes to this is Vi, Rs, we have C1, then we have this R1 parallel R2 right. So, now you have a Cgs, Cgs between the gate and the source, we have this Cm, Vgs, then we have this RL but on top of that now we have a drain to made a mistake here.




So, we will have a Cdb rounded, RL grounded and probably we should I should mark these with a different color because these are new elements that we are incorporating. So, this becomes the Cgs, so this becomes Cdb and this becomes Cgd right. So, this is drain source. In case of a common source amplifier, in case of a common source amplifier this happens to be ground right. So, since this happens to be ground all of them get that connected, but note that if you are dealing with a common gate a common drain amplifier then it will not be the ground right.

So, then you will have to make adequate I mean approximate you will have to account for that ok fine. So, I was talking about an approximation, what is the approximation that I was talking about? So, the approximation that I was talking about was follows. So, we if we are designing a decent common source amplifier what are we assuming? We are assuming that R1 parallel R2 is not loading the source C1 is large enough to be treated as short circuit and so on and so forth right. If those assumptions are right right, so assuming as a designer we would like to make a circuit that works right. So, which means that these assumptions have to be right otherwise we have to go back and change the component values.




Assuming C1 is large enough to be treated as a short circuit and R1 parallel R2 does not I mean we don't have to assume this I mean let us keep this right. If this is the assumption then how does our life change? So, how does this structure change? So, this is RS this becomes R1 parallel R2 then this becomes CGS. Now CGS can be grounded because our source is grounded then we have GM VGS we have CDB right we have RL and we have CGP. So, these are the this is how the transistor model now evolves right. We have neglected channel and modulation because we have RL right we can neglect a channel modulation ok.

So, if this is the case then we have to go ahead and analyze this structure once right before we understand what is the impact of adding these capacitances and how it affects our life going forward ok. So, that is what we will do next. . .