**Course name- Analog VLSI Design (108104193)**
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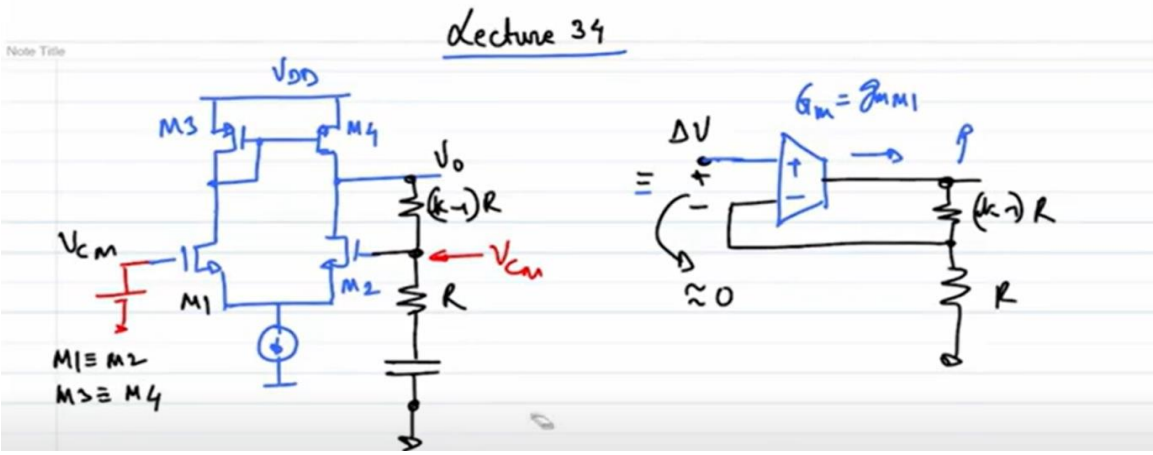
**Week- 11**
**Lecture- 34, module-01**

Welcome back, this is lecture 34. So, in the previous lecture we saw how to use a differential amplifier in negative feedback and a quick recap what we saw that if we have a differential amplifier with a current mirror and we load. So this is let us say Vcm and we do this. Incrementally, this circuit is equivalent to in the incremental picture this is equivalent to some gm. What is that gm? The gm is equal to gm of M1 and this is where assuming gm1 is equal to M2 right, where assuming gm1 is identical to M2 and M3 is identical to M4 right. And we are further saying that in the incremental picture, this is what that is happening sorry, I should not apply Vi here right?

So, this should be grounded and in the incremental picture, this is what that is happening ok. So, one of the arguments that we made was at the fag end of the first module of last lecture well we made a comment I made a comment that the voltage at M1 is being driven right voltage at M1 is being driven by battery Vcm, but we assume that if you put it in negative feedback in this way that this voltage will also become Vcm right. So, what was the genesis of that assumption? The genesis of the assumption was the fact that this entire circuit is a negative-feedback right. So, for example, if you look to the if I assume that for the time being let us assume that you have some voltage here right?

Let us say we have some voltage Vin. So, let us say we have an incremental voltage delta V at this node right. If there is an incremental voltage delta V at the positive terminal right what is going to happen? This is going to push out some current, this is going to increase this voltage which means this is also going to increase this voltage right. It will increase this voltage and when if gm times R is very large what will be the difference between these two voltages? Difference between these voltages will almost be equal to 0 or it will be equal to steady state error right. So, if that is the case which means that the negative feedback loop the job the negative feedback loop is trying to neutralize the voltages at the input of the amplifier right when put in negative feedback ok.




So, by the same token what is this gm what is this? So, let if I here mark this with a different color what happened here right. So, what is this gm? This gm is nothing, but the circuitry that has been made using the transistors in the figure in the left right. So, if incrementally it is the gm is trying to or the trans conductor is trying to pull the two voltages between its input nodes close by the same will try to happen in the transistor equivalent of it right. So, if the other way of arguing is that let us say this voltage is not exactly equal to Vcm it is slightly less than Vcm right. So, this voltage is less than Vcm this voltage is less than Vcm.

So, then what is going to happen what do you think will be the current through M1 and through M2. So, current so if this is I0 if that voltage is less than Vcm the current through M1 will be higher than I0 by 2 and current through M2 will be lower than I0 by 2 correct. So, this current will be higher and this current will be lower, but the higher current will come will get mirrored through M3 and M4 and it will try it will try to increase the voltage Vo thereby try to increase the voltage Vcm. And this-phenomena will keep on going till that voltage at the feedback node till this feedback voltage is sufficiently close to Vcm right. So, that is why if the gain is infinity right if the gm is infinity for example, then these two voltages Vf will and the other node voltage will always be equal to will always be equalized ok that is essentially the principle.

So, while doing quiescent calculations on the negative feedback that is why we often say that since we are trying to make a circuitry with high loop gain high gains at high gain we are using a high gain amplifier to make a negative feedback. It is a fair assumption to assume that the voltages between the plus and the minus terminals of the differential amplifier are equalized under quiescent conditions right? So, this is again under the caveat that we understand they will never be exactly equal there will be a steady state error. So, in order to figure out the steady state error we will do some other calculation, but we have first order approximation it is a good approximation to make that the plus and the minus terminals of the of the transconductance will be will be similar right ok. So, now while we

were at the fag end of the lecture we also saw that what happens if we put a or rather if I if I show it here what happens if I put a resistance RL here.

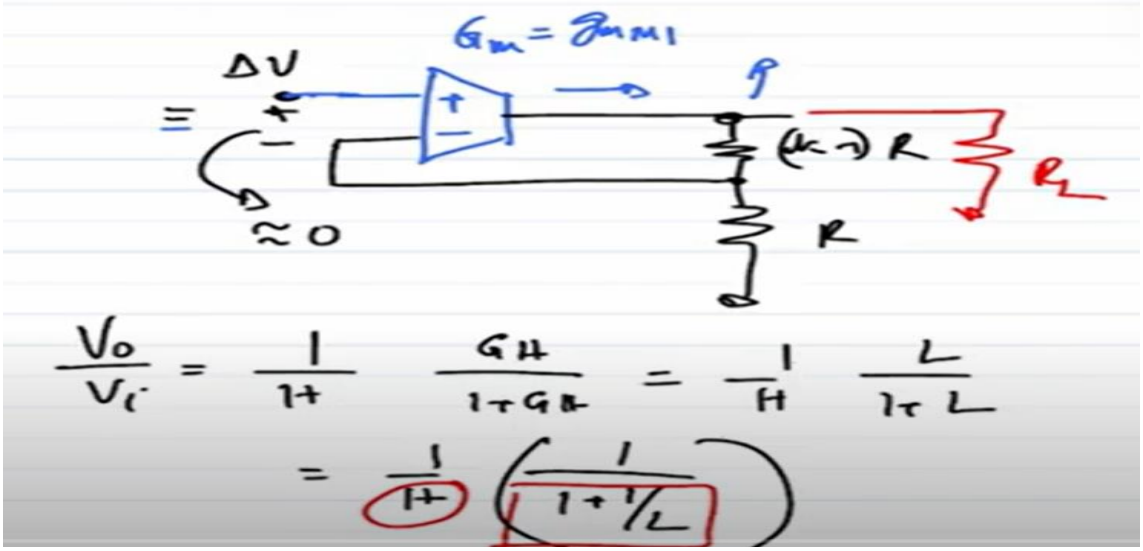
So, this resistance RL has a effect of lowering the loop gain right. What is the loop gain in the absence of RL the loop gain was gm times k r in the presence of RL the loop gain becomes gm times k r parallel RL right. So, if the loop gain is loop gain reduces if RL is much smaller than k r which means the loop gain becomes gm times RL. So, if the loop gain reduces then all the good things of negative feedback vanish right because why because ultimately we know that what do we know we know that Vo over Vi is essentially 1 by h L by 1 plus L right or GH by 1 plus GH. So, let me write in that format GH by 1 plus GH this can also be written as 1 over H, L by 1 plus L this can also be written as 1 by H 1 by 1 plus 1 by L right?

So, I mean either of these two lectures are fine, but the key thing to key thing to notice is that how do I get h I get h by setting the loop gain to infinity right. So, whatever is the if I if I set the transconductance to infinity whatever gain whatever closed loop gain Vo over Vi will get is essentially H right and what should I do to get the loop gain in order to find the loop gain we can break the loop somewhere. So, that loop remains unilateral right and also there is no loading that is no current that is getting drawn and then we apply a test voltage and check the return voltage right. So, this is what we have been doing till now. Now note that that is also not a foolproof way of going about things there are sophisticated ways of finding out loop gain even when those two criteria that I talked about are not satisfied, but they are not part of this course for now.

So, what we will assume that there is a part there is a there is some part of we can identify some place in the circuit where there is no current going in and we will break the we will break the loop there and try to find out the loop ok fine. So, now, quickly what is the problem of putting that RL if RL is sufficiently low the loop gain goes down what happens if the loop gain goes down if I look at this equation if the loop gain goes down the denominator increases which means Vo over Vi is not 1 over H right H in this case was k which means Vo over Vi will not be k it will be lesser gain than k and note that loop gain is what loop gain is a function of gm gm times something and gm is a function of temperature gm is a function of process voltage temperature right. So, which means that in order to make Vo over Vi it is gain closed loop gain independent of process voltage temperature we need to at least ensure that the loop gain is very high if L is very high then Vo over Vi becomes insensitive to temperature variation right. However, if Vo over Vi is not very high then again we have all the bad things right your gain will depend on temperature where you are what time of the day and so on right. So, that is we do not want.

So, the key thing is we are striving to get larger and larger loop gain ok. So, whatever

modifications in the circuit that we will do if that impacts our Loop gain then we will have to take a call and we will have to figure out what we need to do to restore the loop gain back right. Why am I saying all these things I am saying this because if let us say RL if RL gm times RL is not large enough right? Let us say you are in the absence of RL you are getting a loop gain of 100 you put back put in RL such a small amount such a small value the loop gain drops from 100 to 10 right? So, what will impact what will affect? Obviously, a closed loop transfer function will get affected the steady state error will get affected right your final your final error will get affected and so on right



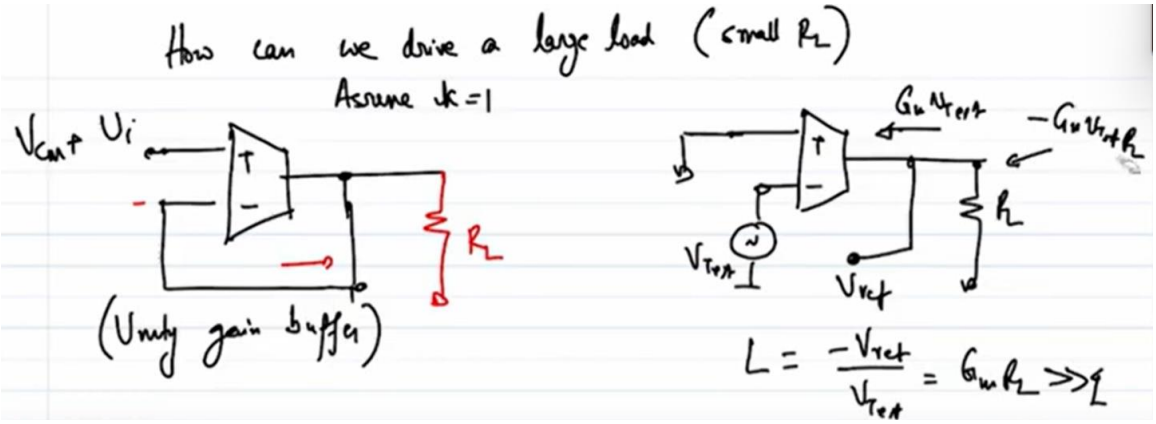

So, essentially the input will not track the output or the output will not track the input accurately. So, so, so what so to summarize what we are essentially saying is that what happens what happens if we have to drive or rather how do we drive a large load? Again large load means small RL or Large capacitance ok. So, we since we have not dealt with this capacitance driving too much. So, let us say till now, let us assume that we are talking about small RL for the time being ok.

So, how can we do that? So, let us go back let us go back to our topology. So, let us say we have this so this is Vi ok. Let us assume you have Vcm plus Vi right we have Vcm on top of this right? So, even though this is a small signal model this is fair enough assumption to assume that since the inputs are tracking each other Let us assume we can apply Vcm on top of that also ok ok. And we need to we need to drive an RL.

Let us make a further simplification let us say that we I mean we what happens if k is equal to 1 let us say we let us say we target k equal to 1 let us say target assume k is equal to 1. What I mean is k if k equal to 1 k if k is equal to 1 this is shorted right. If that is shorted I mean the stop that is connected here R is essentially irrelevant I do not need that I can

basically get rid of it because ultimately the entire feedback is entire part of the output is getting fed back to the input. So, this is often called unity gain buffer right? So, this is often called unity gain buffer why? Why is this called unity gain buffer? Naturally you see that in this case now in this case if the feedback if the loop gain is high and the feedback is tracking each other these two voltages will be almost equal which means this voltage will be also Vcm plus Vi.

So, the input-output is tracking the input without any if hopefully without any attenuation right? By the way what is the loop gain in this case? How will you find out loop gain? Quickly how do you find out loop gain? You short the input right break the loop apply a test voltage and find out what is the return voltage right. So, if I do this what we get is what this current is gm times Vtest. So, this voltage is minus gm times Vtest times RL. So, that is equal to Vreturn.




So, L is what? L is minus Vreturn by Vtest which becomes gm times RL right. So, once you know once you know the loop gain all you have to do is to size gm in such a way that gm times RL becomes much greater than 1 and then I mean then all the good things of the loop will happen that is the input will track the output ok fine. So, let us let us go back to what wherever we were before we got distracted ok. So, let us say we are targeting a unique decision buffer and let us assume that gm let us assume that gm times RL is is comparable to 1. Then obviously our negative good things of negative feedback are not applicable anymore input is not tracking the output and so on.

So, what should we do? So, what what is the core problem the core problem is the output impedance what is the output impedance of this guy what is Rout how will you find out Rout again short the input apply test voltage at the output and find out the test current we have done this multiple times Rout in this case is 1 over gm right gm RL approximately equal to 1 means what R out is approximately equal to RL right which means this is a problem because we will not be able to drive this RL efficiently ok. So, what so what is the solution how did we tackle these solutions before? So, we were we might as well think of

putting a voltage buffer correct we may as well think of putting a voltage buffer between the between this gm and RL and that might might help us correct. So, what is the simplest voltage buffer that we know of a common drain amplifier right it is a voltage control voltage source gain of unity right? So, let us do that. So, let us put a common drain amplifier.

So, let us say let us put a common drain amplifier here and ok. So, even before I connect do this and let us say I have to drive it drive the RL and we know how to drive RL now right we can drive RL through a capacitor of value C infinity and all. So, those things are taken care. So, now can you tell me can you tell me where should I connect this Vo should I connect Vo to the positive terminal of the gm or should I connect Vo to the negative terminal of the gm? So, let us say we connect Vo to the positive terminal of the gm to start off right.

So, then how do we know how do we go about ascertaining whether a negative feedback loop is indeed in the right direction or not what should we do we can assume that there is a hypothetical excitation somewhere in the loop let us say there is an excitation here the voltage increases what is what is going to happen to the voltage the output of the gm this guy will increase if that guy increases what is happening to Vo it is a buffer without an inversion. So, this voltage also increases which means there is a positive feedback which means this is not correct. So, what we can essentially do is to say that this has to be connected to the negative terminal right ok. So, if you want to test it out let us do the test once more if this increases this increases sorry if this increases this voltage decreases because I am applying the excitation the negative terminal of the gm if this decreases this decreases which means the loop is trying to nullify the excitation that we are hypothetically inserting ok. So, this is this is negative feedback this is all good.

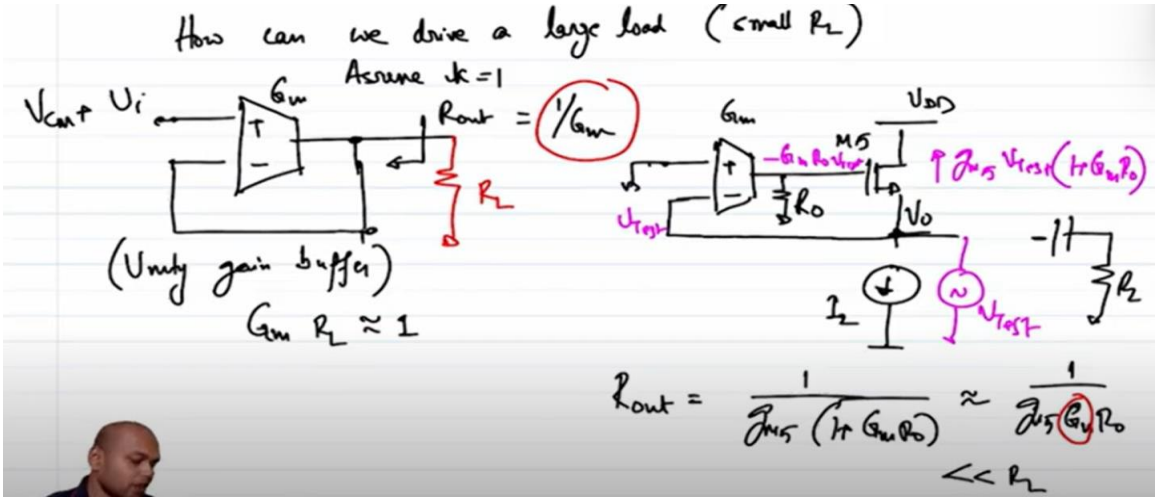
So, let us say we have Vcm plus Vi ok, ok? So, how do we know let us say this is I2 or Let us we had like let us say this is M5 and let us say this call this I2 fine. So, what do you think will this structure be able to drive our RL? How do we know how do we go about figuring that out? Again same old test we will have to find out the output resistance right. So, how do you find out output resistance? So, same old test right. So, we let us assume this is there for the naming and let us apply, let us apply an incremental Vtest.

Note that all these things have to be done in the incremental domain, but I am I am sure by now we are all very comfortable with analyzing incrementals models without replacing the transistors with their incremental equivalent we can do all those things in our head. So, so let us go ahead and do this this I test also I2 also goes out because incrementally that does not make any sense that is open. So, if this is Vtest this guy is shorted, right? So, what is this voltage is Vtest right? If that voltage is Vtest what do you think oh by the way I

forgot to put the output resistance of the gm right, I forgot to put the output resistance of the gm.

So, this is Ro is incremental output resistance Ro. So, if that voltage is Vtest right what is going to be the voltage on Ro it will be minus gm times Ro times Vtest correct ok. If that is the if the if the gate voltage of M5 is minus gm times Ro times Vtest and the source voltage is Vtest how much current by the way there will be an incremental current through M5 in which direction the incremental current will flow? Note that incremental current is gm times Vgs pointing down downwards, but in this case source is positive and gate is negative in the direction we have in the way we have marked the excitations which means the current will be moving upwards right. So, upwards of value gm5 times Vsg in this case which is Vtest times 1 plus gm times Ro correct.

So, what is on Rout what is Rout, Rout becomes 1 by gm5 1 plus gm times Ro right? So, if gm Ro is much higher than 1 this becomes 1 by gm5 times gm times naught as long as this is much lesser than RL we should be able to we should be able to drive right. So, why is this a better configuration the previous one the previous one the output resistance was what previous one output resistance was 1 over gm in this case output resistance is 1 over gm, but it has been reduced by a factor of gm5 times Ro right ok.

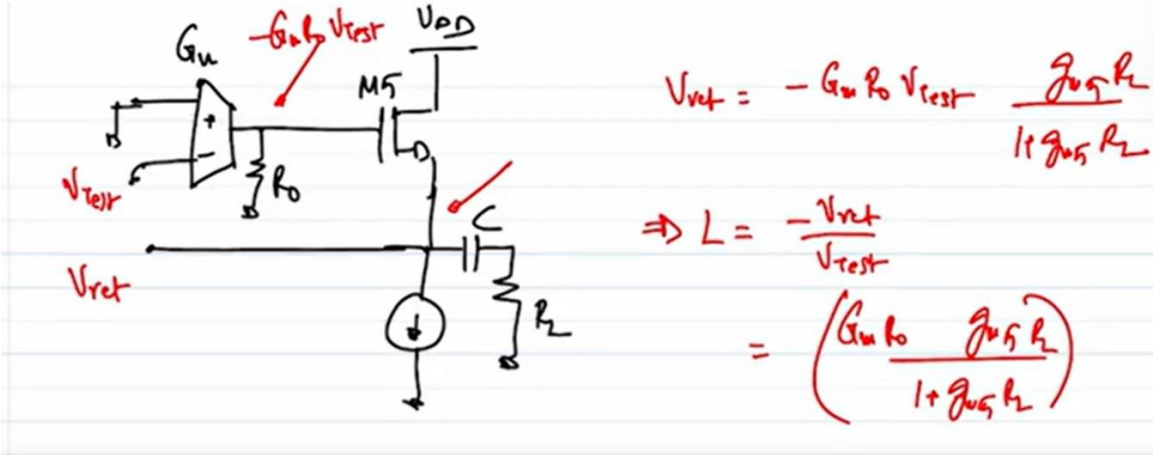



So, you can see that immediately we are making a much better voltage buffer right we are making a much better voltage buffer by putting two of the stages together ok.

So, let us sketch it again. So, if we ensure that if we ensure that ensure high loop gain right by the way what is the loop gain what is the loop gain in the of this structure what is L how do we figure out what is L we do the same thing we short this open this apply Vtest right. So, we have some Ro here this is gm and find out what is a find out what is the return voltage right? So, this is Vreturn what will be Vreturn. So, let us do let us do this. So, this

becomes minus gm times Ro times Vtest right.

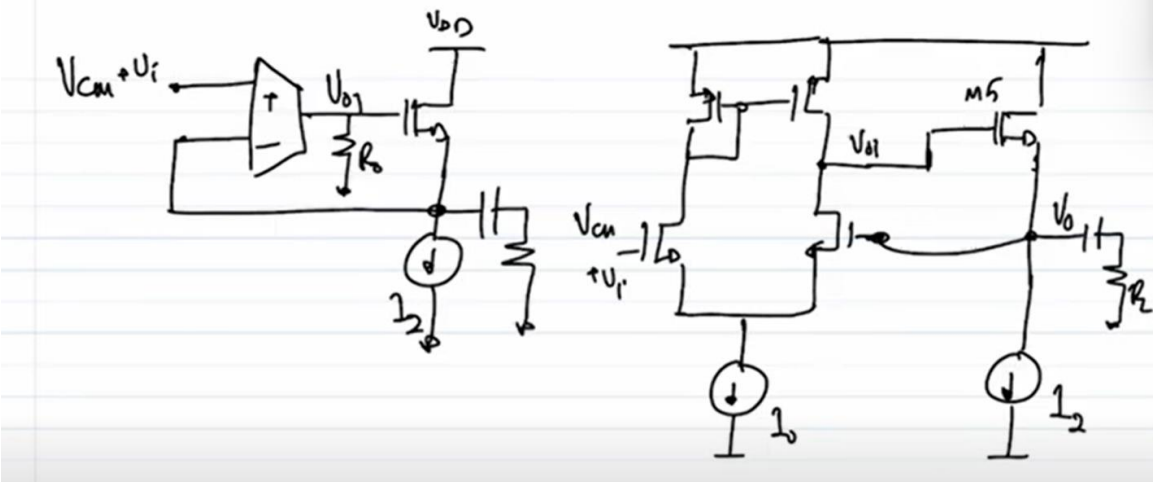
So, what is this voltage if C is large enough if C is large enough this becomes gm5 by 1 plus gm5 RL. So, which means which means this voltage becomes Vreturn becomes whatever was the gate voltage that is minus gm times Ro times Vtest times gm5 by 1 plus gm5 RL right which means loop gain L is minus Vreturn by Vtest which is gm Ro times gm5 by 1 plus gm5 RL ok. So, in the absence of the second stage in the absence of M5 what would loop gain have been the loop gain would have been gm times RL right? So, now in this case I am kind of isolating the I am isolating the gm times Ro terms I am not allowing RL to load the gain of the first stage because as long ok I think I made a mistake here it will gm5 RL times right yeah. So, so as you can see that as long as we can ensure that gm5 RL is not 2 less than 1 even if gm5 RL is like 1 or 2 or something like that then also we will get a decent enough loop gain and RL the loop gain is not directly proportional to RL anymore right.




So, since the loop gain is not directly proportional to RL anymore which means it dependent the dependency of the loop gain on the final load that is driving reduces which means this becomes a better it becomes a better amplifier better driver ok fine. So, this is all good. So, let us put the transistor Level block diagrams together ok? So, what will be the transistor Level block diagram instead of this pulse gm we will have to put replace that gm with our transistor Level equivalent ok. So, this is Vcm plus Vi the first output node right let us say Vo1 this is a Vo1 this Vo1 goes to M5 and this goes to I2 right and here I have RL this is the final Vo and this Vo is connected to the negative terminal of the input what is the negative terminal this is a negative terminal.

So, these two get connected together right? So, this becomes your this becomes a voltage buffer which can drive enhanced loads right because ultimately it can drive a much smaller value of RL than the single-stage configuration would have. Now, the question to you is

we could have as well I mean what is so holy about choosing an M5 for driving the output load a common drain amplifier can as well be made using a PMOS transistor right?




What I am essentially saying is this I could have as well said that this second stage ultimately this has to be a second I mean this is ultimately we are making incrementally this right we are making a common drain amplifier right a common drain amplifier can as well be a PMOS transistor Like this and I flip the minus and the plus sign this will also be fine right. So, if that were the case this architecture would have been something like this and output have been connected here, right?

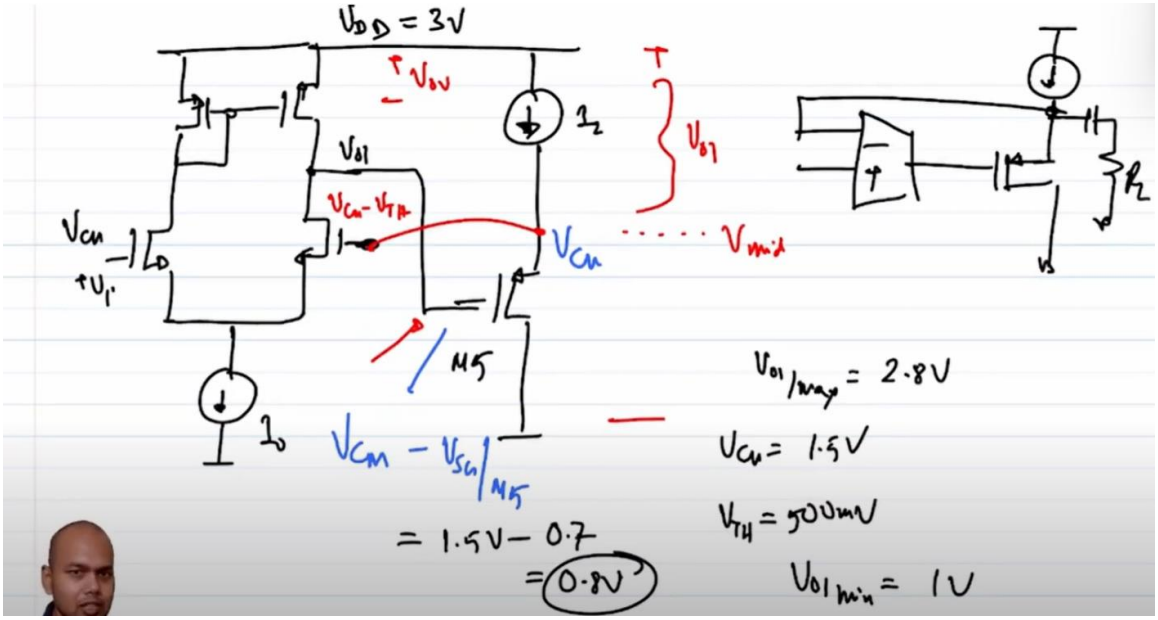
So, this would have been M5. So, why not this structure why did we choose the other structure that is with the NMOS second stage? Now, one might argue that we can use either of them depending upon the situation and that we absolutely right answer, but what situation that is the question to ask right? Now, in the incremental sense, you can use either you can use either the NMOS second stage or the PMOS second stage right or other NMOS M5 or PMOS M5 right. So, but the issue is the following issue is that of quiescent voltage right? So, what do you think is the range of voltage of V1 for which the first stage will work properly right.

So, what do you think the V1 is how far can V1 go V1 can go at least one overdrive to closer towards VDD and on the bottom side how far can it go this can go to Vcm minus threshold voltage. Now, depending upon what is VDD what is Vcm this seems like Vo1 is closer to VDD than to ground right. So, if I say this is the whole range and this is let us say V mid then Vo1 is likely to be here, Vo1 is likely to be situated in the top half right quiescent twice. If that is the case and we want to use Vo1 to drive M5 and I choose M5 to be a PMOS transistor what do you think is a required quiescent voltage for M5 for M5 to work properly? So, if this the using configuration that we have if the circuit operates properly the output will be Vcm right under quiescent.

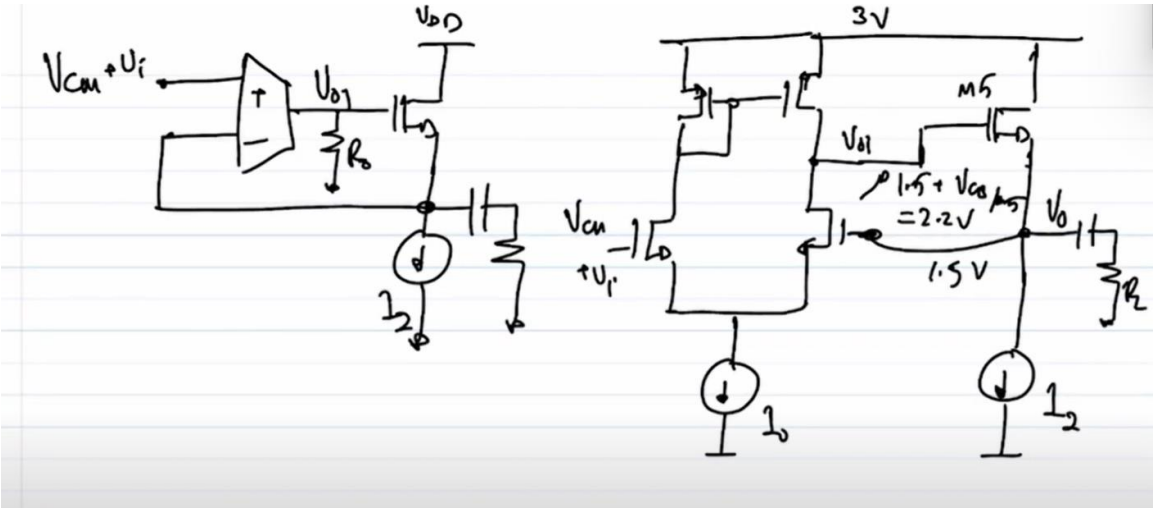
If output is Vcm under quiescent what do you think the gate voltage of M5 will be this will be Vcm minus Vsg of M5 right? If this becomes Vcm minus Vsg of M5 what do you think will be the value of V. So, let us say VDD is equal to let us take some example let us say VDD equal to 3 volt V overdrive let us say is I do not know maybe 100 milli volt or 200 milli volt let us say V over I mean I know in the course we have been taking V overdrive as 1 milli 1 volt throughout but that is more or less for the ease of our calculation. But in reality even that our VDD supply voltages are not like 10 volt 5 volt and so on typically it is 3 volts or less with the modern technology. So, the overdrive voltages are also chosen appropriately the overdrive voltages are generally of the order of 100 to 200 milli volts right.

So, let us say assume V overdrive is 200 milli volts right? So, V01 max becomes 2.8 volt and let us say Vcm is 1.5 volts somewhere in the middle and let us say threshold voltage is 500 milli volt right. Then what is Vcm minus 1 threshold voltage that is 1 volt right and if you want if you want Vsg of an if you want a overdrive of 200 milli volt what is Vgs or Vsg that becomes 700 milli volt which means this voltage becomes like 1.

5 volt minus 700 milli volt that is minus 0.7 which is 0.8 volt right. So, as you can see this the requirement for M5 to be biased properly requires the gate of M5 to be at 0.8 volt but the minimum V01 mean is 1 volt which means the first stage and the quiescence condition of the first stage and the required quiescent condition of the second stage are not are not mapped properly right. They are not shaking Hands properly right. So, that whatever is the second stage whatever quiescent condition that is the second stage wants the first stage is not able to give it.



But what about the what about this case. So, let us do the same thing let us say Vdd is 3 volt and let us say Vcm is I do not know maybe same 1.5 volt ok. So, so what do you expect the gate voltage of M5 to be in this case you expect this to be 1.5 plus Vgs of M5 right.




So, Vgs of M5 is again let us say 0.7 volt. So, this becomes 2.2 volt right? So, that is well within the range of well within the range of the first stage quiescent output voltages. It is because of this reason often an NMOS second stage is preferred if the first stage is also also has an NMOS input pair right. If the first stage where a PMOS input pair right if we have a PMOS differential amplifier then the second stage also we would have preferred it to be a PMOS second stage ok. .