**Course name- Analog VLSI Design (108104193)**
Professor – Dr. Imon Mondal
Department – Electrical Engineering
Institute – Indian Institute of Technology Kanpur
Week- 9
Lecture- 25, Module-2

Welcome back. So, we have been discussing, we have been introducing PMOSFET as a separate complementary device, but I mean the question that should I mean that we should ask ourselves is how does it help, how does it help in our situation. So, let us go back to the requirement, then we will let us see whether a PMOSFET can help us or not. What was the requirement? The requirement was we wanted this terminal, we wanted this terminal right V naught whatever is connected to V naught from the top should be the drain. Now, in case of an PMOSFET the lower potential terminal is always a source potential right. However, note that in this new device which is a source potential, which is a source terminal the higher the higher potential terminal is the source terminal right.
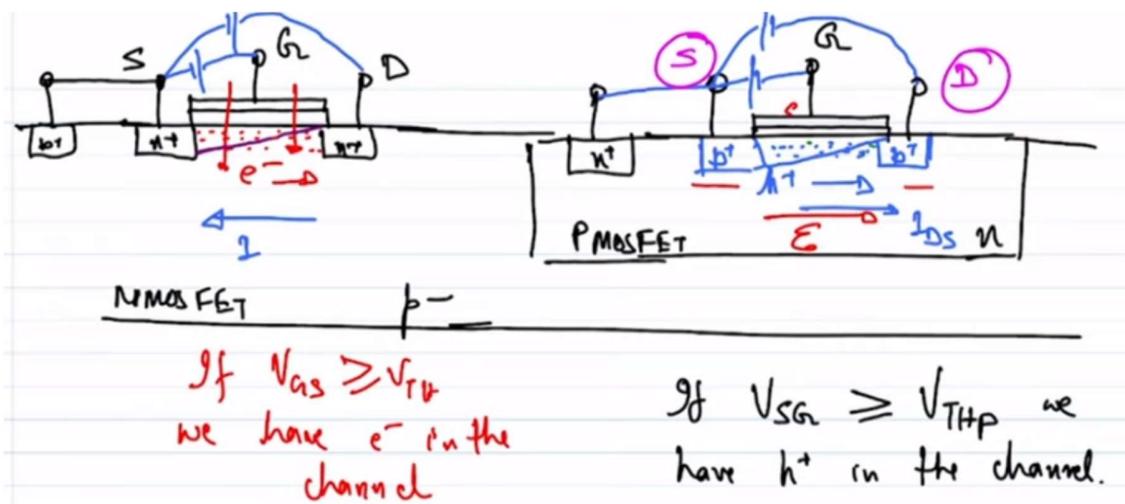
So, in a PMOSFET so, let us make the distinction. So, this is NMOSFET this is PMOSFET. So, to turn on to turn on so, let us write it in this way. If Vgs is greater than equal to threshold voltage, MOSFET is on right.
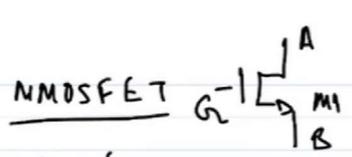
So, instead of writing MOSFET what I will write is I will always call this let us call this M1, M1 is on correct. What else we know? We also know that higher terminal voltage, higher voltage terminal between let us say I call this G this is A between B, terminal between A and B is drain. In case of a PMOSFET so, I will not put the arrow as of now. In case of a PMOSFET gate remains gate let us put the gate and let us call this M2. If Vsg right is greater than some Vth right let me call this Vthp ok then M2 is on and lower voltage terminal between A and B is drain right.So, in a sense if we connect if we connect Vdd on the top right if we connect Vdd on the top

and the current flows from the top to bottom right. So, the this terminal becomes the drain let me use a different color to differentiate. So, this terminal becomes the drain, this terminal becomes the source, this remains the gate right. And since and if I go back to our if I go back to the cross section the carriers are flowing from the higher potential terminal to the lower potential terminal right. In case of an NMOS the carriers were flowing from carriers for electrons they were flowing   from   the   lower   potential   to   the   higher   potential   right.

 So, in case of a PMOSFET the carriers are flowing from the higher potential terminal to the lower potential terminal. Higher potential terminal is the source and hence the arrow goes to the source and in the direction of current flow right. So, hence the arrow is arrow goes on the source in the direction of the current flow. So, note that the direction of arrow points towards the inwards it is point inwards in case of a PMOSFET in case of an NMOSFET the arrow points, points   outwards   ok   fine   that   is   great.   So,   let   us   proceed.

 So, now that we know that the physical phenomena the physical underlying phenomena the physics behind the devices are almost identical just that the carriers are reversed and he says everything in essence everything is reversed. So, whatever was the source in NMOSFET becomes a drain in a PMOSFET whatever was a drain in PMOSFET becomes a source in PMOSFET the gates terminals are fine. But now in case of a NMOSFET we require higher potential at the gate to turn on higher potential in the gate with respect to the channel to turn on the device in case of a PMOSFET we want a lower potential in the gate than the channel to turn on the device right ok. So, in essence the source should be at a higher potential than the gate in case of a PMOS whereas the gate should be at a higher potential in the source in case of a NMOS. Similarly, without again deriving everything right from scratch so let we what we will do is we will take the equations of the NMOSFET and modify it and make it a PMOSFET equation right.
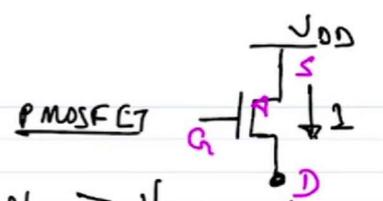
  So, let us write out the equations for the for the NMOSFET. So, in case of a so, Ids is equal to half mu n Cox W by L Vgs minus threshold voltage I am putting a subscript n because now we have both PMOS and NMOS to deal with. So, it is better to discern them whole squared times 1 plus lambda Vds right. So, in case of an PMOSFET this will be the current flows from source to drain so everything is reversed. So, this becomes Isd right is equal to half mu P Cox P is a mobility of the of the carrier in this case this is whole times Vsg minus Vt Pn whole square times 1 plus lambda Isd.

$$I_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_{THN} \right)^2 (1 + \lambda V_{DS}) \quad \bigg| \quad I_{SD} = \frac{1}{2} \mu_p C_{ox} \left(V_{SG} - V_{TPN} \right)^2 (1 + \lambda V_{SD})$$
<div align="center">Sat.</div>

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left[\left(V_{GS} - V_{THN} \right) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad \bigg| \quad I_{DS} = \mu_p C_{ox} \left[\left(V_{SG} - V_{THP} \right) V_{SD} - \frac{1}{2} V_{SD}^2 \right]$$

Note that everything is identical but for the fact that the polarities of the currents and the polarities of the voltages have gotten reversed. What is the equation? This is the equation in saturation this is saturation. What is the linear current equation? Linear current equation is Ids is equal to mu n Cox W by L Vgs minus threshold voltage times Vds minus half Vds square. In case of the PMOS it will be Isd is equal to mu P Cox times Vsg minus threshold voltage times Vsd minus half Vsd square right. Another piece of information that I should tell you before we move on is that in the literature when you see in some books we tend to use these PMOS equations as negative I mean we tend to have negative Vgs negative Vds negative threshold voltage in case of a PMOS equation that is also fine but the only key thing that you need to differentiate is the fact that sometimes in the literature the threshold voltage is referred to as the voltage required on Vgs right.

So, in the literature what we refer to is that sometimes threshold voltage is measured with respect to Vgs and not Esg. So, you might see negative BTHP in some textbooks which is absolutely correct and absolutely fine but in this course what we will do is simplify our life and we will say that we will be using the modulus of BTF BTHP and we will stick to so that we will stick to this terminology of Vsg wherever possible. Hence what we need to do is to ensure that that even if we are given a threshold voltage of negative right. So, we will make it positive by taking the modulus and use these current equations as we proceed ok. This is just to make our life easy and we do not want to learn the current equations all over again for the PMOS given that we have put in so much effort in understanding and the operation of an NMOS right.

So, essentially if we know how a NMOS works what is the NMOS equation, current equation? We also know how the PMOSFET will work and we also know the PMOSFET current equation and just that I where does that we have to flip the terminals ok. So, now so this is as far as this is as far as our terminologies are concerned and as far as our currents and the voltages are concerned absolute currents and voltages are concerned, but now it is time to move on to the incremental model also right. So, in a NMOS what is the incremental model? So, in an NMOS transistor the incremental model is this, this is the source, this is a drain, this is a gate right and the current the incremental current is gm times Vgs and the and the drain to source voltage is referred to as gds right this is in case of an NMOS and we refer to gm as doe id doe Vgs and we get the multiple expressions that we get right mu n Cox W over L times Vgs minus threshold voltage right or we whatever we call it as mu n Cox twice mu n Cox W by L Ids ok. So, what will be the corresponding incremental model in our case, in case of the PMOS? So, let us let us do that. So, in PMOS also we will have a we will have a gate voltage right and we will have an

incremental terminal right, we will have an incremental voltage control current source which is connected between the drain and the source terminals and we should also have a incremental resistance connected between the drain and the source terminals, but now we the way we have sketched it right, where we have sketched it in the actual sense right by take you back to this diagram the source was on top right the drain was at the bottom right.

So, we what we essentially and what I am essentially pointing to is we need to see we need to establish which is the drain which is a source what is the direction of the current in the current source right and so on. So, for that what we need to do is we need to again go back to the drawing boards once again and then and write out the equations right. So, let us say Isd is equal

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{THN})$$
$$= \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{DS}}$$

$$I_{SD} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L}(V_{SG} - |V_{TP}|)^2$$
$$\frac{\partial I_{SD}}{\partial V_{SG}} = \mu_p C_{ox} \frac{W}{L}(V_{SG} - |V_{TP}|)$$

to half mu p Cox W by L Vgs or rather V sg minus mod of V t p whole square right. So, what will how should we define gm, if we want to define the gm at the same way as the in most transistor because we do not want to get confused too much as to into thinking what should we what should be the definition of gm right. So, let us do the usual thing first.

So, what will be if we define gm as del Isd del V sg right. So, what I am saying is if we do del Isd del V sg what should we get we should get mu p Cox W by L V sg minus V t p correct ok. So, this will be the this will be the incremental current between the source and the drain with respect to V sg correct. So, let us say this is a source terminal this is a drain terminal right. So, this will be if we call this as gm right and we say that we will keep the same current direction as in the in MOSFET because again we do not want to learn something new unnecessarily if we can draw a parallel between some things what we already know.

So, we do not want to change the sense change the incremental model right. So, we are trying to see how far we can get by without changing the incremental model and learning a brand new thing right. So, the current direction if we keep it the same way. So, what will be that what will be that current? The current is between source and drain which is now gm times V sg correct. So, because note that gm in this case we are defining as del isd by del V sg correct ok.

And this is the gds what will be the gds? Gds we do not have too much of a problem because in case of a gds the current direction is not too much of an issue in our in MOSFET model gds was lambda ids in case of a p MOSFET model gds will be this is lambda n now this is lambda p ids

right. So, this is what it is right, but now you might turn around and tell me that this might be a bit more I mean this I have been telling that this is we would like to keep these terminologies and everything same, but here I am using Vgs here I am using V sg. So, this seems to be another extra thing to recall. So, what we will do is we will say that we will keep this Vgs only right we will not make this V sg we will keep this Vgs. So, let us keep this V give this as Vgs sorry if we keep this as Vgs what we need to do we need to flip the terminal of the current source essentially this becomes pointing upwards right.

So, in other words this becomes our incremental model this was our incremental model for our n MOSFET this becomes our incremental model for the p MOSFET right. So, note that there is a stark similarity between these two models because as far as the incremental picture is concerned we do not really do not care whether this is n MOSFET or a p MOSFET because in the incremental sense everything is a linearized small signal equivalent of voltage control current sources and resistors and so on right. So, the similarities are similarities between these two models are the gate remains as gate gmVgs remains as gmVgs gds remains as gds there are two important distinctions right the important distinctions are the important distinctions are that the source and the drain terminals we have expressed in the other way around. So, in this case the so in case of n MOSFET the source terminal was at the bottom in this case the source terminal. So, you the different color the source terminal was at the bottom in this case the source terminal is at the top and the drain terminal in this case was at the top here the drain terminal is at the bottom and the third thing that is slightly different is the fact that the direction of the current source is also flipped.

Now, if you want to make this exactly identical we can still do that right. So, what we can still do is we basically can take the incremental drain to source model and flip it right. So, what I am essentially saying is this the PMOS equivalent incremental equivalent becomes this is gate we are marking this as drain and this as source and this as gmVgs pointing upwards correct. Why are we doing this because in the total picture in the total picture we generally tend to have the source on top source on top drain here gate here. So, these pictures look equivalent.

Alternatively if you are not comfortable what you can also do is the following. What you can also do is this is keep the gate as gate right and we let us say just like in case of an NMOS we had the drain on top and source on bottom we can still do that because note that here the current was flowing from incremental current is still flowing from drain to source we keep it as gmVgs and this becomes gds. So, these two models are also identical right. So, there is absolutely no change between this model and this model and the model in the bottom is exactly similar to the model of an NMOS transistor right. But I mean you can use either that is there is no I mean there is I we won't make any distinction if you choose to use the same model but I personally prefer the model on the top because there is a correlation between there is a there is a relation between the incremental model and the actual transistor because in the actual transistor we tend to put source on top in the incremental model the source is on top.

We tend to put the drain on the bottom in case of a PMOSFET here also the drain is at the bottom of the PMOSFET. So, the visualization of the of the network becomes easier right. So,

hence in this course we would like to solve our problems using the model using the model on the top. However, if it helps in your case your personal case you can use you can choose to use either right. So, before we close today's lecture let me just point out what are the let me just point out what   what   can   we   gain   from   the   from   using   a   PMOSFET.

So, note that this was our incrementally this was our common source amplifier right with the nMOSFET. This was grounded this was source this was gmVgs I am ignoring gds right I am ignoring gds. But let us say I mean if I put gds also there is no harm say gdsn let me call this gmn and this is rl ok. So, what was the whole motivation behind search of PMOS? The whole motivation was to was to replace the rl with a with another transistor whose drain is connected to V0   right.

So, this was V0. So, if we can use a PMOS because the higher terminal voltage is now a source then in principle this is possible to. So, let us keep the bottom guy as is. If we replace the top guy if we replace the rl with a PMOS transistor and we replace it with its PMOS equivalent that is we replace it with with this structure right. So, what do we get? We get this is gate this is gate of the PMOS let me call this gp right this is Vgmp Vgs the gmVgs Vgs I should be using a different name right. So,   let me call this gsp gmp Vgp sp and we have Vdsp right.

Now, if we connect these two here correct and if we incrementally short the source just like we have been doing in case of in case of the circuit in the left then what do you think will be the resistance looking up and what do you think will be the distance looking down? The resistance looking up in this case can potentially be very high because we are looking at the drain of the transistor right and if we can if we look if in principle the resistance looking up into the drain of a transistor can be infinity right. But we know that in presence of channel modulation it cannot be infinity but it will be much higher than what we would have gotten if we use an rl and in this case it is possible it is possible to probably get a common source amplifier whose gain is not limited by the quiescent drop across the load resistance right. So, we will start the next lecture from this position and we will see how actually using a PMOS will help us breaking the trade-off between the quiescent drop or and the achievable gain right ok.