

Course name- Analog VLSI Design (108104193)
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Week- 5
Lecture- 15, module-01

Welcome back, this is lecture 15. In the previous lecture, we were discussing how to bias our common source amplifier right. So, we were discussing how to bias our common source amplifier at least on the side of the gate. We were not particularly bothered of what was happening at the side of the drain. So, let us shift our focus to wherever we stopped in the previous lecture. And what was the problem that we are trying to address? The problem that we are trying to address was the fact that if we want to apply our signal like this, then the problem that we encounter is we encounter a floating battery.

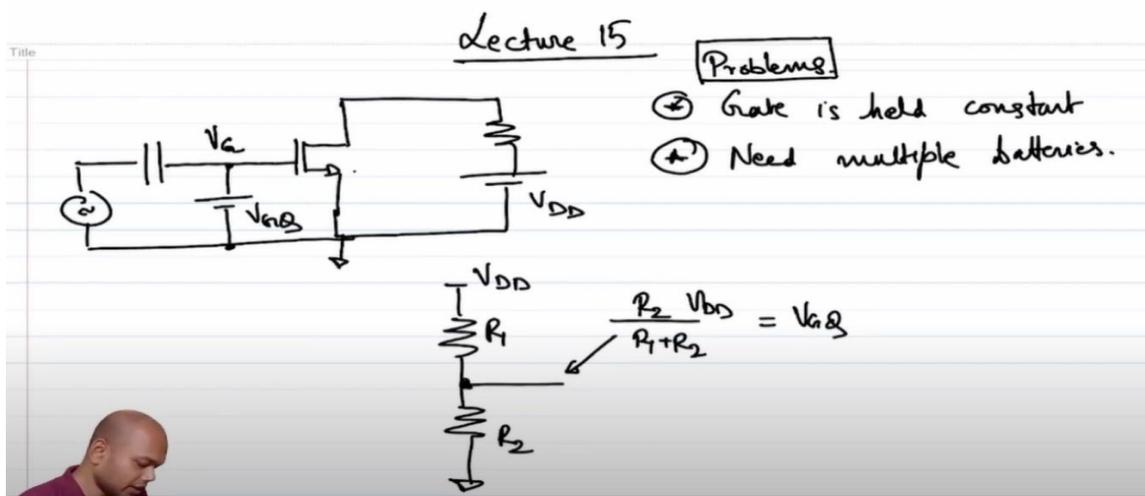
Then we saw that a sufficiently large capacitor acts as a floating battery. But if we have a unlike a battery, a sufficiently large uncharged capacitor right will not be able to do the job because ultimately what is a battery? A battery is a stored house of a sufficient amount of charge. And if you have a battery with sufficient charge, then you have a voltage across it. But if you have a capacitor with no charge right, you do not have any voltage across it.

So, in order to it is not only sufficient to use just a large capacitor, you will also have to charge it with the voltage. And then we said that is then if in order to charge it with the voltage, why do not we apply, why do not we put a battery of V_{gq} right, why do not we put a battery of V_{gq} here? Because it seems like I will be able to charge these two plates of the capacitor with the voltage V_{gq} in the absence of the incremental input. But then we saw that what is the problem? If we do this, the gate of the transistor always remains fixed at V_{gq} . So, that is of no use because ultimately we want the signal input signal to appear at the gate of the transistor right. We want the Y_{11} incremental Y_{11} looking into the network to be 0.

In this case Y_{11} is infinity because looking into the network, I have a battery, a battery incrementally is a short circuit right. So, this is of no use. So, this so the problem number 1 here is the problem number 1 is you have a fixed battery. So, what is the problem number 2? And what is and there is another problem, problem number 2 is something that we briefly alluded to in the previous lecture was that in generally in an integrated circuit or generally in any circuit, you will see that we are given one master voltage source and one master battery right. One master power supply from which we need to derive all the other power all other voltages that are necessary right.

So, I mean right away here we see that we are using two sources one is V_{gq} , one is V_{dd} which is something that we do not have a luxury of simply because I mean this is a circuit with one transistor. If you have like hundreds of transistor, would you use hundreds of voltage sources? Maybe not right. So, so the two problems the problem number 1 is gate is held constant right. So, this is problems and number 2 number 2 is need multiple batteries right. So, let us say I mean let us address the second problem first.

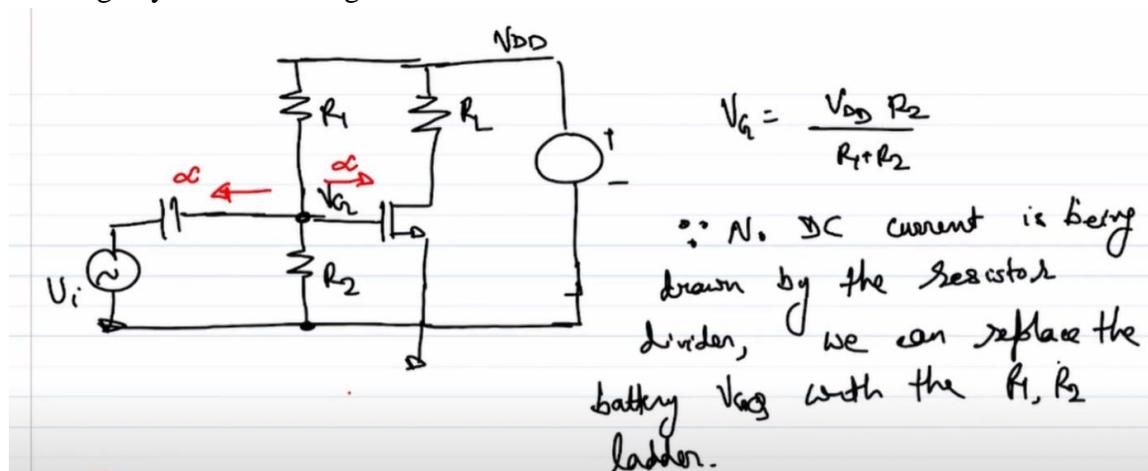
Let us say we want we want to get rid of multiple batteries, we want to generate the voltage V_{gq} from V_{dd} assuming V_{dd} is the highest power supply and that we saw right I mean the requirement of V_{gq} was far lesser than the requirement of V_{dd} when we took the examples a few lectures back right. So, how can I get if V_{gq} is less than V_{dd} , how can I get a value how can I get reduced value of V_{gq} from V_{dd} ? What is the simplest way? Let us say V_{dd} is 30 volts that we had that we had gotten a few lectures back and let us say V_{gq} is supposed to be 3 volts. So, what do you do? You would simply say that simply say that if this is V_{dd} we will put a resistor divider let us call this R_1 , let us call this R_2 and if I choose if I choose R_1 and R_2 in such a way that this voltage what is this voltage? This voltage is R_2 by R_1 plus R_2 by V_{dd} if I choose this to be equal to V_{gq} right right, then it seems like I can I can use this voltage right. So, let us let me mark this as V_g and then it and then I can look it looks like I will be able to use this contraption to bias the transistor right ok. So, let us try that just try that and see what is whether this indeed solves the problem.



So, what will you do? I will redraw it in such a way that I can get away by drawing only one V_{dd} . So, let me call this R_1 right and let us assume we have a battery here of value V_{dd} ok. Here I have this capacitor, here I have my voltage source V_i and here instead of that battery V_{gq} what we are trying to do? We are trying to replace the battery with a resistor divider R_1 and R_2 and this is V_g . What do you think the value of V_g will be? The value of V_g in this case will be whatever we saw in the previous slide right. So, V_g will be V_{dd} times R_2 by R_1 plus R_2 right ok.

So, now if I ask you a question can I always replace a battery of a lower value than Vdd with a resistor divider like this? Obviously you can think of multiple cases where we cannot I mean one example that we saw was in the introductory lectures probably in lecture 2 or something where we saw that if we load a resistor divider with another another resistances. So, that it draws current out of the resistor divider and the value of the voltage at the resistor divider node will drop right. So, which essentially means that you cannot use a resistor divider always to replace a battery because a battery is supposed to hold a voltage right, but how come we are able to use it in this case? We are able to use it in this case because there is no DC current that is getting drawn from this resistor divider right. What is the what is the DC current that is getting drawn on the left hand side? On the left hand side what do I see? On the left hand side I see a capacitor. What is the impedance of the capacitor at DC? It says an infinite impedance right.

What is the DC current that is getting drawn towards the right? What do I see at the right? At the right I see the gate of a MOSFET which is a sense in which in a sense is again a capacitor. So, what is the impedance that I am seeing? I am seeing infinite impedance which means this I am not drawing any current out of this resistor divider. Since I am not drawing any current on the resistor divider it really does not matter right. I can essentially use I can replace the battery using the resistor divider ladder. Without that we are not drawing any DC current right.



This is an important distinction to make right. Since no DC current is being drawn by the resistor divider right. We can replace the battery DG cube with the R1 R2 ladder right. If I had a scenario let us say instead of instead of a MOSFET I had another device which draws current right into its whatever is equivalent to the gate. Then this would have been a problem we would have had to see what values of R1 and R2 would satisfy our constraint of keeping that voltage at the node Vg constant right. So, but fortunately MOSFET does not draw any current. So, we are good ok fine. So, this essentially solves one part of the problem right. This solves this problem we do not need multiple batteries. So, this part is

solved.

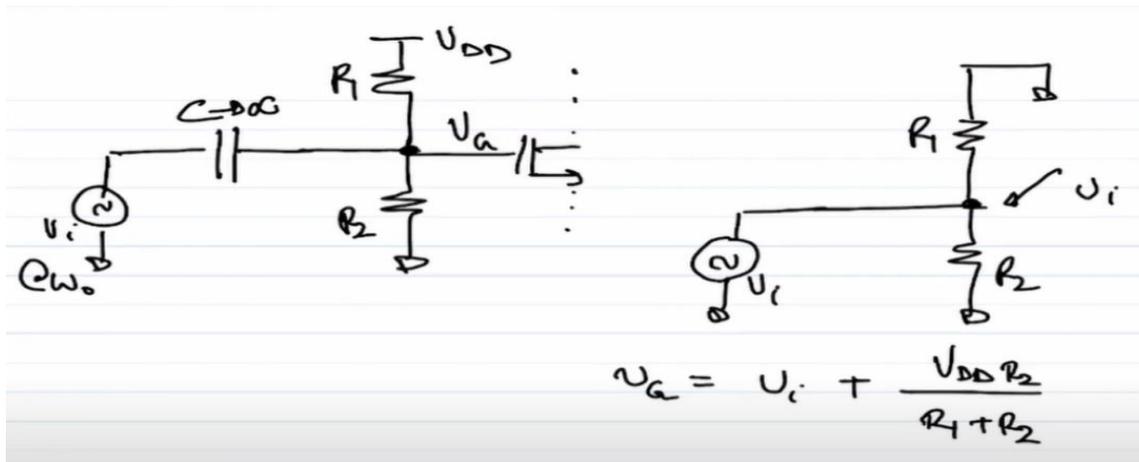
What about the first part? What about the I mean what about the signal part of the of the problem right. So, is a gate held constant? What do you think is going to happen? So, let us look at it again from the signal point of view. So, let me just sketch the gate side of it I mean I will not sketch the full MOSFET just for brevity. Let us say this is V_i you have this capacitor this is R_1 this is R_2 and you have the MOSFET here and so on and stops there. I am interested in the voltage V_g or let me say I am interested in the total voltage V_g right.

Let me just mark the node V_g here and then V_c ok. So, this C tends to infinity that is something that we have assumed ok. So, what do you think will this voltage V_g ? I can as well say that I will do an incremental analysis right. I can do an incremental analysis just like we did in case of in case of a small signal analysis earlier right. Ultimately we are interested in the incremental increment in the voltage V_g when I have applied a input V_i right.

So, what will be the incremental equivalent of this assuming C tends to infinity and V_i is not at 0 frequency right. So, V_i is at omega naught that is V_i is at omega naught, but omega naught is not equal to 0 ok. Because if V_i is at 0 then anyway I mean no signal no DC signal will flow from V_i to V_g ok. So, what will be the incremental equivalent of this? So, the incremental equivalent of this will be what should I do? I should replace all the independent voltage sources with a short circuit. So, this becomes a short circuit this R_1 remains R_1 , R_2 remains R_2 .

What happens to C ? What you see infinite capacitor is like a battery. So, the infinite capacitor is like a battery and what do we do with the battery? We short it. So, that goes off right and what do I have here? I have V_i . So, what is the incremental voltage here right? I mean it is like what am I asking right it is a short between V_i and that point. So, the incremental voltage at this point will be will also be equal to V_i .

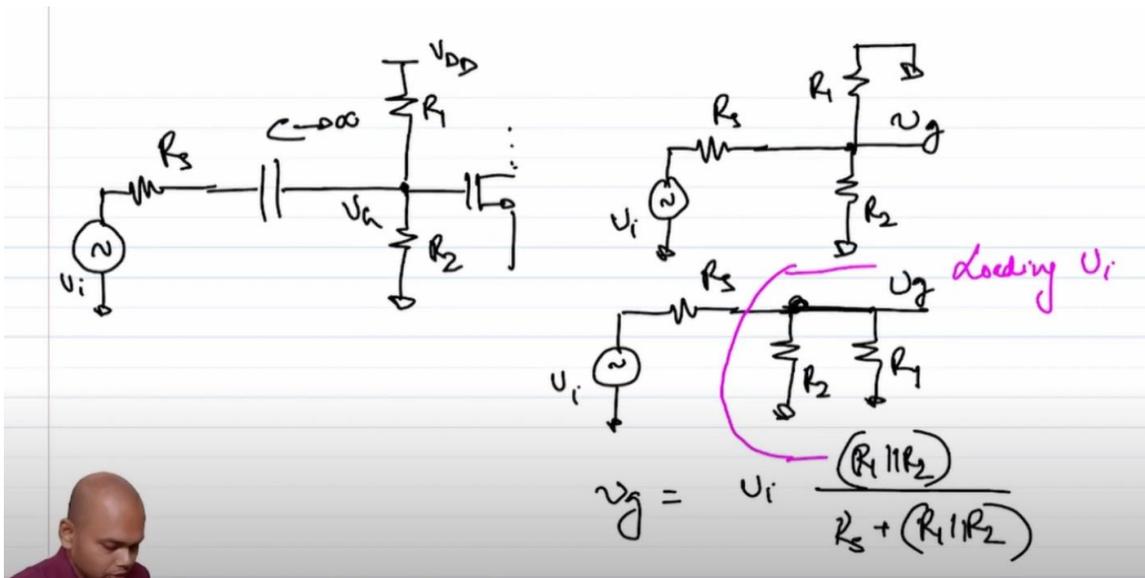
So, what will be the total voltage at V_g ? What will be the total voltage at V_g ? The total voltage will be incremental plus quiescent. So, incremental is V_i and quiescent is V_{dd} R_2 by R_1 plus R_2 ok fine right. So, seems like this is what this is what we exactly want right seems like this is what we exactly want at least of the input side and seems like putting this contraption of a capacitor and this is just a divided ladder of R_1 and R_2 seems to have done the trick right ok. But not so fast because you might have already noticed that I have made slight change as to how I have represented the source V_i . I have not marked the source impedance or the source resistance R_s which I had initially marked at the beginning of the lecture right.



So, let us put back the resistance and let us put back the resistance and see whether it has any effect or not right. So, let us put it back. So, what I meant by is let us say you have V_i , this source is always accompanied with some resistance R_s , but you cannot wish it away. You have a capacitance C and V_{DD} R_1 this is R_2 this goes here and you have a you have this MOSFET and everything. You are interested on the gate you are interested in the gate voltage right assuming C tends to infinity again.

So, what will be the incremental what will be the incremental voltage at the gate the incremental voltage what will be the incremental circuit same old same old I will retain whatever I mean I will retain R_s obviously V_i is required because V_i is I am trying V_i is the incremental source C infinite capacitance acts like a battery. So, I can short it right R_2 goes to ground here R_1 also goes to ground here right because V_{DD} is V_{DD} is constant voltage then you have then you have the MOSFET right then you have the MOSFET and let us not bother about the MOSFET right now because we are concentrating on the gate voltage ok. So, now what will be this incremental voltage V_g ? So, V_g note that V_g will not be equal to V_i right because of what because essentially if I redraw this circuit what am I seeing? I am seeing this V_i then you have R_s then you have a parallel combination of R_1 and R_2 right you have a parallel combination of R_1 and R_2 and this node voltage here is essentially V_g . So, what is V_g ? V_g is V_i times R_1 parallel R_2 by R_s plus R_1 parallel R_2 fine. So, in order to so now can you comment on how do you choose R_1 and R_2 if I want V_g to be almost equal to V_i because V_g to be almost equal to V_i is the goal is not it.

If V_g is almost equal to V_i then I know that the entirety almost the entirety of the input signal appears at the gate of the transistor. So, in other words I do not want any loading I do not want. So, this what is this what is this stuff doing? This stuff is loading V_i correct since this is loading V_i it is drawing current out since it is drawing current out the voltage at V_g is dropping right. It is not equal to V_i anymore. So, you cannot you do not have any control on V_i you do not have any control on R_s .



However you have a control on R_1 and R_2 because you are the designer you are in charge of choosing the values of R_1 and R_2 which essentially means that which essentially means that in order to ensure V_g is almost equal to V_i or I_e to prevent loading. What do we need to do? We need to choose R_1 parallel R_2 such that R_1 parallel R_2 is much much greater than R_s right. Mathematically also this turns out to be true if you see R_1 parallel R_2 is much much greater than R_s then V_g is almost equal to V_i and from the assignments in week 1 that we that we did you would appreciate that in order to prevent loading what should we need to do? The part of the network that is loading the actual network should be the resistance of that should be much much higher than the Thevenin resistance of the network that I am looking in. In this case the Thevenin resistance that we are looking in this side is R_s right and the loading part is R_1 parallel R_2 . So, in essentially if you do not want to load you have to ensure R_1 parallel R_2 is much much greater than R_s fine.

To ensure $U_g \approx U_i$ i.e. to prevent loading
 choose $(R_1 || R_2) \gg R_s$

So, if this is in designers control then we are good to go right, but there is one pesky problem what is that problem from where do I get an infinite capacitance right. So, we have been we have been liberally using this assumption that this capacitor that we have here is of infinite value right, but in reality nothing is infinite. So, we will have to replace it with the finite value of the capacitor and what will happen if I replace it with the finite value of capacitor what do you think is going to happen? So, clearly if I use a finite value of capacitor and V_i is again at omega naught not at not at 0 frequency then there will be some

voltage drop across across the capacitor right. So, let me still restrict myself to incremental equivalence and let me just simply say that this is R_1 parallel R_2 instead of drawing the entire entire stuff right. So, how do you how would you go about figuring out what is the what is I mean what value of capacitance that we need to that we need to use.

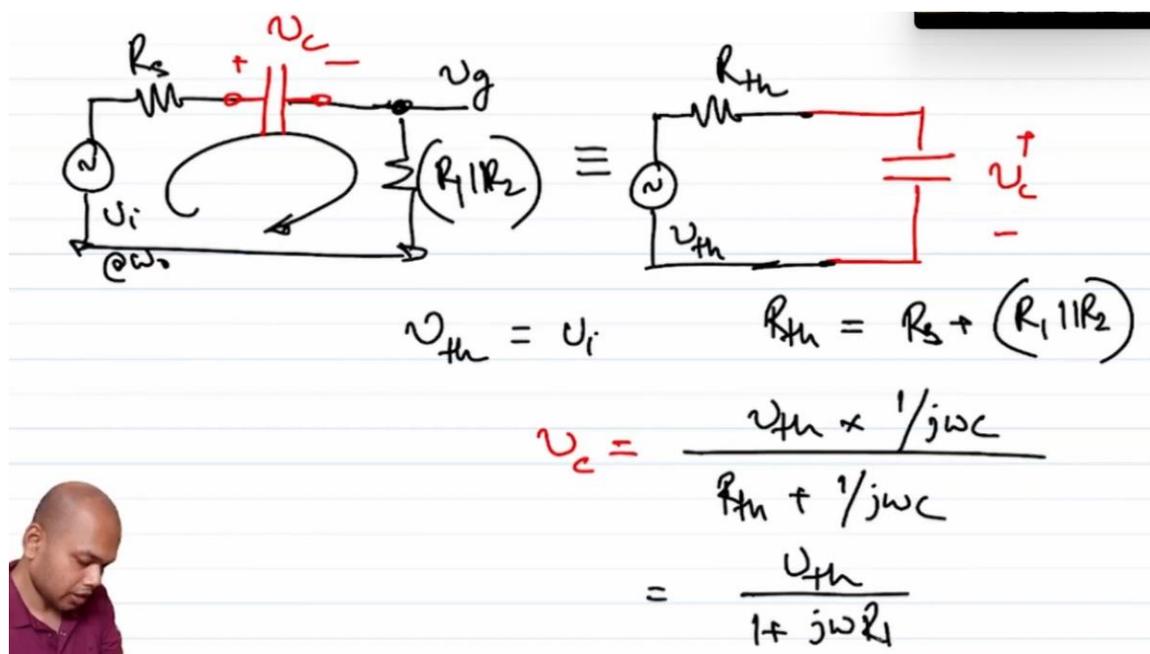
One way to think about it is that the value of the capacitance should be such that the voltage drop across the capacitance should be much much lesser than much much lesser than the voltage drop anywhere else in the in the loop right. So, note that this is a loop this is a loop if the capacitor would have been of infinite value what would have been the incremental voltage drop across the capacitor note that I am again asking about the incremental voltage drop not the absolute voltage drop right. The absolute voltage drop the DC the capacitor was holding a DC voltage to begin with that it is still hold right, but I am not talking about that I am talking about the incremental voltage drop in if the capacitor would have been infinity right the voltage drop across the capacitor would have been 0 right. But in principle we cannot get a we cannot get any infinite value of capacitance which means we cannot get any 0 voltage drop across the capacitance. So, what is the alternative? The alternative is to say that we need to size the capacitor in such a way that the voltage drop across the capacitor is much much less than anything the capacitor anything that is anything in the loop in which the capacitor is a part of right.

Now, what is a generic way of looking into it instead of saying that I mean I can have multiple loops this is a particular scenario I can have multiple loops in the network you cannot probably identify the capacitor to be a part of the one loop right it is quite possible this is a particular case I where I could where I can identify a particular loop, but in general if you face this type of problems of trying to figure out how large a capacitor supposed to be or maybe how small a capacitor is supposed to be right for in order to pass a signal without causing any voltage drop or rather without causing any significant voltage drop across it what would you do? You try to see what is the Thevenin equivalent resistance that is the capacitor sees right. So, in other words what we are saying is if I let me mark the capacitor with a different color in other words what we are saying is if I am looking at the network sitting on the capacitor right what will I see I will see in this case I will see a resistive loop right. So, I can as well I can in order to figure out what is the voltage across the capacitor what we need to do I will Theveninize the I will Theveninize the circuit and assume capacitor to be the to be the load right. If capacitor is the load say capacitor is the load and I am trying to Theveninize the circuit right. So, I am trying to make the equivalent these two equivalent as far as the voltage drops across the capacitor that is concerned right I am trying to figure out what will be this V_c right what will be this V_c ok.

So, then what should I do I am trying to I am trying to figure out what will be the Thevenin equivalent of this. So, in other words I am trying to figure out what will be V_{th} what will

be R_{th} right. If I know this then I can simply say that that I can simply say that this is a first order RC circuit right and all I need to do is to just analyze the first order RC circuit right. So, I mean one might you might turn around and tell me that why am I spending so much time on this because it is looks like it is pretty evident looking in the network on the left what I am trying to get at here is that it might not be as this evident always your network might have lots of other elements wrapped around the capacitor.

So, then what do you do right. So, use this please use this as a as an example of how to go about figuring these things out ok. So, let us do it with the simple network. So, what will be what will be what will be V_{th} the V_{th} will be what how will you figure out what V_{th} will be you open the you open the you open the load right and see what will be the what will be the voltage that you are supposed to get. What is then what is the V_{th} ? V_{th} is nothing, but if you open the capacitor the voltage across the capacitor in the circuit on the left will be will be nothing, but V_i right because no current will be able to able to flow. What will be R_{th} ? Again let us open the capacitor what will you do to find R_{th} you short the voltage source you de-energize any source in case of voltage source you short it right and you see what is the what is the effective resistance.



In this case if you short your voltage source right you short your voltage source then what is the effective resistance? The effective resistance is nothing, but R_s plus R_1 parallel R_2 right. So, R_{th} is R_s plus R_1 parallel R_2 ok. So, what do you think your V_c is? V_c is equal to V_{th} times 1 by $j\omega C$ divided by R_{th} plus 1 by $j\omega C$ right which I can simplify as V_{th} by $1 + j\omega R_{th} C$ right ok. So, which I can say that mod of V_c right or let me let me not say mod of V_c let me just keep V_c as is I should also say this V_c of $j\omega$ this

is not V_c of V right V_c of $j\omega$ V_c of $j\omega$ will be equal to a magnitude and a phasor right. So, what is the magnitude part of it? The magnitude part of it will be V_{th} by root $1 + \omega^2 R_{th}^2 C^2$ I forgot to see here ω^2 or $R_{th}^2 C^2$ right.

I should not see ω because I think I said ω naught there. So, this should be ω naught should be ω naught because I have applied a sinusoid of frequency ω naught right and it will also have a phase. What will be the phase? Phase will be minus of $\tan^{-1} \omega R_{th} C$ ok. So, let us not bother about the phase for the time being all we need to ensure is that all you need to ensure is that if your V_c right the voltage across the capacitor is, but it should be as low as possible right. We want the capacitor to be as to be almost like a short which means what? It means we want for C to act like a short circuit, we want V_c to be equal to 0 or V_c should tend to 0 i.

e. the denominator should tend to infinity right or tend to be as high as possible right which means you need to ensure ω naught or $R_{th} C$ should be much much greater than 1 which means C should be much much greater than ω naught ok. So, why do we go through all this song and dance? We are doing this all this song and dance just to just because in principle we cannot get infinite capacitor which means we need a large capacitor. If we need a large capacitor we need to figure out what is large right is 1 picofarad large is 1 nanofarad large is 1 microfarad large the answer to that is it depends. What does it depend on? It depends on R_{th} right that is good because R_{th} is in your control. What is R_{th} ? R_{th} is R_1 parallel R_2 plus R_s R_{th} is R_1 parallel R_2 plus R_s R_s is not in your control, but you can you can increase the value of R_{th} by increasing R_1 parallel R_2 that is one good thing and also I mean ω naught might not be in your control, but if you have if you are designing a circuit for high high frequency let us say if ω naught is large enough then probably you can get away with a smaller value of capacitance.

$$\Rightarrow V_c(j\omega) = \frac{V_{th}}{\sqrt{1 + \omega^2 R_{th}^2 C^2}} \angle (-\tan^{-1} \omega R_{th} C)$$

for C to act like a short ckt, we want $|V_c| \rightarrow 0$, i.e.

$$\omega R_{th} C \gg 1$$

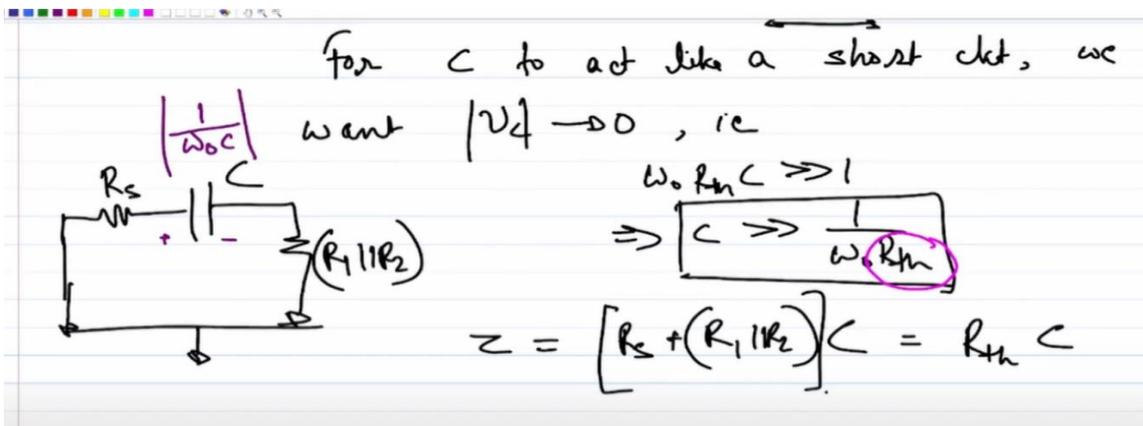
$$\Rightarrow C \gg \frac{1}{\omega R_{th}}$$

If ω naught is small then I mean nothing doing you can either try to make R_{th} very high in order to keep the value of the capacitance in check or you just have to go with larger

value of C ok. Now note that this is the same thing I mean we could have come up with the same conclusion without doing all this detailed analysis right. What is another way of coming at it? I am sure you know this already, but let me just phrase it for completion purposes. So what is this circuit? This circuit when we sketch this circuit what is the order of this circuit? Note that the order of the circuit is 1. What will you do in order to figure out the order of the circuit? In order to figure out order of a circuit is independent of a source right.

So you short the source in this case again it is a voltage source so I am shorting it had it been a current source I would have opened it. So you short the source and then try to see how many first I mean you can obviously see in this case you can see that you have one capacitor and a series connection of R_s and R_1 parallel R_2 so this clearly this is a first order circuit. So in general the trick is to see how many independent initial conditions you can establish in a circuit that has memory elements like capacitor is a memory element if you had inductor inductor would have been a memory element, but the trick is to essentially see how many firstly how many memory elements you have and even more important than that how many independent initial conditions that you can establish in the network. In this case obviously I can establish only one independent initial condition that is the voltage across the capacitor right. So the order of the circuit is 1 so in a first order circuit what is the most relevant parameter for a first order circuit it is a time constant right.

So what is the time constant of this network the time constant τ is R_s plus R_1 parallel R_2 times C right. So it is no doubt that time constant is nothing but our TH Kevinin equivalent resistance times capacitance and what is the condition that we are looking for the condition that we are looking for is the impedance offered by the capacitance what is the impedance offered by the capacitance the impedance offered by the capacitance is 1 by mod of the impedance offered by the capacitance is 1 by ω naught C right. So the voltage drop if you want the voltage drop across the capacitance to be much much lesser than anything that is present in the loop in a Thevenin loop right.



So what is the trick then you all you have to ensure is that the impedance of the capacitor right is much much less than the much much less than the Thevenin resistance right. So essentially you have to ensure ensure let me write it in a new page to ensure negligible voltage drop across the capacitor we need to ensure the the impedance of the capacitor at whatever frequency omega naught right.

To ensure negligible voltage drop across a capacitor,
we need ensure $\left| \frac{1}{j\omega_0 C} \right| \ll R_{th}$

$$\Rightarrow C \gg \frac{1}{\omega_0 R_{th}}$$

$$\Rightarrow \tau \gg \frac{1}{\omega_0}$$

So in other words in this case $1/\omega_0 C$ which is the impedance of the capacitor is much much lesser than the Thevenin equivalent right. The Thevenin resistance of the loop right which essentially means that the constraint that it directly comes out the constraint is the constraint is C should be much much greater than $1/\omega_0 R_{th}$. So this comes out of plain argument right or in other words I can I can also say that this also implies that the time constant of the loop that is C times R_{th} could be much much greater than $1/\omega_0$. So you can approach this problem from multiple dimensions you can approach it from the from the perspective of finding out the time constant and then relating it to $1/\omega_0$ you can approach it from the perspective of sketching out a Thevenin equivalent and then finding out the actual drop across the capacitor and trying to minimize it. You can also say that once I have the time constant right once I have the Thevenin equivalent resistance then I do not even have to I do not even have to do anything I will just set C to be much much greater than $1/\omega_0 R_{th}$ and I am good ok. I will see you in the next lecture. Thank you.