Course name- Analog VLSI Design (108104193)
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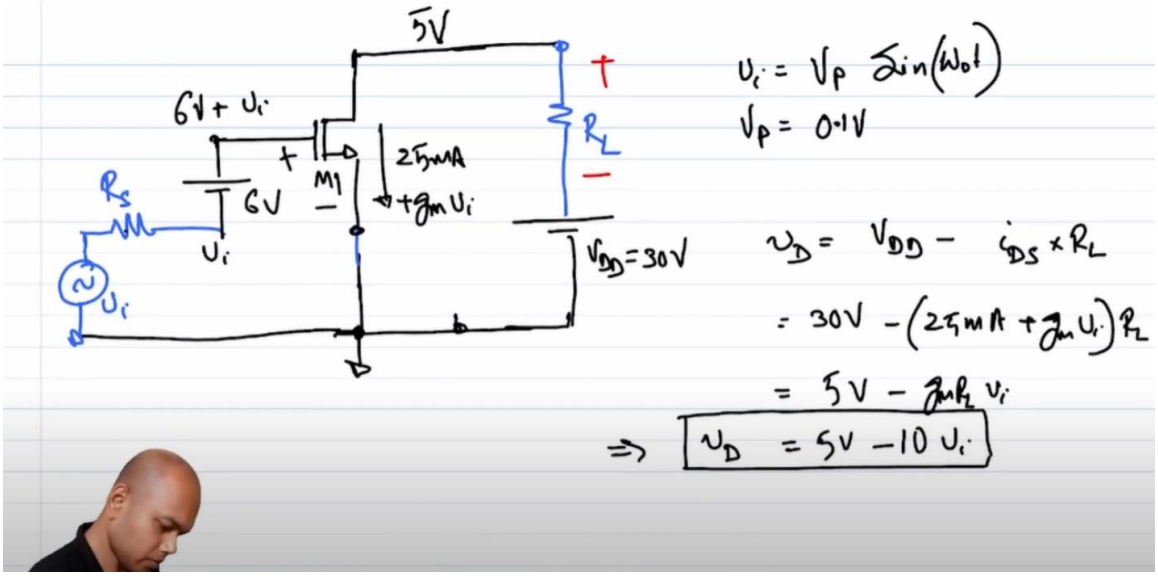
Welcome back. So, I hope you got time to develop an opinion as to what will happen if I apply Now Vi by Vi is equal to 0.1V sine omega t. So, let's start from the input side. So, Vi is 0.1V sine omega t.

So, this since I am not drawing any current through this loop. This voltage will also be Vi. So, the voltage at the gate, the total voltage at the gate of M1 will be 6V plus Vi, right. It will be 6V plus Vi.

If the total voltage is 6V plus Vi, what is the total current flowing through the transistor? The total current flowing through the transistor is 25mA plus gm times Vi, right. So, if this is the total current, what is the total voltage that has developed at the drain? The total voltage will be the quiescent drain voltage, right. So, essentially the total voltage will be Vd. Note again small d, capital D, which means I am trying to figure out the total drain voltage. The total drain voltage is the total current that is Ids or rather let me just say Vdd minus the total current Ids times RL, right.



So, Vdd is 30V, Ids is 25mA plus gm times Vi times RL, which is 1 kilo ohm, which essentially means that this becomes 5V minus gm RL times Vi. What is gm RL? gm RL is nothing but the gain and gain is 10, right. So, this becomes 5V minus 10, right. So, this is the total drain voltage. So, now what do you think is going to happen? Note that your Vi is

0.

1V sin omega t, which essentially means that. So, let me take a different page. So, my foot, so the incremental input is, this is the incremental input, this is time, this goes on, this goes on. So, this is the incremental input Vi. What is the quiescent input? The quiescent input is 6V.

So, this is, so let us say this is 6V, right. I understand this is not to scale, but bear with me. So, this is 0.1V, right. So, this is Vgq, ok.

So, what is the total, now if I sketch with respect to time, with respect to time, if I sketch the total drain voltage, what should I get? So, let me again point out the fact that total drain voltage is 5V minus 10 times Vi, right. So, let us sketch the 5V first. So, let us say this is, use a different color. So, let us say this is Vgq, which is 5V, right. And this is the quiescent.

What is the incremental? The incremental is minus of 10 times Vi, right. So, there are two things to notice here. One is the amplitude of the sinusoid, right. So, if I write it in terms of sinusoid, what do I get? This becomes Vd is equal to 5 volt minus 10 times Vp sin omega 0 t. Note that the amplitude of the sinusoid has gotten multiplied by factor of 10 if the transistor is in saturation, right.

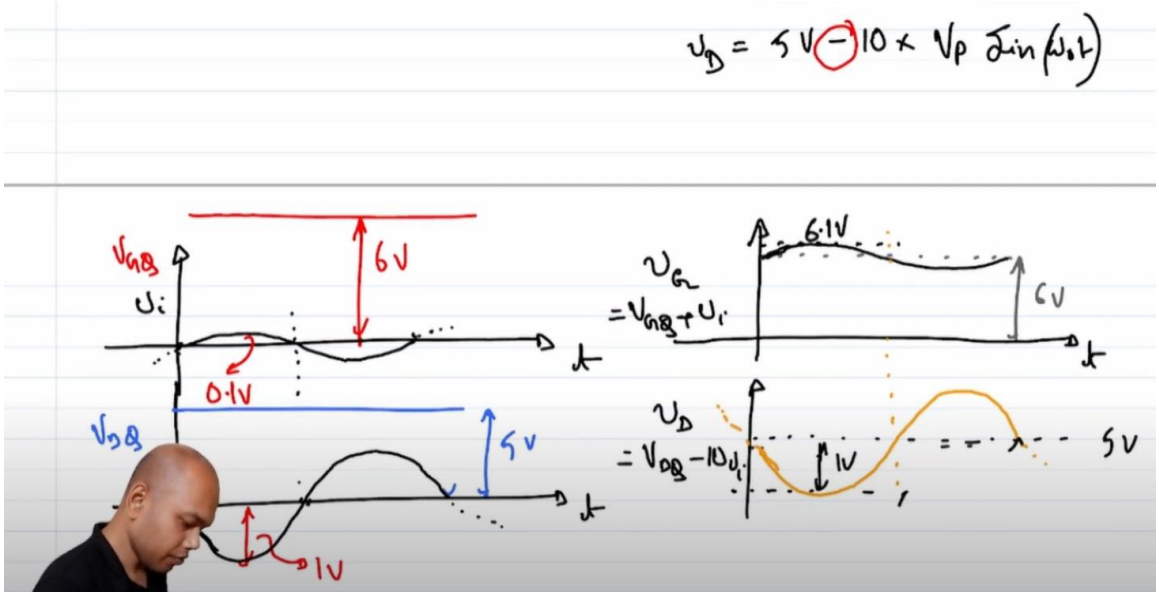
But not only that, there has been a sine reversal, right. There has been a sine reversal and this sine reversal is the consequence of the fact that I am drawing current out of the load island, right. So, how should I sketch this? So, this minus 10 Vp sin omega t should look like 10 times, oh let me make this shallower, otherwise it really does not make too much sense. So, let me make it really shallow, as shallow as I can make without losing the context, right. So, let us say here this is one cycle of that sinusoid and you have repeated cycles.

So, if I make this 10 times bigger and multiply it minus 1 which means I have to flip the sine on the sinusoid. So, if I, let us say this 10 times bigger means something like, something like this. This clearly is not 10 times, but let us say this is 10 times for the time being. So, what will this be? This will be 1 volt. So, clearly this cannot be 5 volt, right.

I mean the way I have sketched it, this is clearly, I mean that I probably will have to bring it bit up, this is 5 volt. Let me bring this further up, let us call this 6 volt, ok. So, now do you see a problem? Clearly there is a problem because now if I see the total gate voltage and the total drain voltage what do I notice? So, the total gate voltage let us say now I am plotting the total gate voltage that is Vg, right, total gate. Total gate is Vgq plus Vi, right. So, the total gate voltage will be some 6 volt, let us say this is a 6 volt line.

On top of that I will have Vi, so this is the total, this is the total gate voltage. And what is the total drain voltage? Again this is we are assuming the transistor is always in saturation and that is why we are drawing all these plots. The total drain voltage is Vgq minus 10 times Vi, right. So, I have some 5 volt line here. So, this is the 5 volt line and I will have, ok.

Fine. So, what do you notice here? You notice clearly that when the input is going high, right, if I go back to this, if I go back to this diagram once again, what am I noticing? The thing that I am noticing is that when the gate voltage is going high, the gate voltage is clearly a sinusoid on top of a DC voltage, right. So, this is my gate voltage. So, when the gate voltage is going high, what is happening to the drain voltage? So, let me remove this. What is happening to the drain voltage? When the gate voltage is going high, the drain voltage is going down. And what is the minimum the drain voltage is going? Or rather what is the, when is the drain voltage going to its minima? The drain voltage is going to its minima when the gate voltage has gone to its maxima, right.



So, when the gate voltage is at its peak that is 1.1 volt, the drain or rather 6.1 volt, what is the drain voltage at? Drain voltage is 5 volt. So, let me just remove this line and just call this a 5 volt line. So, what is this? If this is 1 volt, what is the minimum drain voltage? This is at 4 volt, correct.

So, the drain voltage here is doing just the opposite, the drain voltage is doing this. So, when the gate voltage has gone up to 6.1 volt, the drain voltage has gone down to 4 volts. So, now can you comment if this transistor under this condition at this time juncture, is it in saturation or is it in linear region or triode region? Clearly, the transistor here is not in saturation, it is in linear region, right, because I am not satisfying the condition of Vd

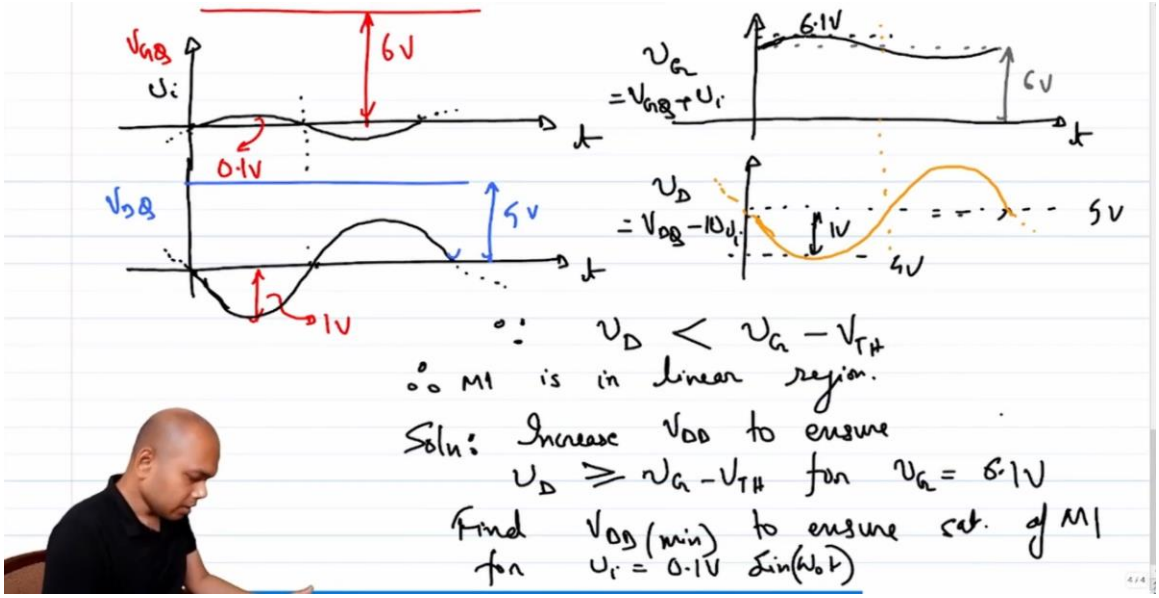
should be greater than Vg minus threshold voltage, right. In other words, the easy way to think about it is that if you know the total gate voltage, you can only allow the drain voltage to go 1 threshold voltage below the gate.

If the drain voltage goes less than 1, more than 1 threshold voltage below the gate, the transistor goes out of saturation, right. So, clearly if in this case, when the input has gone to 6.1 volt, the minimum the gate voltage, the minimum the gate voltage or the drain voltage that is allowed should be 5.1 volt, right. Other than that, you will have a problem, ok.

So, what is the solution? The solution clearly is the same old, same old, the transistor is in triode, right. What we need to do? We need to raise the drain voltage and what is the only handle that we have? The handle that we have is to raise the Vd, right. So, what is the solution? So, in this case, let me write down. Since Vd that is a total drain voltage, since Vd is less than total Vg minus threshold voltage, therefore M1. Therefore, M1 is in previous region.

Solution increase Vdd to ensure Vd is less than Vg minus threshold voltage. Vd is always, what are the, let me just say, to ensure Vd is greater than equal to Vg minus threshold voltage for all values of the input, right. Or what is the worst case situation? The worst case situation is that for the maximum amplitude of the input, right. For Vg is equal to 6.

1 volt, right. So, if you can ensure that, then you are good. So, what is it? So, what will be the value of Vdd if we have to ensure that? So, I leave it up to you to do this exercise, right. Ok. So, let us, so let me write it down. Find Vdd min to ensure saturation of M1 for Vi is equal to 0.



1 volt sin omega 0. Right. Ok. Ok, great. So, now let me ask you one more question. What do you think is going to happen? So, let me copy this figure once again. So, let us assume you have raised the Vdd, right. Let us assume we have raised the Vdd and the transistor is in saturation, which means when this is at 6.

1 volt, this minimum voltage is at 5.1 volt, right. So, this let us assume that we have been able to successfully raise the Vdd, ok. So, now the question is, I mean are we all good? What is that? Is there any issue? So, one might, I mean you might ask is that we took care of the, we took care of the condition when the input was rising, right. So, what about the case when the input is falling, right. So, what about this cycle? What about this cycle? So, what is the, is there a problem if the input goes low? Clearly if the input, when the input is going low, when the gate voltage is going low, what is happening to the drain voltage? When the gate voltage goes down, when the gate voltage is going down, the drain voltage is going up, right.

They are anti-phase, the drain voltage is going up. So, I am increasing the difference between the drain and the gate. So, I am clearly pushing the transistor more and more into saturation. So, getting into saturation is not the problem, but is there a problem on, is there a problem in the input side? As in is it at all possible, is it at all possible that the transistor is getting cut off, right. So, what do you think will be the likely problem? Now, one might say that if we apply, if we apply a negative voltage, negative incremental voltage, right.

So, the gate to source voltage is reducing, right. So, the gate to source voltage is reducing, which essentially means that I am pushing that transistor more and more towards cut off region, right. I am pushing the transistor more and more into cut off region, I am trying by simply reducing the current further and further, right. So, what is the total current? Total current that is Ids, the total current Ids is Ids Q plus incremental current, correct. So, what is the total, what is Ids Q in this case? This is 25 milliamps.

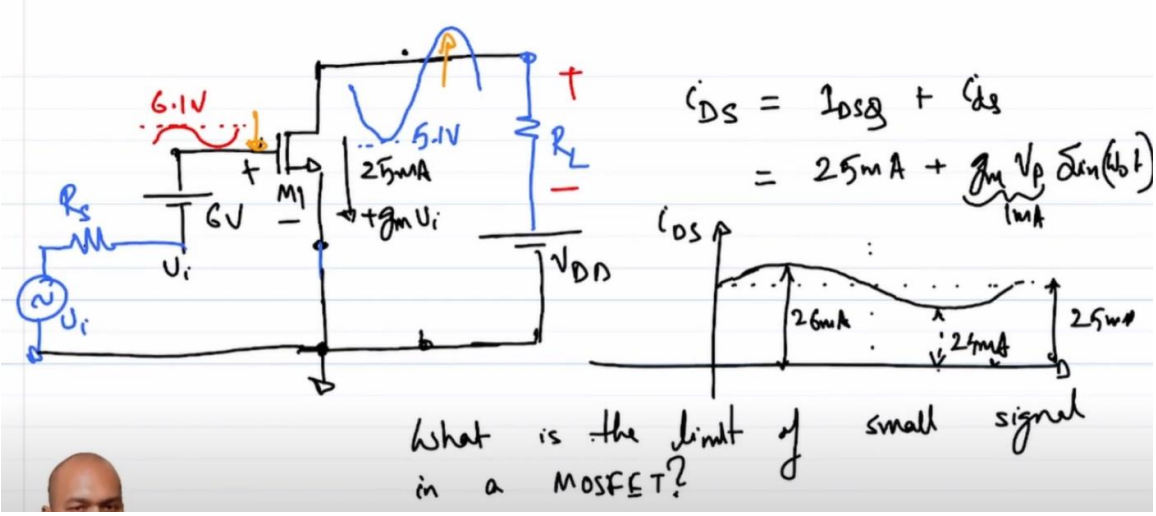
What is the incremental current? Incremental current is gm times Vp sine omega not t. Now, what needs to happen, what needs to happen in order to push, in order to, so rather let me ask you this. What do you think your total Ids will look like? So, if I sketch the total Ids, again total Ids is Ids Q plus gm Vp sine omega not t. So, let us say this is my 25 milliamp line, right.

What is gm? gm is 10 milli Siemens, right. gm is 10 milli Siemens and what is Vp? Vp is 0.1 volt, right. So, what is gm times Vp? 10 milli Siemens times 0.1 volt is 1 milliamps, right.

So, this is 1 milliamps. So, what do you think will your, what do you think your Ids will

look like? Ids essentially will look like this. So, this will go up by 1 milliamps and it will go down by 1 milliamps. So, this is 25 milliamps. So, the minimum current will be 24 milliamps and the maximum current will be 26 milliamps. So, clearly, so clearly we have not, we have not applied a large enough Vp to completely shut the current down, right.

We have only applied, we have only applied a small enough current, a small signal current, right. So, that the current does not change at all, right, ok. So, here in comes another question that we have been avoiding till now that is what is small signal, right. What is the validity of small signal in a or rather what is the limits of small signal, what is the limit of small signal in a MOSMOS? So, the answer to that again one might point out is dependent on architecture, right. So, whatever is small signal for one particular architecture might not be small signal for another architecture, but let us take a vanilla MOSFET into account, right.



Let us take a vanilla MOSFET that has been biased in saturation into account and try to make a case for it, right. So, let us assume that a transistor is in saturation, right. Let us assume the transistor is in saturation and I have biased it such, right. The same thing that we have done till now, right and let us say this is Vgsq and this is Vi and we and this is the Vds is held in such a way that the transistor is in saturation, ok. So, we will try to answer this question in the context of what is small signal as far as the current and the voltage relationships are concerned, right.

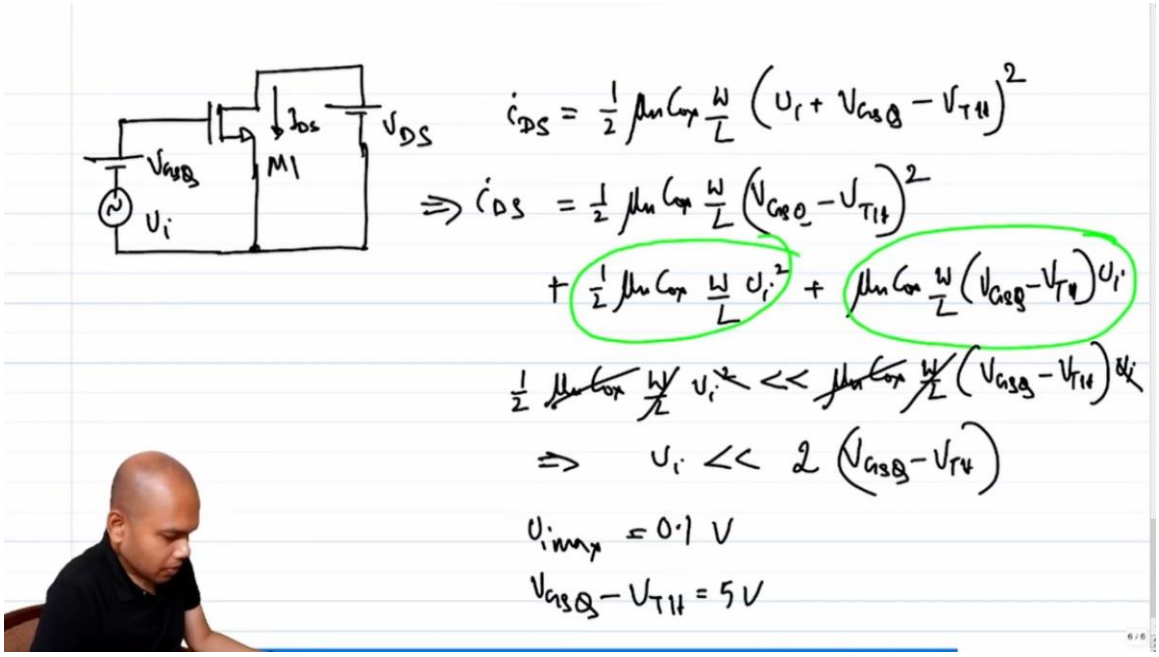
So, in the context of Idsq or in the context of Ids versus the input signal, right. So, let us quickly do that. So, what is Ids? What is the total Ids? Total Ids is half U n C ox W over L Di plus Vgsq minus ratio of voltage whole square which is half U n C ox W over L. Vgsq minus threshold voltage whole square plus half U n C ox W over L Vi square plus U n C ox W over L Vgsq minus threshold voltage.

Right. So, this is what Ids is and when we say that we are doing small signal, what are you

saying? We are saying that we are neglecting this term with respect to this term. Which essentially means that we are assuming half U n C ox W over L Vi square is much, much less than U n C ox W over L Vgsq minus threshold voltage times Vi. So, these go off, this goes off, one Vi cancels, right. So, essentially we are assuming that Vi should be much, much less than twice of Vgsq.

Vgsq minus the threshold voltage, right. So, as long as we can satisfy that Vi is much, much lesser than twice the overdrive, right. Yeah, we are good, right. So, this is as far as the constraint on small signal is concerned, right. So, is the small signal constraint valid in the case, in our case, I mean for example, it is a small signal constraint valid when Vi was 0.

1 sin omega t. So, in our case what was Vi? Vi max was 100 milli volt. So, Vi max was 0.1 volt. And what was overdrive? Vgsq minus threshold voltage was 5 volt.



And clearly this condition was satisfied. So, we could safely assume that a small signal approximations are well and good. So, to quickly recap, what did we do in today's lecture? We saw that we started off and saw that what do we need to do in order to ensure that the MOSFET is in saturation provided obviously the input side has been taken care, right. So, we needed to apply a higher drain, higher VDD, higher supply voltage on the drain side in order to keep the transistor in saturation. Then we said that what we need to do, I mean is something change, does something change if I apply a sinusoidal input. So, clearly if we apply a sinusoidal input, then it is likely that the transistor might go out of saturation.

If you bias the quiescent condition, if you bias the transistor at quiescent condition just at the edge of saturation because as the signal swings, the drain voltage will also swing. And as it turns out if the gate voltage increases, the drain voltage decreases and the transistor goes closer and closer towards linear region and away from saturation. So, you need to keep some margin and ensure that under quiescent condition, you do not bias your transistor just at the edge, right. And then we say, then we try to investigate what happens when the input goes down. When the input goes down clearly or the input decreases, when the Vg decreases, I should not say input because input can be applied anywhere.

When the gate voltage decreases, the drain voltage increases which means the transistor is safely into saturation. However, there is a chance that the transistor current might reduce so much that it completely shuts off, right. So, we need to be careful and see whether that is valid or not and we saw that under the condition we, under the condition that we used, it seems to be ok, right. Then we essentially said that what needs to be done in order to validate, in order to first validate whether the approximate, the small signal approximation that we have been so liberally using in case of a MOSFET is actually valid or not. We had done this limit calculation in case of a diode which turned out to be twice that of the thermal voltage and we did the same thing here and what did we find? We found that as long as far as the IDS versus VGS characteristics is concerned, the small signal approximation holds good as long as the applied gate to source, incremental gate to source voltage, right.

I should actually be more careful and let me just say that this is, let me instead of putting Vi, let me make it more explicit, let me call it incremental VGS because the input has been applied between the gate and the source. So, let me modify this as VGS, small vgs, small vgs. So, we saw that as long as the incremental gate to source voltage is much much less than twice the overdrive of the transistor, the approximation of small signal is valid, right. So, let us stop here and see you in the next class. Thank you.