Integrated Circuits and Applications
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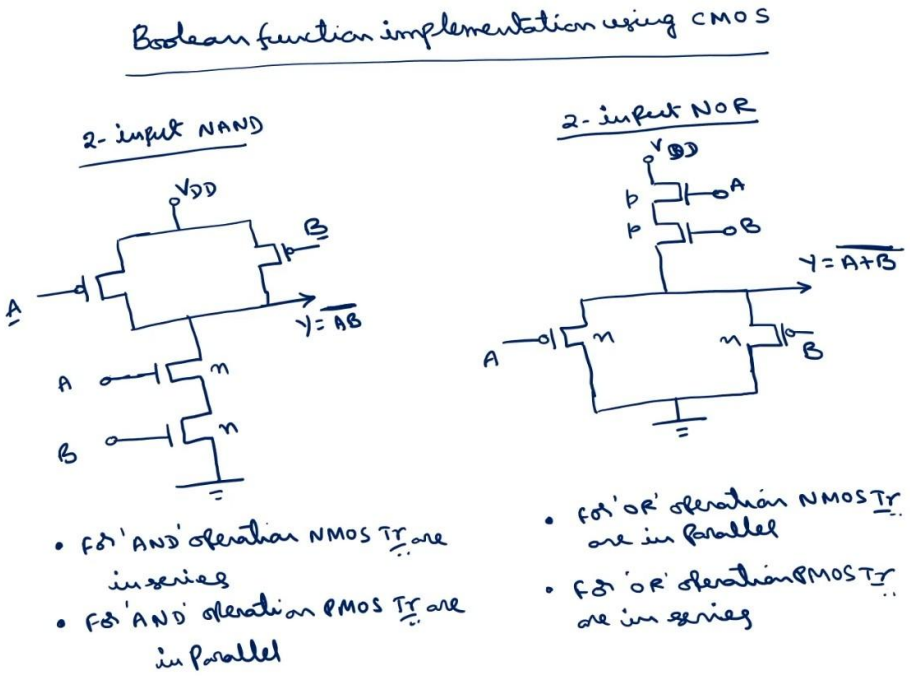
Digital CMOS Circuits
Lecture – 44
Boolean function Realization using CMOS & Sizing

In the last lectures, we have discussed about CMOS inverter, CMOS NAND gate and CMOS NOR gate. Today we will discuss how to implement any Boolean function using CMOS devices. So, we know the two input NAND gate circuit and two input NOR gate circuit. By observing these circuits we can generalize the relation to any Boolean function. So, in case of two input NAND gate, PMOS transistors will be in parallel, NMOS will be in series. Whereas in NOR, it is the opposite.

PMOS will be in series, NMOS will be in parallel. By observing these two circuits, we can see that here, if I neglect about this complement operation, let us assume that this is AND operation only. So, for AND operation, these NMOS transistors are in series. Whereas PMOS transistors are in parallel.



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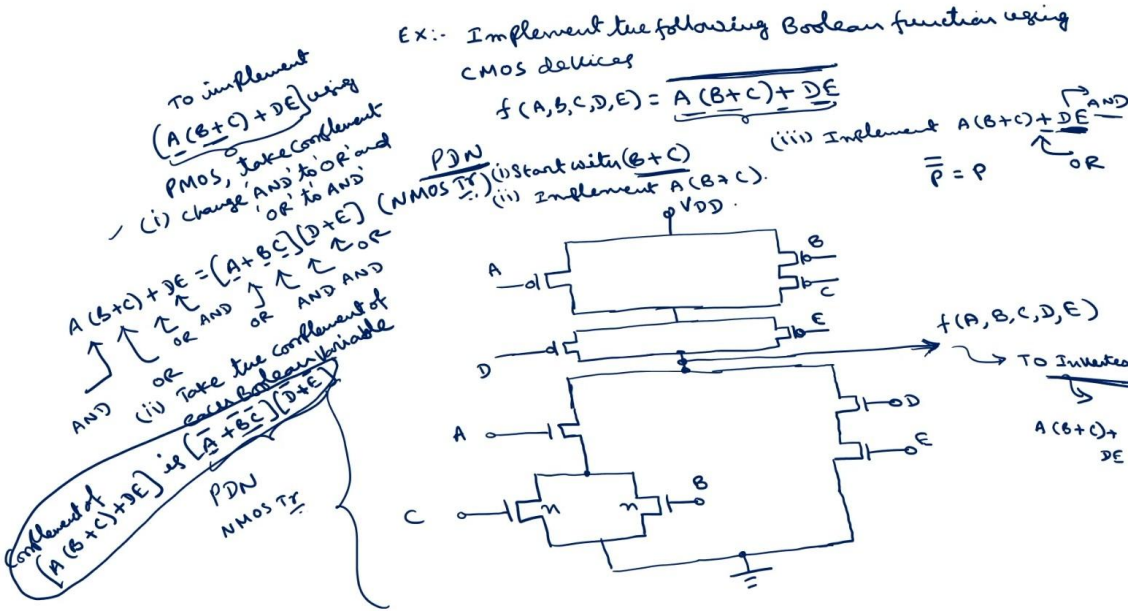
Whereas, here, if I forget about this complement operation for OR operation, these are two NMOS transistors, here two PMOS transistors. NMOS transistors are in parallel, and PMOS transistors are in series. Based on this observation, we can implement any Boolean function using CMOS devices. Let us take an example. $F(A,B,C,D,E) = \overline{A(B+C)+DE}$.

For the sake of simplicity, let us take as whole bar. So, that we need to consider only the Boolean expression, which is present in without bar. If you want to get this without bar, you can come connect a inverter at the end of the circuit. So, here you can see that there is one AND operation here, there is another AND operation, one OR operation, another OR operation. First, you have to start with $B + C$, and you consider only first pull down network.

So, in the pull down network $B + C$ for OR operation, NMOS transistors will be in parallel because in the pull down network, we will be having only NMOS transistors. So, this is B, this is C, these are NMOS transistors you have to connect in parallel to get the OR operation. Then you implement $A(B + C)$. So, for this, $B + C$ is AND operation. So, you have to connect A in series with $B + C$.



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Then implement $A(B + C) + DE$ means OR operation this DE will be again in series

because D and E here the operation is AND operation, here the operation is OR operation. So, AND operation means these two will be in series, OR operation means this DE will be in parallel with $A(B + C)$. Means here there will be a parallel path in which again D and E, AND operation they will be in series. This part will be grounded this is the complete pull down network, which consists of only NMOS transistors. Now, coming for the PMOS, in order to get the PMOS, we can reverse these operations, or we can take the complement of this $A(B + C) + DE$.

$A(B + C) + DE$, this is the one which we have implemented using NMOS transistors in order to obtain using PMOS this expression using PMOS take complement. So, you might have studied in your digital circuits to get the complement of any Boolean function you have to do two operations. One is you have to change the AND operation to OR operation; OR operation to AND operation. So, the first one is change AND to OR and OR to AND. So, here this OR becomes AND this AND becomes OR.

So, this $A(B + C) + DE$ will become $A + BC$, this OR becomes AND into $D + E$. So, this AND operation you have changed to OR, this OR operation you have changed to AND, this OR operation you have changed to AND, this AND operation you have changed to OR. The first step to get the complement of any Boolean function is you have to exchange AND and OR operations. Then, the second step is take the complement of each Boolean variable. So, that the complement of this $A(B + C) + DE$ will become $\bar{A}$ this you have take the complements of each and every element plus $\bar{B}$ $\bar{C}$ into $\bar{D}$ plus $\bar{E}$.

This is the $(A(B + C) + DE)'$. This is how you can obtain the complement. Now, the pull up network relation consists of the relation of the complement of the given Boolean function. So, this complement you have to implement by using PMOS. So, again this OR operation means parallel, AND operation means in series.

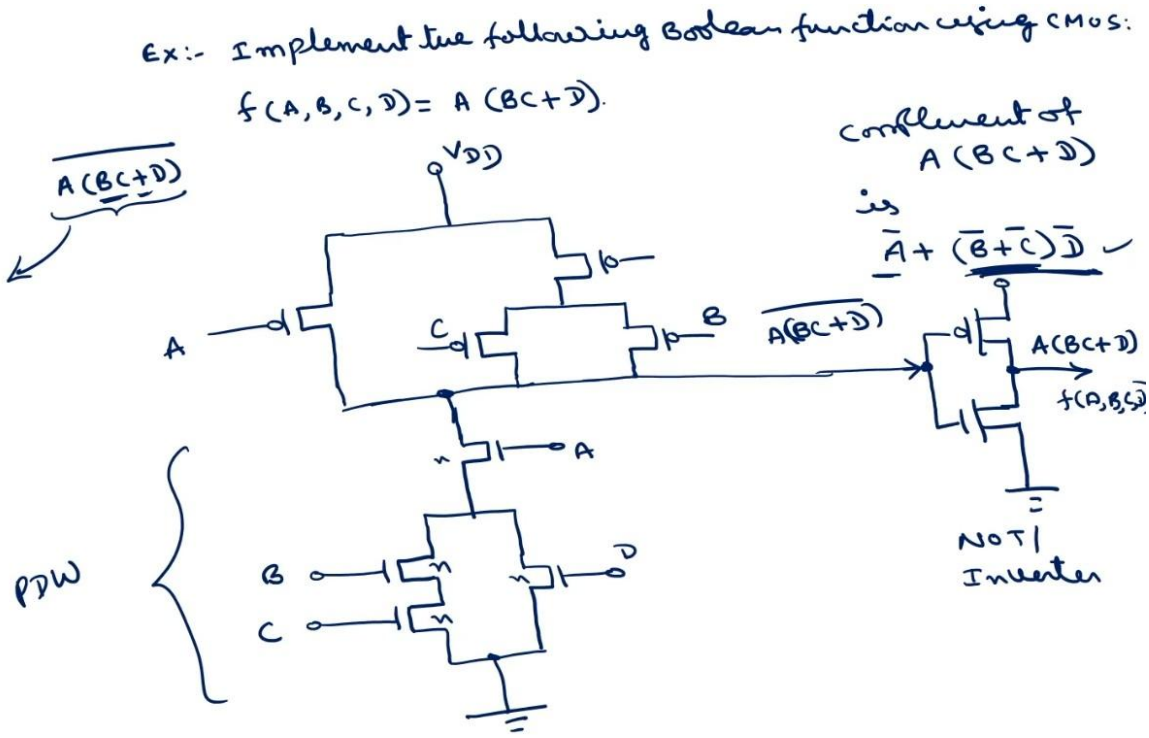
So, how to implement this? $A + \bar{B}\bar{C}$, of course; here, we are going to use NMOS transistors, BC will be in series. This is this $\bar{B}$, $\bar{C}$, then $\bar{A}$ in parallel because you are taking the complement, you can follow the same end logic. For this again $D + \bar{E}$ in series, these two will be connected. This is D, this is E because of these bubbles they are bars, and here we are going to connect to VDD. Here at this junction, we will get the output F(A, B, C, D, E).

If I do not want this complement, then you can connect this to inverter circuit, which we know the output of the inverter will be now simply $A(B + C) + DE$. If want with complement, you can take the output here, if I want without complement you can pass this output through the inverter then you can take the output of the inverter that will be without complement. Because complement of complement is same value only, because

you have P double complement is P itself, and this inverter will complement the given input. So, this is the relation of the given Boolean function $A(B + C) + DE$.

Now, let us take another example. $F(A, B, C, D)$, 4 variables only is equal to $A(BC + D)$. Here, I don't have the complement. So, let us first implement the $\overline{A(BC + D)}$, which is with complement, then you pass through the NOT gate. Then what is the implementation of $\overline{A(BC + D)}$, and you have to consider this part only? So, in the pull down network, B, C AND operation means series.

D is OR operation. So, in parallel with this, there will be D. Then whole thing with A AND operation. So, this is in series. This is pull down network, and all the transistors are NMOS. Then, the pull up network will be you have to take the complement of $A(BC + D)$, change the AND to R, R to AND, then take the complement of individual elements.



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This is the complement of this. Then how to implement this $\bar{B}\ \bar{C}$ in series, means OR operation means in parallel in series with D. This is B C. So, $\bar{B} + \bar{C}$, this is D. So, $(\bar{B} + \bar{C})D$.

This $\bar{A}$ plus OR operation is there you have to connect in parallel. This will be connected to VDD; this will be connected to ground. Here, this will generate $\overline{A(BC+D)}$. You get $A(BC+D)$ itself. You connect this to NOT gate. Now, this will be $A(BC+D)$.

This is NOT gate or inverter. This is the complete relation of the Boolean function $F(A,B,C,D) = A(BC+D)$. Now, the last topic is how to size the transistors so that they can have the delays which is equivalent to that of the inverter delays transistor sizing. For example, if I take this the first example, this function. So, the circuit diagram of this one we have already derived.

So, for better explanation, I am drawing this circuit again. This is pull down network, and pull up network is just opposite to this. This is DE, this is BC, this is E. Now, I want to make the delay of this one same as that of the inverter. So, we have derived the propagation delays of t_{PHL} and t_{PLH} in the previous lectures.

And we have also shown that $t_{PLH} > t_{PHL}$. So, the reason is so, in case of low to high transition, this P type transistor will be involved, and the mobility of holes is less than that of the electrons. As a result of that, this will take more time to change from low to high. Assuming that if I take the same $\frac{W}{L}$ ratios. Now, in order to make this is $t_{PHL} = t_{PLH}$, we can size the transistors accordingly. L. Anyhow, we are going to keep it fixed because if I reduce the L below a value, then there will be some short channel effects. So, forget about this L then W. If I choose this twice the W as the width of NMOS transistor, then these two will be equal because the mobility of holes is approximately twice that of the electrons.

So, this is the normal practice will take this twice W this is W. So, that t_{PHL} and t_{PLH} will be equal, and this value depends upon the W and Cox lot of parameters because this is given by 2.2 times and $2 \times 0.693 R_p C_{out}$ or $R_n c_{out}$. Now, here we are choosing this R_p as a twice R_n. So, we will get the same value.

Now, this delay will be more than that of the delay of the inverter because here, many gates are involved. Because of that, the delay of this one is readily greater than delay, delay of the inverter. Now, the problem here is you have to size the transistors of this Boolean function such that so these two will have same delay. For that, if I consider the pull up network, only one p mass transistor is here with a 2W width whereas, here, there are 5 PMOS transistors, then what should be the size of this 5 PMOS transistors? So, that the equivalent width will be equal to 2W.

Similarly, if I take the n mass transistor the width is W. Here, we have 5 NMOS transistors. How to size this 5 NMOS transistors such that the width of these two will be

equal. We know that this resistance is inversely proportional to the width. We have discussed this in the earlier lectures. The relation for the R will be in the form of R_n is nothing, but $\frac{1}{\mu_n C_{ox}(\frac{W}{L})_n[V_{DD}-V_{T,n}]}$, the threshold voltage of NMOS transistor. So, we can see that here R_n is inversely proportional to W. Similarly, R_p is also inversely proportional.

So, in general, R is inversely proportional to W. So, if I have this width of any transistor is KW implies the resistance will be $\frac{R}{K}$. This is clear if I multiply the width by K, then the resistance because inversely proportional will be divided by K. This is one of the important result we are going to use to size the transistors.

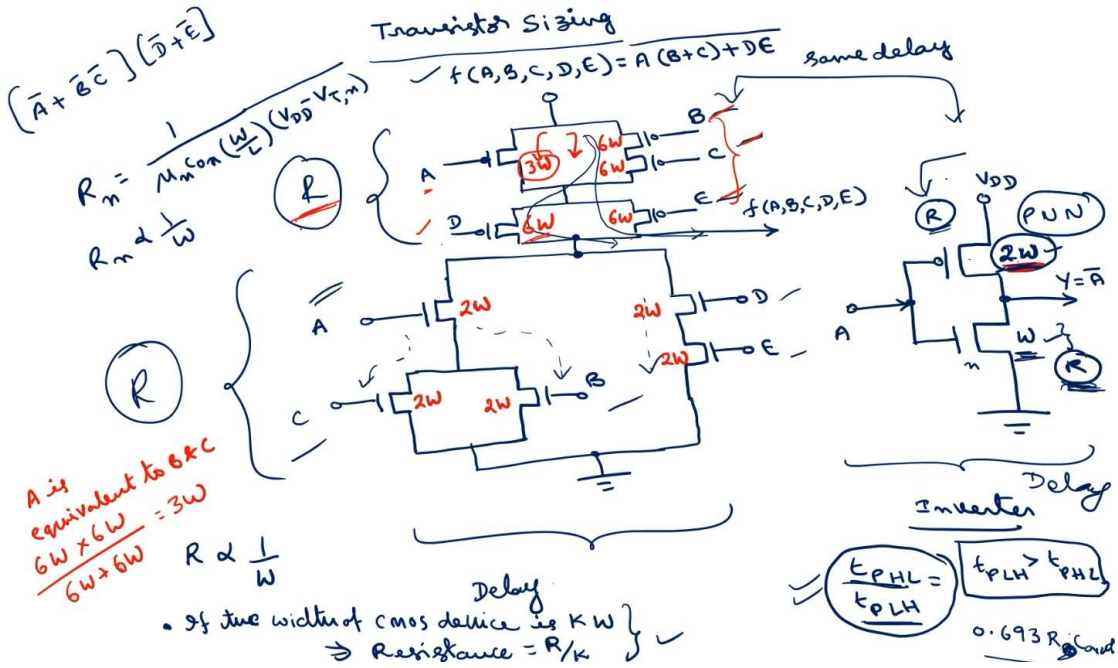
Now, coming for this PMOS sizing. So, what are the worst case propagation delays? As we have discussed in the previous lectures that you have to consider the worst case propagation delays for a better design because once if you design a circuit for worst case conditions then it will work for the best case conditions, also. So, what is the worst case delay in this case? BCE if these three are in series then it is worst case delay or DCD. This is BCE this is the series this one or BCD. Now, because this is the twice the width. So, here, the resistances will be $\frac{R}{K}$. In general, you have to find out the value of the K.

So, that the equivalent resistance will be R. So, basically here, if this resistance is equivalent to R this 2W also will be equivalent to R resistance. Only then, only you will get a $t_{PHL} = t_{PLH}$. So, if I increase the width of this PMOS transistor twice that of the width of the NMOS transistor then both will give the same resistance as a result of that in this this R_p will be no more R_p or R_n it is simply RC_{out}. So, that the propagation delay of low to high or high to low will be same, the effective resistance should be R. So, this entire network should have effective resistance of R this entire network should have effective resistance of R.

So, if I assume that the resistance of B and C E, this is equal to here because this is multiplied with 2 here, this will be divided by K, this is $\frac{2R}{K}$. If I consider either this path or this path $\frac{2R}{K}+\frac{2R}{K}+\frac{2R}{K}$, this $\frac{2R}{K}$ is corresponding to B this $\frac{2R}{K}$ is corresponding to C this $\frac{2R}{K}$ is corresponding to E this should be equal to the equivalent resistance of R. The effective resistance should be R for both pull down network as well as pull up network. So, what will be this R R get cancelled? K is LCM from this, we will get $K = 6$. That means, the widths of this B, C and E should be 6W, 6W, 6W. This is 2W.

So, if this is 6W, 6W, 6W, then the resultant resistance becomes R. Here, this 2W resistance is R. So, you see the size of B C and E. Now, what about D B C E or B C D is

two worst case paths. So, in B, C, E, if we have 6, 6, 6 means, this also should be 6W, then only both will give the same equal resistance. Now, if I consider B C E, it is giving resistance of R means if I consider D size as 6W, then only B C and D also will give the equivalent resistance of R that is why the size of D also should be 6W. Now, what about the size of A we can see that these two paths are in parallel means this A is equivalent to B and C two resistors if you connect in series the resultant resistance is 2R.



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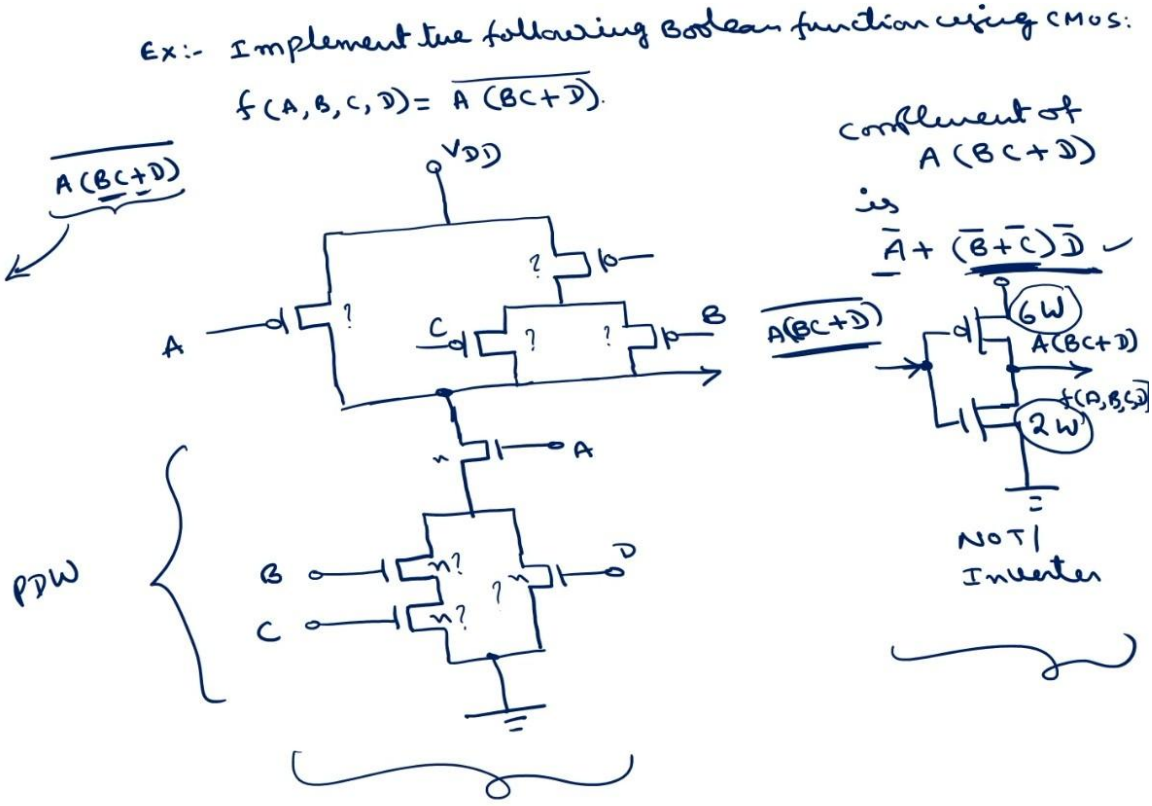
So, this should be equivalent to 3W because the resultant of this 6W 6W in series resistance are in series means we have to add widths are in series means we have to take the parallel combination $\frac{6W \times 6W}{6W+6W} = 3W$. So, the size of this one is 3W this is about the pull up network. Now, coming for the pull down network or NMOS sizing here what is worst path we have three paths, either D E or A B or A C A C in any case two transistors will be in series, either D E or A B or A C D E A B A C. So, what is the resistance here this will be $\frac{R}{K}$ because this resistance is directly R this is already having the equivalent resistance of R only whereas, this will be having twice W that is why you are taking here 2R, but in the computation of this NMOS sizes you have take R. So, $R + K + R + K = R$ because the equivalent resistance should be R implies $K = 2$.

That means, whether this path or this path or this path all are having only two transistors

in series. So, all the transistors should have a width of twice the W. So, this should have 2W, 2W, 2W this is how we can size the transistors to have the equal delay when compare with the inverter which is having both t_{PHL} and t_{PLH} are equal. In a similar way you can size the second problem also. Let us consider here also the if the implementation is up to $\overline{A(BC+D)}$, let us forget about this.

Now, you size this which is equivalent to the size of the CMOS inverter let us forget about this now. So, this output is now this is bar. Now this is CMOS inverter. So, let us assume that this is 6W, 2W. So, I want the size of this one as 6W, I want the size of this one as 2W. So, to meet this requirements what are the sizes of this? This I think I have given as a one of the exercise problems in the assignment ok.



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So, you can do in a similar manner, ok. So, this is all about this course, integrated circuits and applications. So, if you have any doubts, you can ask in the faculty forum, and the final examination will be similar to that of the assignment pattern. So, we will be having similar types of questions which I have given in the assignment, and thank you for your cooperation and all the best for your final examinations.