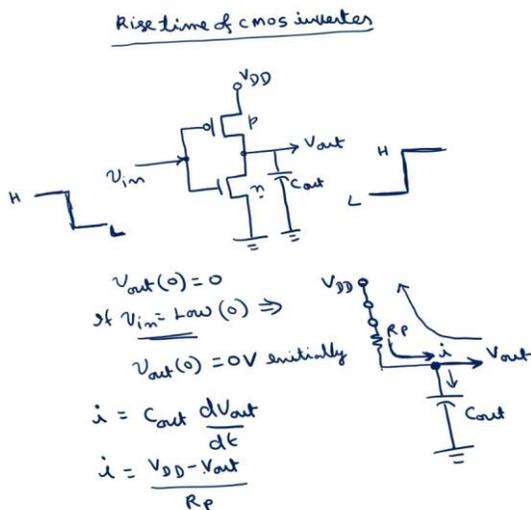


**Integrated Circuits and Applications**  
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**Digital CMOS Circuits**  
**Lecture – 42**  
**CMOS NAND Gate**

So, in the last lecture, we have derived the expression for fall time of CMOS inverter. Today, we will derive the expression for rise time of CMOS inverter. So, in order to find out the rise time, the output has to change from low to high. So, that input will be high to low. So, initially, the output was low, then it will change to high if the input changes from high to low; that is, the initial condition is  $v_{out}$  of 0 initial condition it was, 0. So, if the input is high to low means if the input is low, what happens to this PMOS and what happens to NMOS? Logic 0 implies  $V_{GS}$  of this NMOS is 0.

So, it will be off,  $V_{GS}$  of PMOS is negative, it will be on as you have discussed earlier. So, this equivalent circuit will be here. There is a short circuit, but there will be resistance  $R_p$ , which is the on resistance; here, we have a capacitor  $C_{out}$  and here, this part is open circuit to ground this. I am removing because of the open circuit. So, here the point where the output is taken  $v_{out}$  and the capacitor is also connected here. So, when the input is low, output was initially at 0V; now, it will charges towards  $V_{CC}$ , the charges towards  $V_{DD}$ .



So, what is the expression for this current? If I call this current as  $i$ , then  $i$  is equal to across this capacitor  $v_{out}$  minus 0. So, this is  $i = C_{out} \frac{dv_{out}}{dt}$ ; this is positive sign because direction of the current is from  $v_{out}$  to ground. In the previous case, the direction of the current was opposite. So, we have got minus sign. This is one expression for  $i$  in terms of  $v_{out}$  and  $C_{out}$ . And if I consider from this  $V_{DD}$  to this  $v_{out}$  and this  $R_p$  is the resistance the current through this  $R_p$  is also  $i$ .

So, I also can be expressed as direction is from  $V_{DD}$  to  $v_{out}$ . So,  $\frac{V_{DD}-v_{out}}{R_p}$ . So, if we equate these two, then the difference equation will be  $C_{out} \frac{dv_{out}(t)}{dt} = \frac{V_{DD}-v_{out}(t)}{R_p}$ . The first order differential equation with the initial condition of  $v_{out}(0) = 0$ . By solving this differential equation, we can obtain the expression for the  $v_{out}(t)$  as here also all these are function of  $t$ . I am not writing is equal to  $V_{DD}(1 - e^{-\frac{t}{\tau_p}})$ .

The solution of the first order equations you might have studied in your mathematics. So, where  $\tau_p = C_{out}R_p$ , which is the time constant of PMOS device. Now, we will define this rise time as initially 0; now, it will increase to  $V_{DD}$ . So, this is  $V_{DD}$ , this is  $v_{out}(t)$ , this is  $t$  output will change from low to high. So, the rise time is defined as the time taken to change from 10% to 90% of the  $V_{DD}$ .

$$C_{out} \frac{dV_{out}(t)}{dt} = \frac{V_{DD} - V_{out}(t)}{R_p} \leftarrow \text{first order differential equation } v_{out}(0) = 0$$

Solving this differential equation

$$V_{out}(t) = V_{DD} \left[ 1 - e^{-t/\tau_p} \right]; \text{ where } \tau_p = R_p C_{out}$$

= Time constant of PMOS device

At  $t = t_x$ ;  $V_{out}(t) = 0.1V_{DD}$

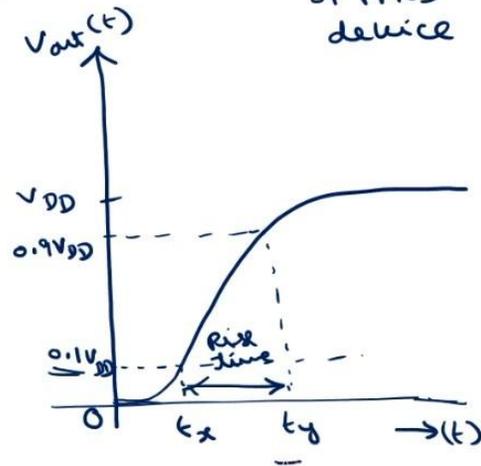
$$0.1V_{DD} = V_{DD} \left[ 1 - e^{-t_x/\tau_p} \right]$$

$$\Rightarrow e^{-t_x/\tau_p} = 1 - 0.1 = 0.9$$

$$-\frac{t_x}{\tau_p} = \ln(0.9)$$

$$t_x = -\tau_p \ln(0.9)$$

$$\Rightarrow t_x = \tau_p \ln\left(\frac{1}{0.9}\right) \dots (1)$$



(Refer to the slide at 09:44)

This if I call as  $0.1V_{DD}$ , we call this as time  $t_x$ , this you call as  $0.9V_{DD}$  corresponding time if you call as  $t_y$ , then this time difference is called as rise time. So, in this expression, if I substitute  $t = t_x$ , what is  $v_{out}(t) = 0.1V_{DD}$ . We substitute this in this

expression  $0.1V_{DD} = V_{DD} \left( 1 - e^{-\frac{t_x}{\tau_p}} \right) \Rightarrow e^{-\frac{t_x}{\tau_p}} = 1 - 0.1 = 0.9 \Rightarrow -\frac{t_x}{\tau_p} = \ln(0.9) \Rightarrow$

$t_x = -\tau_p \ln(0.9)$ . This can also be expressed as  $\tau_p \ln\left(\frac{1}{0.9}\right)$ ; this is one expression by substituting this condition. The second condition is at  $t = t_y$ ,  $v_{out}(t) = 0.9V_{DD}$ . We

substitute this  $0.9V_{DD} = V_{DD} \left( 1 - e^{-\frac{t_y}{\tau_p}} \right) \Rightarrow e^{-\frac{t_y}{\tau_p}} = 1 - 0.9 = 0.1 \Rightarrow -\frac{t_y}{\tau_p} = \ln(0.1) \Rightarrow$

$t_x = -\tau_p \ln(0.1)$  0.9, if we take the minus sign this becomes  $\tau_p \ln\left(\frac{1}{0.1}\right)$ . See equation 2.

Rise time is defined as  $t_y - t_x$ . This is  $\tau_p \ln\left(\frac{1}{0.1}\right) - \tau_p \ln\left(\frac{1}{0.9}\right)$ . So,  $\tau_p$  is common

logarithm of a-b is equal to  $\log a$  by  $b$ . We will get  $\ln\left(\frac{0.9}{0.1}\right)$ , which is 9 is equal to  $2.2\tau_p$ .

This can also be called as sometimes time taken to change from low to high. So, we have

got fall time as  $2.2\tau_p$  also called as high to low. One important observation here is between these two, which one is larger. Here,  $\tau_p = C_{out}R_p$ , and  $\tau_n = C_{out}R_n$ . As I have discussed earlier that  $R_p > R_n$  because the mobility of holes is less than mobility of electrons.

So, the resistance of holes is more than resistance of n-wars, resistance of p type device is more than resistance of n type device. So, between this  $\tau_p$  and  $\tau_n$ ,  $\tau_p > \tau_n \Rightarrow t_r > t_f$ . So, you see the transient analysis of CMOS inverter. In this, we have derived this both rise time as well as the fall time. Sometimes, you will define propagation delay of CMOS inverter.

- At  $t = t_y$ ;  $V_{out}(t) = 0.9V_{DD}$

$$0.9V_{DD} = V_{DD} [1 - e^{-t_y/\tau_p}]$$

$$e^{-t_y/\tau_p} = 0.1 \Rightarrow t_y = -\tau_p \ln(0.1)$$

$$\Rightarrow t_y = \tau_p \ln\left(\frac{1}{0.1}\right) \dots (iv)$$

$$t_n = t_y - t_a = \tau_p \ln\left(\frac{1}{0.1}\right) - \tau_p \ln\left(\frac{1}{0.9}\right)$$

$$= \tau_p \ln\left(\frac{0.9}{0.1}\right) = 2.2\tau_p$$

$\therefore$   $t_n = 2.2\tau_p = t_{LH}$        $\tau_p = C_{out}R_p$

$t_f = 2.2\tau_n = t_{HL}$        $\tau_n = C_{out}R_n$

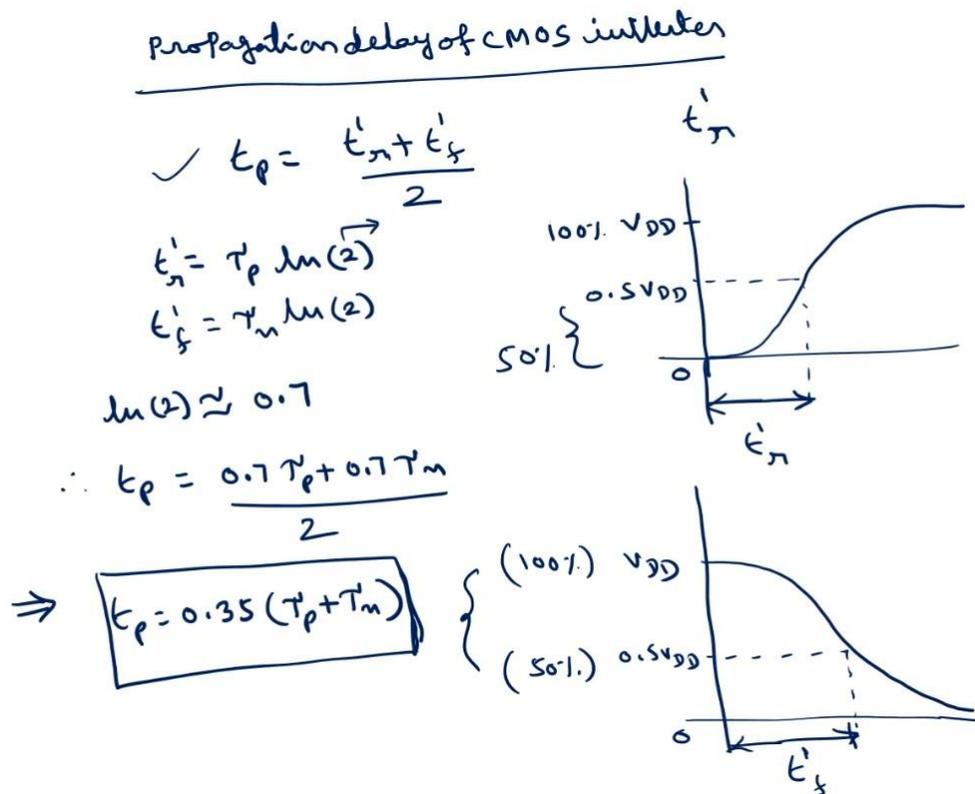
Since  $R_p > R_n \Rightarrow \tau_p > \tau_n$

$\Rightarrow$   $t_r > t_f$

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So,  $t_p = \frac{t_r + t_f}{2}$ , it is average of rise and fall times, but here we will consider this T rise time and T fall time in a different way that is I am calling as a  $t'_r$  and  $t'_p$ . So, is actually the time taken to change from 0 to 50% instead of taking from 10 to 90%. If this is  $V_{DD}$ , this is 0; this is 100%, 50% means  $0.5 V_{DD}$ , this is 50%. So, this total time from 0 to 50% this I am calling as  $t'_r$ .

Similarly, T fall time dash and this is  $V_{DD}$ , this is 0 this is  $0.5V_{DD}$ , this is 100%, this is 50%, this time we are calling as T fall time dash and the average of this is defined as propagation delay. You can easily see that here: instead of substituting this as  $0.9V_{DD}$ , we will take as  $0.5V_{DD}$ . So, with these changes, we can easily derive the expression for  $t'_r$  as tau p. There we have got log 9, now we will get as log 2. By using this definition of 0 to 50% we will get log 2 here this was 9 if I consider from 10% to 90%. Similarly, fall time, it was  $\tau_n \log 9$ , if I consider from 10% to 90% if, I consider from 100% to 50% this 100% to 50% then it will be 2. So, this is log 2 value is approximately equal to 0.7. So, therefore,  $\tau_p = \frac{0.7\tau_p + 0.7\tau_n}{2} \Rightarrow \tau_p = 0.35(\tau_p + \tau_n)$ . This is a expression for the propagation delay of CMOS inverter.

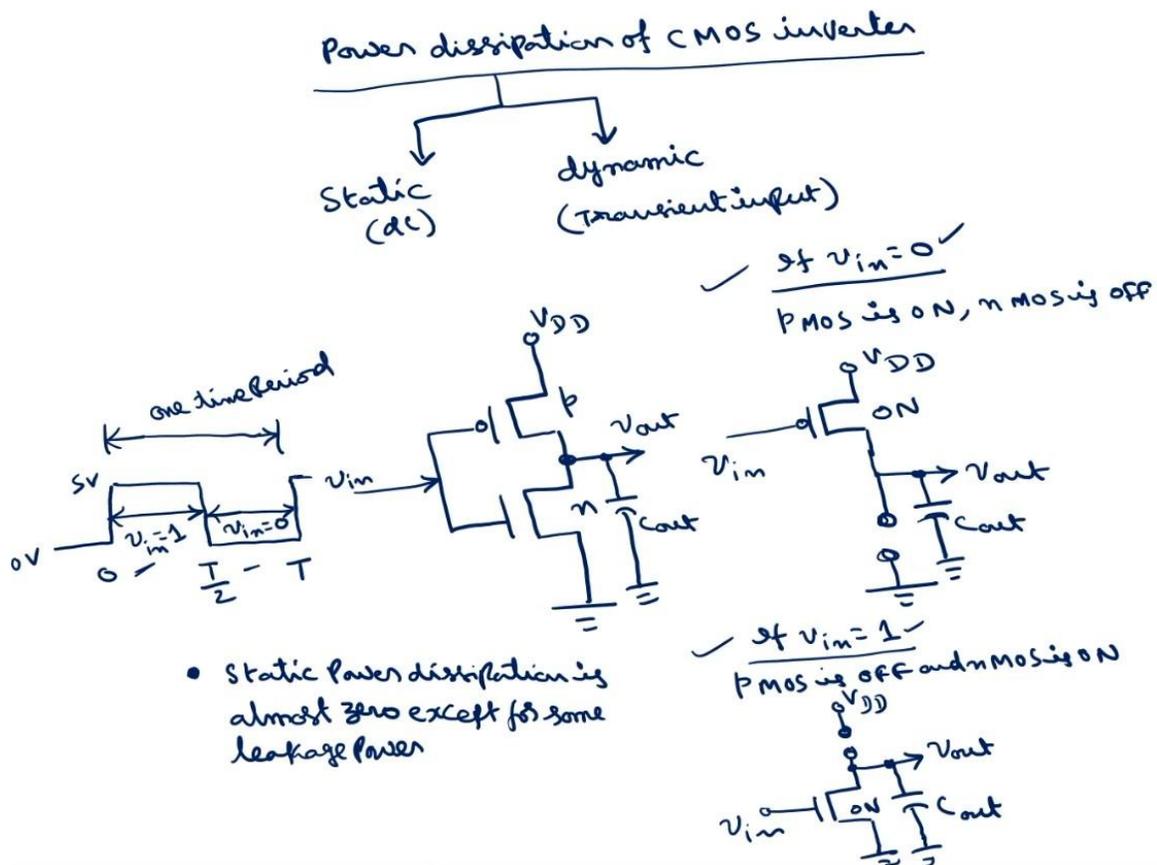


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For any digital circuits, the important parameters are the speed, which is inversely proportional to propagation delay, and the other one is power consumption or power dissipation. Now, what is the power dissipation of CMOS inverter? We have two types of the power dissipation: one is called static due to DC another is called dynamic due to transient input. So, if I take this CMOS inverter. If  $v_{in}$  is 0, the logic 0 output is logic 1. So, what happens to this PMOS and NMOS, as we have discussed earlier?

So, the PMOS is ON, NMOS is OFF as a result of that the equivalent circuit will be something like. If  $v_{in}$  is logic 1, that is  $V_{DD}$ , this is logic 0, this is logic 1, then reverse PMOS is OFF, and NMOS is ON. And what will be the equivalent circuit here? This will be open circuited where this one will be on. And, of course, we have capacitor  $C_{out}$  in case of the transient input. If I consider the DC, then the capacitance will not be present.

So, you can see that in any case, there is a open circuit in the circuit there is a open circuit either in the pull up network or pull down network. And for DC, there is no capacitor. So, because of that, the static power dissipation is almost 0 except for that there is some leakage per except for some leakage per. This is one of the important advantage of the CMOS circuit. Whereas, if you consider only the PMOS circuits or only the NMOS circuits, there will be some static power dissipation, whereas, in the CMOS circuit, static power dissipation is almost negligible.



(Refer to the slide at 24:19)

Now, the maximum portion of the power dissipation is due to the transient type of the input, which is called dynamic power dissipation. For that if I consider the input signal as a square wave and this is the time period  $0$  to  $2t$  from here to here is one time period  $t$ . So, during this period,  $v_{in}$  is equal to logic 1. If I assume that this is 5V 0V during this period,  $v_{in}$  is logic 0, that is this case here and this case here. So, in any case, one of this device is on here this is on if I take the practical case, there will be some on resistance here, as we have discussed in the transient analysis and in this case this is on this will have some on resistance of  $R_n$ .

So, there will be some power dissipation due to this on resistances and capacitance there will be some time constant. So, in order to derive the expression for the power dissipation, we will first write down the expression for the maximum charge across the capacitor.  $Q = CV$ ,  $C_{out}$  is the capacitance maximum, means it is  $V_{DD}$  maximum charge across the capacitor is  $V_{DD}$ . And if I call the drain current as  $i_D$ , in this case, this is  $i_D$ , in this case, this is  $i_D$ , the drain current  $i_D = \frac{dQ}{dt}$ , and here I am considering this total power

dissipation over a one time period and the maximum change in the Q is  $V_{DD}$ ,  $C_{out}$  into  $V_{DD}$  is equal to  $\frac{C_{out}V_{DD}}{T}$ . And, but what is the expression for the power I can call this as a average power because I am considering from 0 to T this is the average of both the positive half cycle as well as negative half cycle. The average power expression for the power will be  $V_{DD} \times i_D$  if I substitute this  $i_D$  here, then the average power is given by  $V_{DD} \times \frac{C_{out}V_{DD}}{T} = \frac{C_{out}V_{DD}^2}{T} = C_{out}V_{DD}^2 f$ ,  $\frac{1}{T}$  is nothing, but frequency of this is one of the important expression for the dynamic power dissipation of CMOS inverter.

- Maximum Charge across Capacitor  $C_{out}$  is

$$Q = C_{out} V_{DD}$$

- Drain current  $i_D = \frac{dQ}{dt}$

$$= \frac{C_{out} V_{DD}}{T}$$

- Power dissipation (Average)  $P_{av} = V_{DD} i_D$

$$P_{av} = V_{DD} \frac{C_{out} V_{DD}}{T} = \frac{C_{out} V_{DD}^2}{T}$$

$$\Rightarrow \boxed{P_{av} = C_{out} V_{DD}^2 f}$$

$$P_{av} \propto f$$

- \* High speed circuits consumes more power compared to low speed circuits

(Refer to the slide at 28:21)

You can see that  $P_{av} \propto f$ . If frequency is more, power is more, if frequency is less, power is less for high speed circuits, the frequency will be more. So, the conclusion here

is high speed circuits consumes more power and dissipates more power because  $f$  will be large. So, P average also will be large compared to the low speed circuits; this is one of the important conclusion. And, we also know that there is a compromise between speed and power because speed power product is constant.

So, this is all about this CMOS inverter. So, the next digital CMOS circuit is NAND gate because we know that NAND and NOR gates are universal gates. So, I will take two input NAND gate. Here we will use two NMOS transistors and two PMOS transistors. NMOS transistors will be connected in parallel, whereas PMOS will be connected in series. These two are PMOS transistors. These two are NMOS.

This is A, this is also A, these two will be connected, and this is B, this is also B, these two will be connected to the stage  $V_{DD}$ . Now, how to explain the operation of this NAND gate? For NAND gate, if I call the output as Y is equal to, you should get  $A \overline{B}$ . If A and B are the inputs output Y should be 0 0 0 into 0 0 0 bar is 1 0 1 0 into 1 is 0 0 bar is 1 1 into 0 is 0 0 bar is 1 for 1 1 1 into 1 is 1 1 bar is 0. This is the truth table of a two input NAND gate. So, in order to verify the operation regardless of the number of inputs for the NAND gate only two conditions we have to check.

One is we can combine these three combinations into single condition. What is that condition? If any one of the input is 0, you have to show that output is 1. This is one condition. Second condition is if all the inputs are 1, output is 0. So, regardless of the number of inputs, if I check these two conditions, it is enough.

If I consider the first condition, if any one of the input is 0 or both A B are 0. Then, if I assume that initially the MOSFETs are ideal, then what happens to this four transistors if we call this  $Q_1, Q_2, Q_3, Q_4$ ? So, what is the status of each transistor? We know that NMOS transistor will be ON if  $V_{GS}$  is positive, PMOS transistor is ON if  $V_{GS}$  is negative, either device is OFF, if  $V_{GS}$  is 0. Now, what is the  $V_{GS}$  of each of these transistors? First, you consider the  $Q_1$ . What is  $V_{GS}$  of  $Q_1$ ?  $V_{GS,Q_1} = V_{G,Q_1} - V_{S,Q_1}$ .

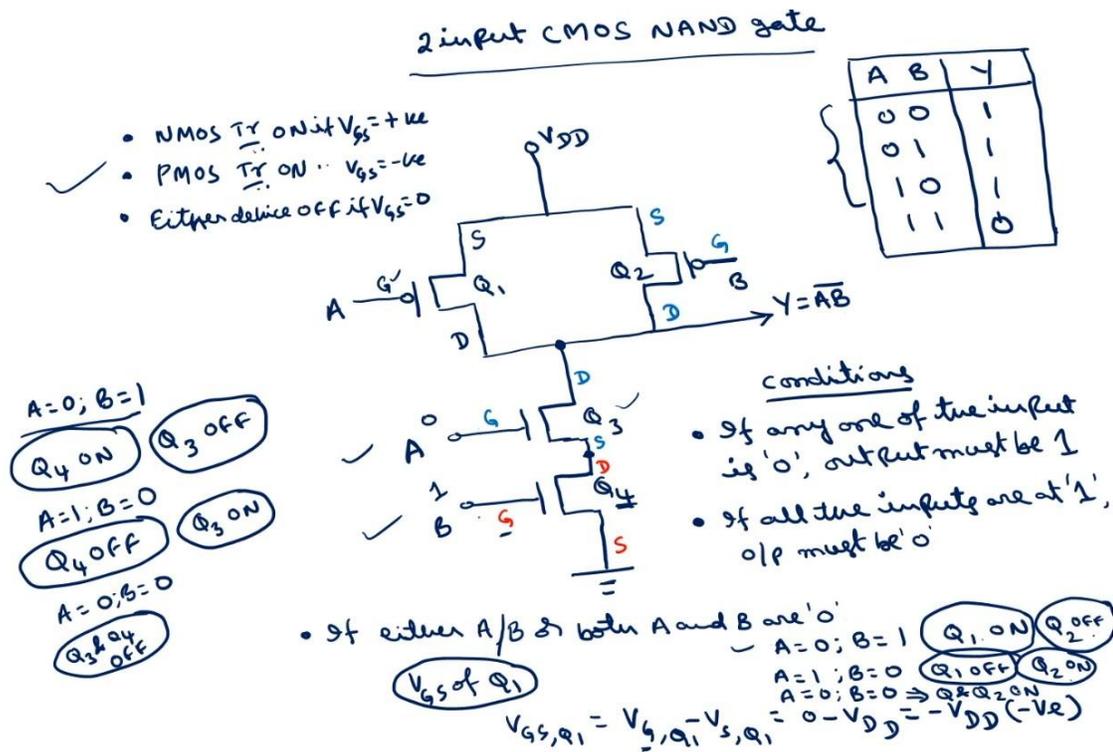
So, if A is 0, B is equal to 1, then  $V_{G,Q_1}$  is this is gate, this is source, this is drain. As for PMOS this is gate, this is source, this is drain of  $Q_4$  whereas, for  $Q_3$  this is source, this is gate, this is drain. For  $Q_1 Q_2$ , this is source, this is gate, this is drain. So, the gate voltage of  $Q_1$  is if A is equal to 0, this is 0; source voltage is  $V_{DD}$ , this is equal to  $0 - V_{DD}$ , this is equal to  $-V_{DD}$  negative.

If  $V_{GS}$  is negative for PMOS, then it will be ON. So, if A = 0, B = 1, this is on,  $Q_1$  is on, and  $Q_2$  is off because this gate voltage will be B = 1 means  $V_{DD}$  and source is also  $V_{DD}$ . So,  $V_{DD} - V_{DD}$  becomes 0. On the other hand, if A = 1, B = 0 reverse,  $Q_1$  is off,  $Q_2$  is ON.

If both are 0s, both  $Q_1$  and  $Q_2$ , both will be ON. Means in the equivalent circuit here, either both will be short circuit or one of this one will be short circuited if I take the ideal case.

Then what happens to this  $Q_3$  and  $Q_4$ ? For  $Q_4$ , gate voltage is, if I take the first case,  $A = 0$ ,  $B = 1$ , gate voltage is 1 whereas, source voltage is 0. So,  $V_{GS}$  is positive  $V_{GS}$  is positive means this transistor is on this will acts as short circuit. Whereas, what happens to  $V_{GS}$  of this  $Q_3$  this is short circuited. So, this ground potential will be available here.

So, the source of this  $Q_3$  is 0, and gate is also at 0. So,  $V_{GS}$  becomes 0 as a result of that  $Q_3$  will be off. Here, itself I will write  $A = 0$ ,  $B = 1$  can you easily see that the  $V_{GS}$  of  $Q_4$  is positive. So, this will be on for this  $Q_4$  is ON,  $Q_3$  is OFF for  $A = 1$ ,  $B = 0$  reverse  $Q_4$  is OFF you can easily verify this using the  $V_{GS}$   $Q_3$  is ON. If both are 0, both will be OFF whereas, in case of PMOS, in one case,  $Q_1$  is on,  $Q_2$  is OFF other case,  $Q_1$  is off,  $Q_2$  is on. In the third case, both will be on. So, what are the possibilities here? If I take the worst case from here to here, this is the where you are going to take output Y.



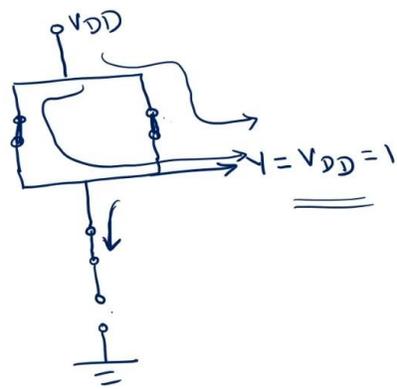
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So, here, in one case,  $Q_1$  is on  $Q_2$  is off. In the worst case both will be on. Here either

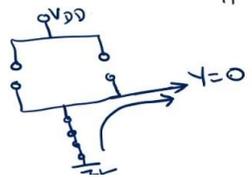
both will be short circuited, or one of this one is short circuited, whereas, here, either one of this one will be short circuited, or both will be open circuited. In any case, does not matter either this will be short circuited, or this will be open circuited, or this will be short-circuited this will be open circuited still, there is no path to flow the current here. Whereas, here, even if one is short circuited the other one is open circuited, the current flows through this to the output. If this is short circuited current flows through this, if both are short circuited current flows in the both the branches whereas, here in any case one of this one is open circuited. So, here there is no current as a result of that output Y will be here because there is a short circuit between the  $V_{DD}$  to output; output is  $V_{DD}$ , which is logic 1. So, if either of A B or A and B are 0s output, you are getting as logic 1. This is verified.

The second condition is if all the inputs are at logic 1, then what happens this is at logic 1, this is at logic 0, or ground  $V_{GS}$  is positive.  $V_{GS}$  is positive means this will be on, and this will act as a short circuit. So, this is at ground potential assuming that this  $Q_4$  is ideal, this is ground, and this is 1.

So,  $V_{GS}$  is again positive this is also ON. Whereas  $V_{GS}$  of this is at  $V_{DD}$  and A is also at  $V_{DD}$  because both A and B are 1s. So,  $V_{GS}$  becomes  $V_{DD}$  minus  $V_{DD}$  0. So, this will be OFF similarly the case of this one here. This is  $V_{DD}$  source is also  $V_{DD}$ . So, this is  $V_{GS}$  of this one is 0. This is OFF. So, both the PMOS transistors will be OFF, NMOS transistors will be on.



- If all the inputs are '1'  $\Rightarrow$  Both PMOS Tr are OFF  
 " NMOS " " ON



(Refer to the slide at 42:15)

So, what will be equivalent circuit here? The upper part is open-circuited; this is open circuit. This is open circuit here; I am taking the output Y as here both are short circuited; this is grounded. So, what happens to output this short circuited output becomes ground which is logic 0 this is logic 0. So, this is the operation of a 2 input CMOS NAND gate. If any one of the inputs is 0, output is at logic 1. If all the input are at logic 1, output is 0. So, this is the operation assuming that the transistors are ideal, but in practical case there will be some on resistance. If a transistor is off, it will acts as open circuit. If the transistor is on, then it will offer some on resistance. If it is a PMOS transistor,  $R_p$  is the on resistance, NMOS transistor,  $R_n$  is the on resistance.

So, in that case, what will be the transition response of this 2 input CMOS NAND gate that we will discuss in the next lecture?