Integrated Circuits and Applications

Prof. Shaik Rafi Ahamed
Department of Electronics and Electrical Engineering Indian Institute of Technology, Guwahati

Digital CMOS Circuits
Lecture – 41
CMOS Inverter

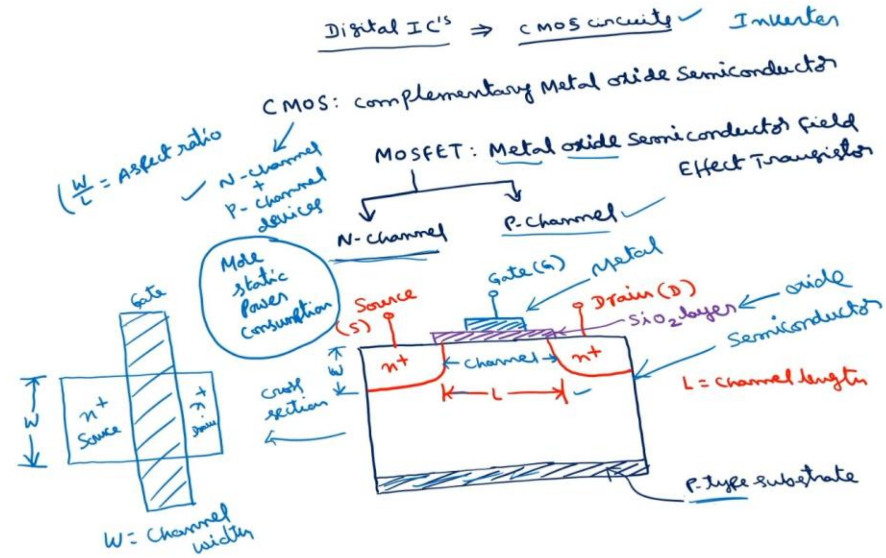
So, in the last lectures, we have discussed various analog integrated circuits and some mixed signal circuits such as A to D and D to A converters, which consists of a part of analog circuitry, a part of a digital circuitry. Today, we will discuss some of the digital circuits, especially the CMOS circuits. So, the expansion of the CMOS is complementary metal oxide semiconductor. So, you might have studied MOSFET in your electronic devices course. This is called a metal oxide semiconductor field effect transistor. Basically, there are two types of the MOSFETs: one is N channel, another is P channel.

If you consider the structure of this N channel MOSFET, there will be a P type substrate, and two in place wells. In between this is called as channel, L is the channel length. Here, there is one terminal called source, and here, there, is terminal called drain.

And, there will be SiO_2 layer above which there will be a gate. That is why the name metal oxide semiconductor. You can see three layers this is metal, this is oxide and this is semiconductor. That is why the name metal oxide semiconductor. N channel, as the name implies, the channel here is N type. This is channel, and the substrate here is P type.

If you take the P channel, then the substrate is N type and channel is P type. Here, if I take the cross dimension of this figure, this is the gate, this is one end place, this is another end place, this is source, this is drain, this is gate. If you take the cross section of this diagram, we can see here the channel length; channel width is this W. Here somewhere we will be having W, this is channel length L, this is width W. So, this $\frac{W}{L}$ ratio is called aspect ratio.

This plays an important role in the design of CMOS circuits. So, this is the basic structure of N channel MOSFET. Similarly, you can have P channel MOSFET. Now, the CMOS circuits consists of both N channel as well as P channel devices. We can construct the circuits using only N channel as well as only P channel devices, but there are some drawbacks of this N channel devices and P channel devices.



(Refer to the slide at 08:40)

To avoid these drawbacks, we will use the CMOS circuits, which consists of both N channel as well as P channel. The main drawback of this N channel or P channel devices is more static power consumption. Later, we can see that in CMOS, the power consumption is less when compared with the N channel devices or P channel device based circuits. So, I will start the CMOS circuits with the basic circuit inverter. So, the first circuit is CMOS inverter.

As I have told this consists of both P channel as well as N channel device. So, this is the CMOS inverter. So, you see the symbol of mass weight. There are basically four terminals; normally, the substrate will be grounded. Here, will be some substrate also, and it will be grounded.

So, if we neglect this, then there will be gate, source and drain. So, this bubble represents this is P channel and this is N channel. So, in P channel, the current direction will be inside this arrow and here outside. So, this is gate of P channel, this is gate of N channel, this is source of P channel, this is source of P channel, this is drain of P channel, this is drain of N channel. Now, we will see the operation of this CMOS inverter.

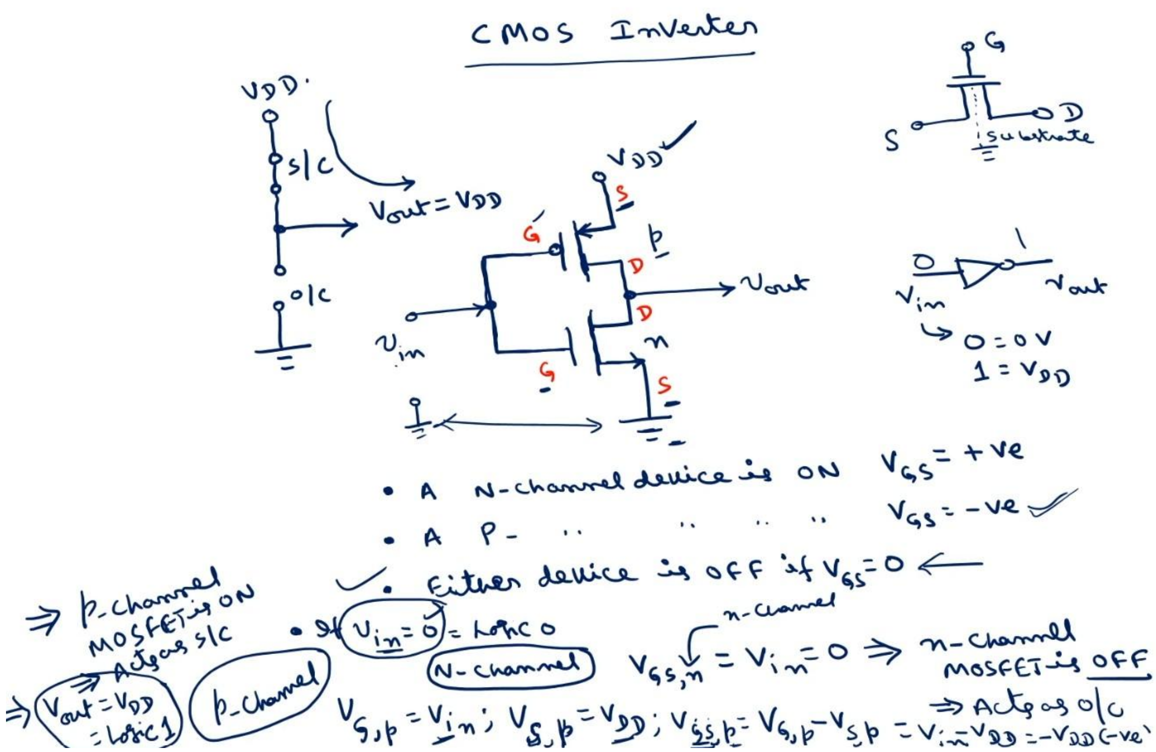
This is basically a inverter with Vin as input, v_{out} as output. So, in order to understand the operation of any of the CMOS circuits, you have to remember three points. One is a N channel MOSFET, or N channel device is on if $V_{GS} = +ve$ V_{GS} is equal to positive. A P channel device is on if $V_{GS} = -ve$. Either device means either N channel or P channel is off if $V_{GS} = 0$.

So, initially I am assuming this P channel and N channel are ideal. So, what are the two possibilities of this v_{in}? This can be 0 or logic 1; 0 means 0 volts, logic 1 means

V_{DD}. If v_{in} is 0 that is logic 0, then what happens to the P channel device and what happens to N channel device? If we consider the N channel device, this v_{in} is with respect to this ground and this is V_{GS}. So, what is $V_{GS,n}$? This N stands for N channel. $V_{GS,n}$ means gate to the source is nothing, but these two points are connected.

So, v_{in} and G are same. This v_{in} also with respect to the same ground. So, these two are same. $V_{GS,n} = v_{in}$ itself that v_{in} we have taken as 0. If $V_{GS} = 0$, according to this implies N channel MOSFET is off.

Ideally, it will acts as open circuit, open circuit. Then what happens to P channel? So, what is V_{GS} of P channel? If I know this V_{GS}, I can find out whether this device is on or off. What is V_G? V_G of P channel. $V_{G,p}$ means this gate voltage of P channel device. This is directly connected to v_{in}.



(Refer to the slide at 17:17)

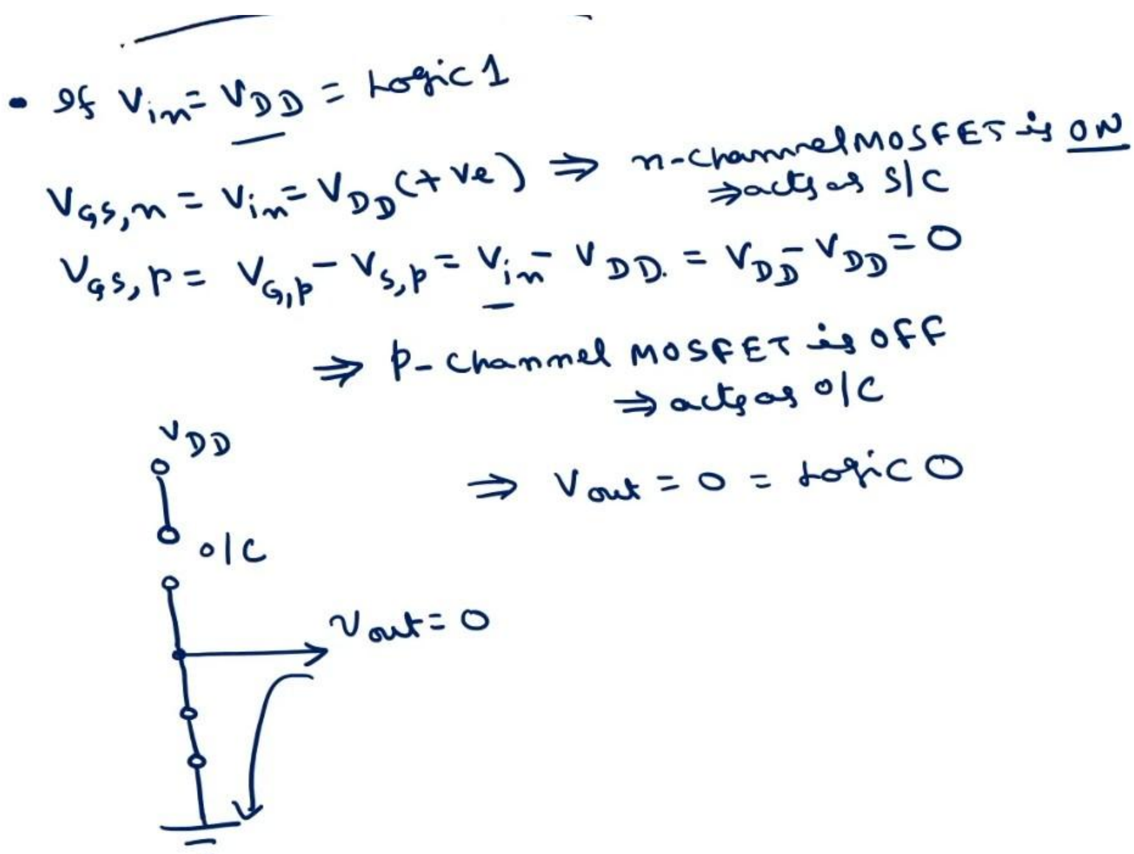
So, this is equal to v_{in} only. And what is V source voltage of P channel? This S stands for source, this P stands for P channel. So, this is V source voltage of P channel, which is nothing, but V_{DD}. Therefore, what is $V_{GS,p}$? P channel V_{GS} voltage is nothing but $V_{G,p} - V_{S,p}$. This is $V_{GS,p}$ means $V_G - V_S$.

$V_{G,p} = v_{in}$, $V_{S,p} = V_{DD}$. $v_{in} - V_{DD}$. What is v_{in}? $v_{in} = 0 - V_{DD} = -V_{DD}$, and this is negative. So, V_{GS} of P channel is negative. So, what happens? V_{GS} is on implies

P channel MOSFET is on.

Ideally, it will act as short circuits. So, what will be equivalent circuit of this one now? So, this V_{DD} this P channel will act as short circuit. This is short circuit, and here N channel will be open circuited. This is grown point. So, what will be output we are taking here? This is V_{DD}.

So, what happens? This entire V_{DD} will be appeared across v_{out}. So, this $v_{out} = V_{DD}$ implies $v_{out} = V_{DD}$ which is at logic 1. So, if input is logic 0, output is logic 1. This is the inverter. This is logic 0, here this is logic 1.



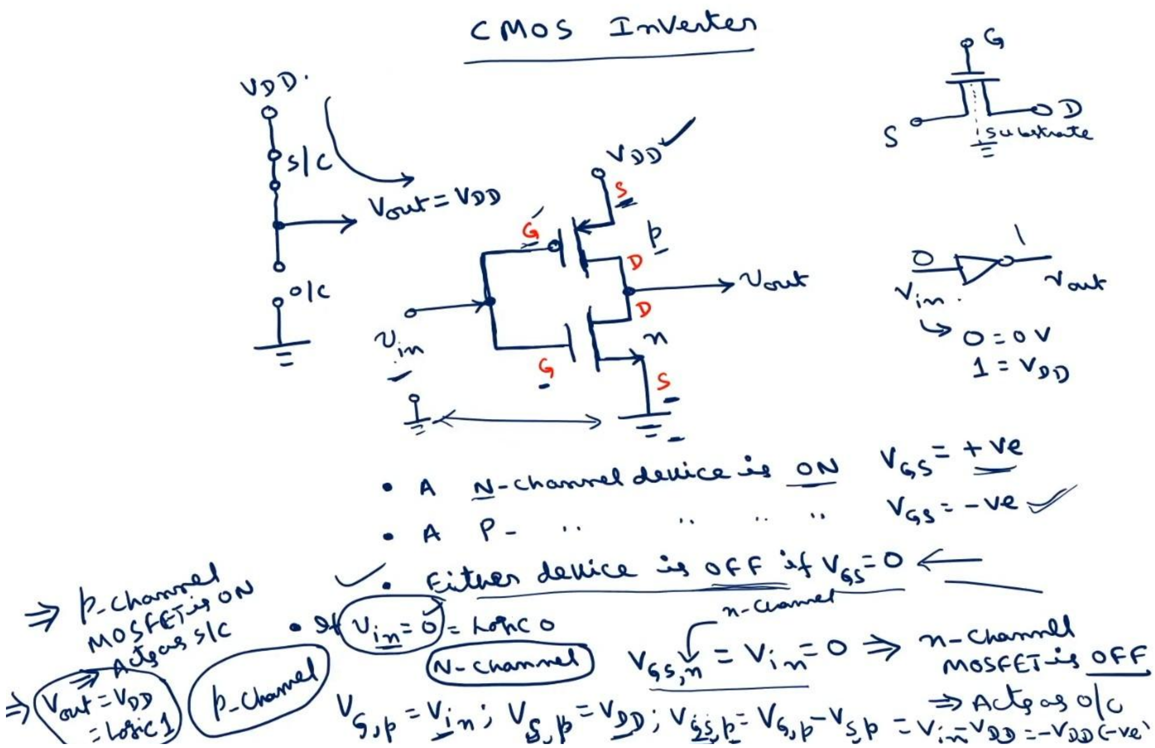
(Refer to the slide at 20:10)

Second case is if v_{in} is V_{DD}, what happens? What is V_{GS} of N channel? What is V_{GS} of P channel? Based on this, we can find out whether the device is on or off. What is V_{GS}? As you have seen here, V_{GS} N is nothing but v_{in} itself and what is that v_{in} V_{DD}, which is positive? So, if V_{GS} of N channel is positive, this will be on, implies N channel MOSFET is on, N access short circuit. Then what is V_{GS},p is nothing, but $V_{G,p} - V_{S,p}$. This is equal to $V_{G,p}$ nothing, but v_{in} and V_{SC} nothing, but V_{DD}.

This is equal to V_G is v_{in} and $V_{S,p}$ is V_{DD}. But what is v_{in} V_{DD}? This is equal to

$V_{DD} - V_{DD} = 0$. If V_{GS} of either device is 0, this will be off, implies P channel MOSFET is acts as open circuit in ideal case. So, what will be circuit now? Here we have V_{DD}, this is P channel, this acts as open circuit. Then here we have N channel, this will acts as short circuit; this is grounded and here you are taking the output v_{out} because this was shorted $v_{out} = 0$.

If v_{in} is at logic 1, v_{out} is at logic 0. This is the operation of the inverter. So, this will acts as a inverter. If, I give logic 0 here, we will get logic 1 here. If I give logic 1 here, output is logic 0.



(Refer to the slide at 20:10)

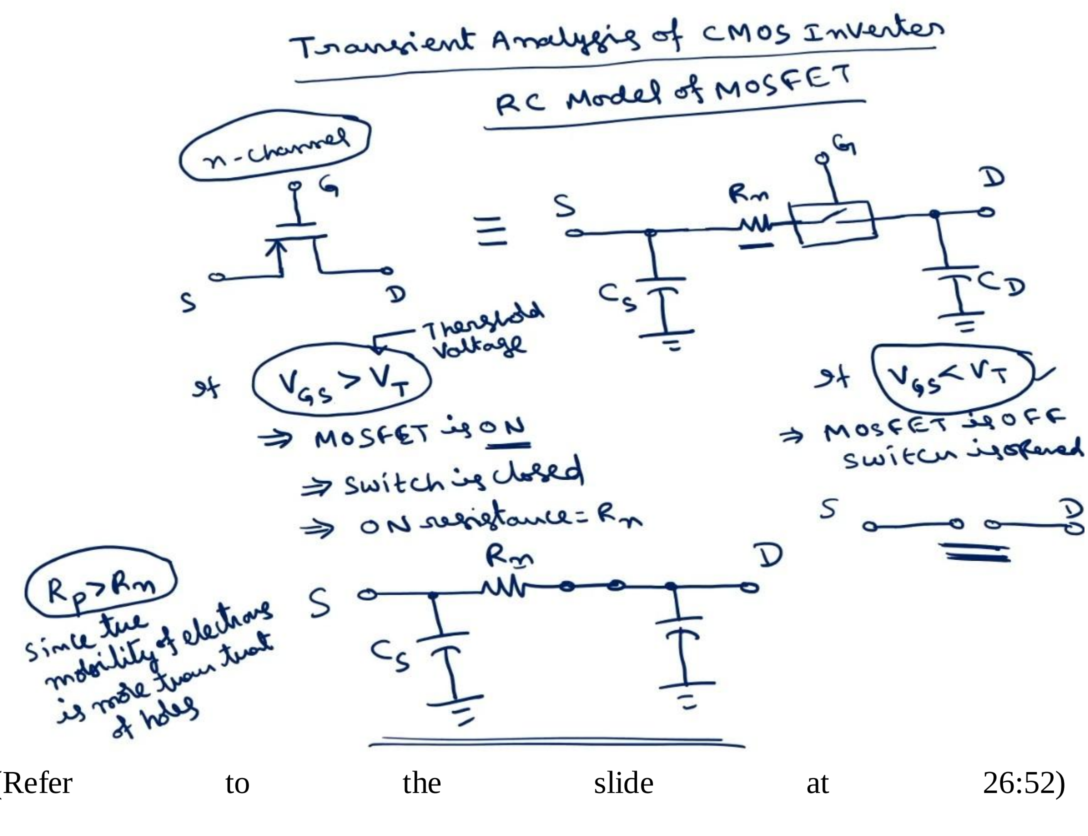
This is the ideal case, but practically it will take some time to change from 0 to 1 and 1 to 0. This is what is called the transient response. So, transient analysis of CMOS inverter. Now here we have to take the practical case. The source drain gate, this equivalent RC model, is we have source; then there will be some capacitance here, which is called as source capacitance.

So, wherever two conductors are there, there will be some capacitance. In ideal case, we will assume the capacitance are not present, and you have obtained this output as logic 1 for input as logic 0 and vice versa. In practical case, you have to consider the capacitances also. Then this will acts as a switch with some resistance. This is gate terminal; this is R_n is the on resistance of n channel MOSFET.

If we call this as n channel MOSFET, then this is drain terminal. Here also, there will be some capacitance, which is called C_D, drain capacitance. Now, it depends upon the V_{GS}. So, in case of ideal case, what we assumed is if V_{GS} is positive, N channel MOSFET will be on, and it will acts as short circuit. There is no resistance at all and if V_{GS} is 0, then it will acts as open circuit. Whereas, in practical case if $V_{GS} > V_T$, this is called threshold voltage.

Of course, everything is for n that is why I am not writing comma n and all, then MOSFET is on. So, whenever this is on, then this switch is closed, and this will provide on resistance of R_n. So, what will be equivalent circuit now? This is source, then R_n, of course, this will act as short circuit and drain here, source capacitance here, drain capacitance this is R_n. If $V_{GS} > V_T$, if $V_{GS} < V_T$, MOSFET is off and switch will be opened. And simply, there is a open circuit between source and drain.

Because there is a open circuit, there will be no resistance, no capacitance, nothing. Actually, this will be acts as open circuit; this is same as the ideal case. So, this is the equivalent circuit. In case if $V_{GS} < V_T$, simply open circuit; if $V_{GS} > V_T$, this is the equivalent circuit of NMOS device. Similarly, you can have PMOS device here that will be having R_p; $R_p > R_n$. Why? The mobility of electrons is greater than the mobility of holes. That is why the resistance to holes is more than resistance to electrons.



(Refer to the slide at 26:52)

Now, in the transient analysis I will consider the same CMOS circuit, I will consider the same CMOS inverter circuit. If I apply low to high transition here, output changes from high to low. So, this delay time is called as T high to low, also can be called as fall time. Of course, fall time is later. I am going to define from 90% of the high value to the 10% of the high value change is called as fall time. We are going to derive the expression for the fall time of this CMOS inverter.

Later I will consider the rise time. So, I am not showing here the capacitance all, but all the capacitance will be present source capacitance and drain capacitances. Here I will take now this as a function of time. So, how does this output will changes? If, I connect here some capacitance C_{out}, which consists of the drain capacitance of this P channel as well as drain capacitance of N channel. So, C_{out} is drain capacitance of the P channel plus drain capacitance of N channel and some load capacitance also. So, across this C_{out}, we are taking output voltage.

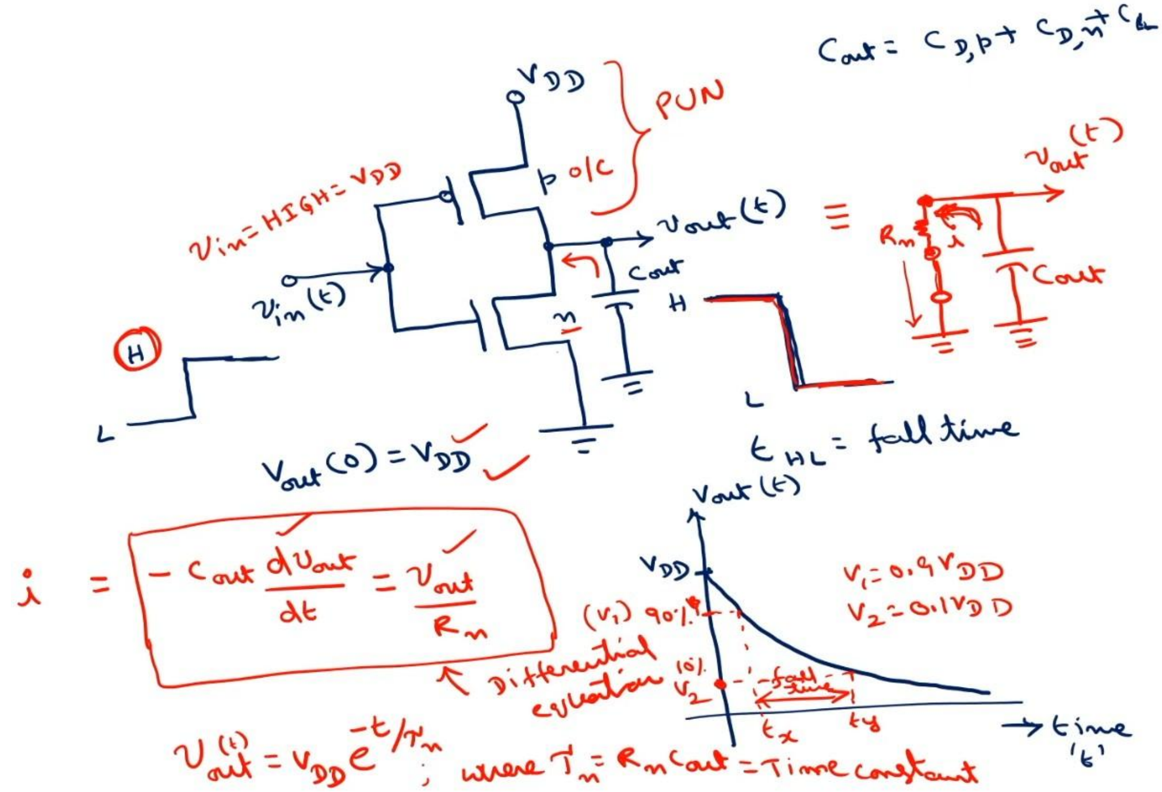
Initially, what will be the output voltage high? Then it will comes to low. Initially, V_{DD}, but it will not come abruptly in case of ideal it will this time taken to change from high to low is 0, but practically because of this capacitances and all there will be exponential decay. Finally, it will come to low. This is nothing but v_{out} as a function of time. What is the initial value of v_{out}? It is 0 initially high this V_{DD}.

If I assume, that this is the direction of the current. So, what will be equivalent circuit? If I apply from low to high, if input is high then what happens to the P channel what happens to N channel? If P in is high this is V_{DD}. As in the previous case, if v_{in} is high, then P channel will be off, N channel is on. So, what will be equivalent circuit? This V_{DD} and P channel will be open circuited. So, there will be no part of this pull up network. This is called pull up network, only pull down network will be there.

So, there will be a short circuit here. This is the output, and this will have a short circuit, P channel for input is high, and here we are taking the capacitor C_{out}, and this is the current direction. Now, the capacitor will discharges to ground. Similarly, what will be voltage across this one V_{DD}, because this was in high now it will comes to low. So, from this high to low transition takes place through this short circuit and then to the ground. So, what is the expression for the current because the current direction is from ground to this v_{out} this is v_{out} point. $i = -c_{out}\frac{dv_{out}}{dt}$, is the expression for the current through the capacitor.

But if I consider this practical case, there will be on resistance. So, here there will be some on resistance there is a short circuit and this is on resistance because this is N device is on. So, what is the expression for this current? This is the voltage v_{out}. This is resistance. $V = Ri$, and this is also equal to $\frac{v_{out}}{R_n}$. This is an expression for i. In terms of C this is the expression in terms of V and R this is the expression. So, if

I solve this first order linear differential equation this is a differential equation with initial condition that v_{out} of 0 is equal to V_{DD}, we will get $v_{out} = V_{DD} e^{-\frac{t}{\tau_n}}$, where $\tau_n = R_n C_{out}$, this is called time constant of N channel device.



(Refer to the slide at 34:53)

Now, the fall time is defined as normally the 90% of this V_{DD}, which is 0.9 if I call this one as t_x and if I call this voltage as V_1, $V_1 = 0.9V_{DD}$, means 90% of V_{DD} and if I call this as V_2, V_2 is 10% of V_{DD} is 0.1 V_{DD} this is t_y this time is defined as normally fall time. So, in order to derive the expression for this one, $e^{-\frac{t}{\tau_n}} = \frac{v_{out}}{V_{DD}}$ or $-t = \tau_n \ln[\frac{v_{out}}{V_{DD}}]$ or if I take t then you have to reverse this $\tau_n \ln[\frac{V_{DD}}{v_{out}}]$.

Then we are calling t_x as the time at which $v_{out} = 1V$, which is $0.9V_{DD}$. If I substitute that at $t = t_x;\ v_{out} = 0.9V_{DD} \Rightarrow t_x = \tau_n \ln\left[\frac{V_{DD}}{0.9V_{DD}}\right] = \tau_n \ln[\frac{1}{0.9}]$, this is expression 1. At $t = t_y;\ v_{out} = 0.1V_{DD} \Rightarrow t_y = \tau_n \ln\left[\frac{V_{DD}}{0.1V_{DD}}\right] = \tau_n \ln[\frac{1}{0.1}]$. And what is fall time t_f if I call as fall time the difference of these two $t_f = t_y - t_x = \tau_n \ln\left[\frac{1}{0.9}\right] - \tau_n \ln\left[\frac{1}{0.1}\right] = \tau_n \ln(9) = 2.2\tau_n$.

$$e^{-t/\tau_n} = \frac{V_{out}(t)}{V_{DD}}$$

$$\Rightarrow -\frac{t}{\tau_n} = \ln\left[\frac{V_{out}(t)}{V_{DD}}\right]$$

$$-t = \tau_n \ln\left[\frac{V_{out}(t)}{V_{DD}}\right]$$

$$t = \tau_n \ln\left[\frac{V_{DD}}{V_{out}(t)}\right]$$

At $t = t_x$; $V_{out}(t) = 0.9V_{DD}$

$$t_x = \tau_n \ln\left(\frac{V_{DD}}{0.9V_{DD}}\right) = \tau_n \ln\left(\frac{1}{0.9}\right) \quad \text{--- (i)}$$

At $t = t_y$; $V_{out}(t) = 0.1V_{DD}$

$$t_y = \tau_n \ln\left(\frac{V_{DD}}{0.1V_{DD}}\right) = \tau_n \ln\left(\frac{1}{0.1}\right)$$

$$t_f = t_y - t_x = \tau_n \ln\left(\frac{1}{0.1}\right) - \tau_n \ln\left(\frac{1}{0.9}\right) = \tau_n \ln(9) = 2.2\tau_n$$

$$\boxed{t_f = 2.2\tau_n = t_{HL}}$$

$$\tau_n = R_n C_{out}$$

(Refer to the slide at 38:27)

This is normally called as high to low transition $t_f = 2.2\tau_n = t_{HL}$, where τ_n is time constant, which is equal to $R_n C_{out}$. This is expression for the fall time. So, in the next lecture, we will discuss about the rise time, and we will have some discussion. Thank you.