

Integrated Circuits and Applications
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Data Converters
Lecture – 39
Inverted R-2R Ladder D/A Converter

In the last lectures, we have discussed about the weighted resistor D to A converter and R-2R ladder D to A converter. The drawback of this weighted resistor and R-2R ladder DAC is the current through the resistors varies with the input bit pattern. Current through the resistor changes with input bit word and the input digital input. You can easily see that here, the voltage is this much, this much, this much, whereas the resistors are same. So, the current here is different from the current here, current here. So, if the bit pattern changes, the voltage here will be different again.

This voltage of $-\frac{V_R}{16}$ this is corresponding to 001, corresponding to 100. The voltage here is V_C , we have got as $-\frac{V_R}{4}$. This is $-\frac{V_R}{4}$ for input of 100 whereas, the same voltage at node is node C is $-\frac{V_R}{16}$ if the input bit pattern is 001 for 001 $-\frac{V_R}{16}$ for 100 $-\frac{V_R}{4}$. So, because of this different voltage, but in both the cases, this is to R. So, the current through this one is varies with the input bit pattern, even in the case of R weighted resistor DAC also.

So, because of this current change in the resistors due to the change in the input bit pattern, the power dissipation will be more. To avoid this, we will use inverted R-2R ladder DAC. Here, we are going to show that regardless of the input bit pattern, that is, regardless of the values of the digital input, the current through the resistors remains constant. Because of that, the voltage across the resistor is constant, thereby less power consumption well as. So, the stray capacitance will not slow down the performance of the DAC. These are the two advantages of inverted R-2R ladder DAC. If I consider 3-bit inverted R-2R ladder DAC, the circuit diagram is as follows.

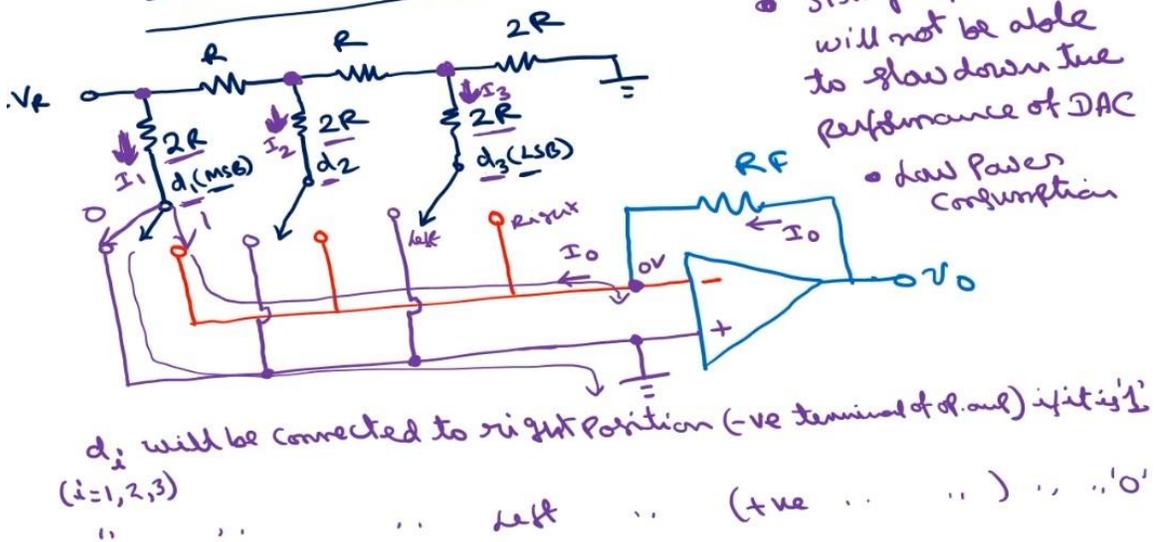
This is R R, this is 2R, this is $-V_R$, this is 2R, 2R, 2R. One major difference between the R-2R ladder DAC and inverted R-2R ladder DAC is here we are going to apply the MSB bit and here LSB. In case of direct R-2R ladder, here, it is LSB, and here, it is LSB. This is one difference. And another difference is here, in any case, the current flows through the ground regardless of the switch position, and the switch is connected to the right position. This is connected to the minus terminal, correspond to the plus terminal. The switch is connected to the left, and

this is connected to the feedback resistor R_F . Here, output v_0 is taken, and this point is grounded.

Drawback of weighted resistor & R-2R ladder DAC

- Current through the resistor changes with input bit word (digital input) \Rightarrow More Power dissipation

Inverted R-2R ladder DAC (3-bit)



(Refer to the slide at 12:27)

So, this also will get ground potential because of the virtual ground. If I assume that this current is, I_0 , the same I_0 will flow through this one. Let this current be I_1 because of this d_1 , this is I_2 , this is I_3 . d_i in general i varies from 1, 2, 3 will be connected to right position this is right position, and this is left right position, which is connected to minus. If it is at logic 1, whereas d_i will be connected to left position, which is nothing, but positive terminal of half amp if it is at logic 0.

Now, an interesting fact here is if this d_1, d_2, d_3 bits are 0, then this will be connected to the positive terminal here this will be connected here this will be connected here if this bit is 0 and, this will be connected here if this bit is 1. So, in either of these positions, say if this is connected to this point, this current will flow from here through here to ground. If this switch is connected to the right position, say this here, the current will flow here, here, here this also flows to flows to ground because this is also at virtual ground. That is, regardless of these d bits, whether d is 0 or 1, the current always flows to the ground, and these resistor

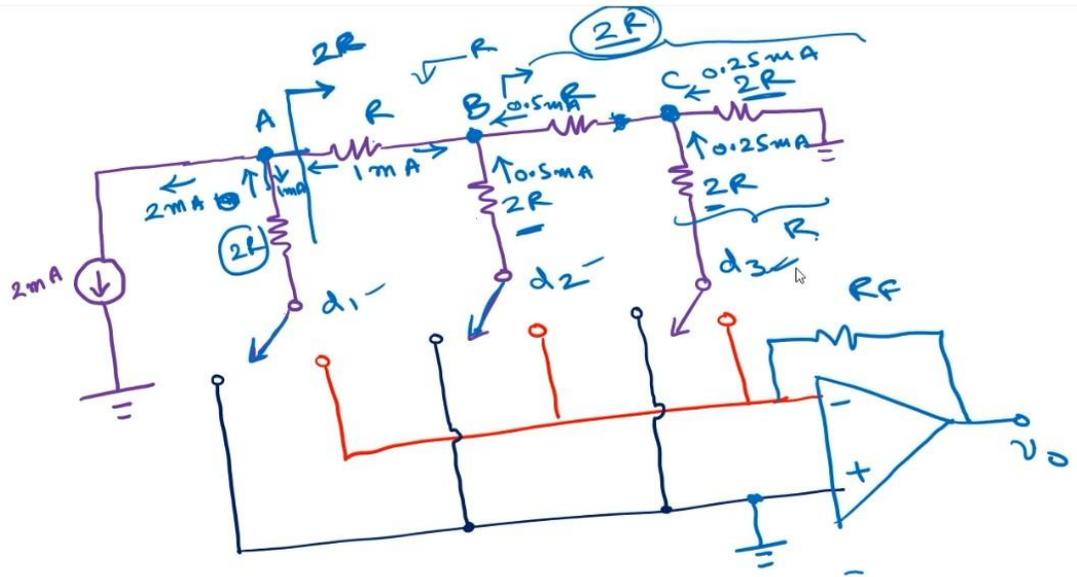
values are equal. Because of that, the current through these resistors is independent of the pattern of d_1, d_2, d_3 . So, whatever the combination of these d_1, d_2, d_3 , we can have 8 combinations 0 0 0, 0 0 1, 0 1 0, 1 0 0 so on up to 1 1 1 for all the 8 positions, the current I_1, I_2, I_3 are constant.

This is one of the beautiful features of this inverted R-2R ladder DAC. So, because of that, what happens is the voltage at these points is the same regardless of this d_1, d_2, d_3 input binary word. So, because this voltage here is the same, this will be less affected by stray capacitances. So, stray capacitance will not be able to slow down the performance of the DAC, whereas, in case of direct R-2R ladder or weighted resistor, these voltages are different, as you have seen in the previous slides. So, because of that, the stray capacitance will slow down the performance.

So, in that way this inverted R-2R ladder is faster than the previous two DACs. This is one advantage of inverted ladder R-2R ladder DAC, and the second one is low power consumption, why because the current is constant regardless of d_1, d_2, d_3 values. So, if there is a change in the current, then it will dissipate more power, but here, independent of d_1, d_2, d_3 , the current is constant, so power consumption is less. So, we can see how this current will be constant here in these branches; if I consider the equivalent current diagram, if I assume that the reference current is 2mA, then the circuit diagram will be like this. So, now this is 2mA here. Let us call this as node A, node B, node C.

So, in any case this point will be connected to the ground regardless of this d_1, d_2, d_3 . So, what will be the total resistance if you look from here total resistance to the right side of this node A? These are 2R values, this is 2R, this is R so, this 2R, 2R in parallel. So, resultant is R this R plus, this R total up to here, this is 2R again, this 2R, this 2R in parallel. So, up to here, this is R, this R plus, R total 2R.

So, here, this is a 2R, and to the right side, the entire circuit is having 2R resistance, means this 2mA will be equally distributed between this branch and this branch. This is 1mA here and 1mA here. Similarly, if I see at the B right side of this is 2R again, and this is 2R, this is 1mA. So, this will be again equally divided into 0.5mA and 0.5mA. Again, at C right side also, this is 2R, this is 2R. So, this current is this current is 0.5mA. So, this will be 0.25mA, this will be 0.25mA, this is regardless of this d_1, d_2, d_3 . This is how we can maintain the constant current to the resistors regardless of d_1, d_2, d_3 values. Now, we will discuss one problem on this inverted R-2R ladder D to A converter. Consider the following inverted R-2R ladder DAC. This was the DAC that we have considered in the previous slide.



• Resistance to the right of node A

(Refer to the slide at 16:45)

This switch is connected to right side, it is connected to negative terminal, and this is connected to positive terminal. Virtual ground this is a actual ground C, $-V_R$ here $2R, R, 2R, R, 2R, 2R$. If $R = R_F = 10k\Omega$, determine the output v_0 .

If d_1, d_2, d_3 is equal to 1 1 1, this is d_1 MSB this is d_2 this is d_3 LSB. So, if d_1, d_2, d_3 are 1 1 1 this will be connected to the negative terminal. So, the equivalent circuit of this one will be now simply $-V_R, R, R, 2R$ this is $2R$ connected to the negative terminal this $2R$ also will be connected to negative terminal this also connected to the negative terminal, this 3 will be short circuited terminal will be simply grounded this is R_F this is I_0 this is also I_0 because here the current is 0. If I assume that out op amp is ideal, this is the equivalent circuit. If I call this current as I_1 , this as I_2 , this as I_3 , then the current that is entering here is I_0 at this junction. All the currents I_1, I_2, I_3 and I_0 are entering.

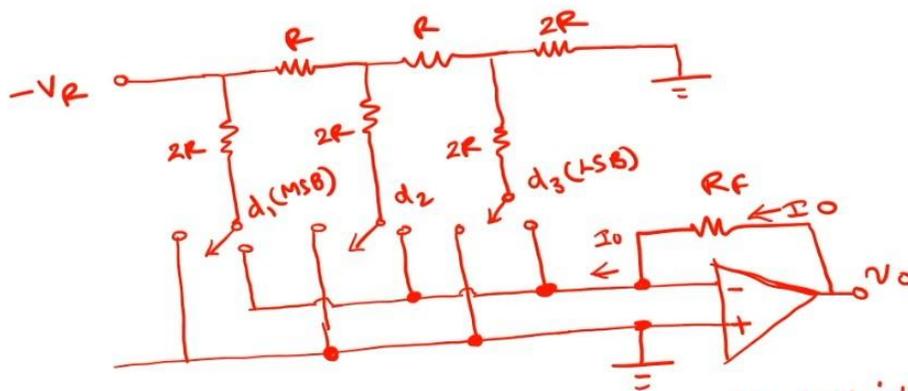
So, $I_1 + I_2 + I_3 + I_0 = 0 \Rightarrow I_0 = -(I_1 + I_2 + I_3)$. Now, here the voltage is $-V_R$ because this point is shorted with this. So, what is the expression for I_1 , this is at ground potential, this is also ground potential, this is also ground potential. So, the direction of the current is this. So, $I_1 = \frac{-V_R - 0}{2R} = \frac{-V_R}{2R}$.

It is given that $R = R_F = 10k\Omega$, and let us assume that it is also given the V_R value, let $V_R = 10V$. Then what will be this $\frac{-10}{20k\Omega} = -0.5mA$, right? Now, what is

I_2 ? As you have seen in the previous slide, the current through this one is half of the current through this because this current will be divided equally between this branch and this branch. Similarly, this current will be equally distributed between this branch and this branch.

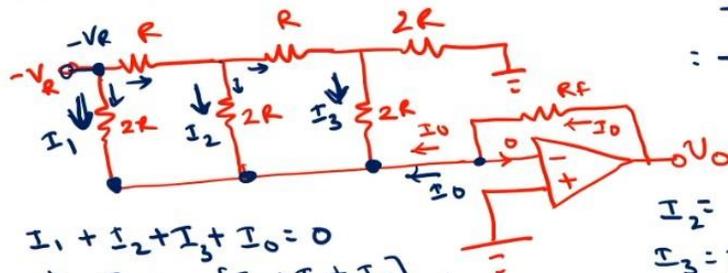
As a result of that this $I_2 = \frac{I_1}{2} = -0.25\text{mA}$. $I_3 = \frac{I_2}{2} = -0.125\text{mA}$. So, what is I_0 from here? $I_0 = -(I_1 + I_2 + I_3) = -(-0.5\text{mA} - 0.25\text{mA} - 0.125\text{mA}) = 0.875\text{mA}$. This is equal to -0.875mA . So, we want the output voltage v_0 ; you can see that from here to here, this direction of current is from output to this virtual ground. So, $I_0 = \frac{v_0 - 0}{R_F} \Rightarrow v_0 = I_0 R_F$. $R_F = 10\text{k}\Omega$ this is minus of all these values are -0.5mA , -0.25mA , -0.125mA . So, as result of that, this minus minus becomes plus, this is equal to $0.875 \times 10^{-3} \times 10\text{k}\Omega = 8.75\text{V}$.

Ex:- consider the following inverted R-2R ladder DAC:



If $R = R_F = 10\text{k}\Omega$, determine the output v_0 if $d_1, d_2, d_3 = 111$. Let $V_R = 10\text{V}$

Sol:-



$$I_1 + I_2 + I_3 + I_0 = 0$$

$$\Rightarrow I_0 = -[I_1 + I_2 + I_3]$$

$$I_1 = \frac{-V_R - 0}{2R}$$

$$= -\frac{V_R}{2R} = -\frac{10}{20\text{k}\Omega}$$

$$= -0.5\text{mA}$$

$$I_2 = \frac{I_1}{2} = -0.25\text{mA}$$

$$I_3 = \frac{I_2}{2} = -0.125\text{mA}$$

(Refer to the slide at 24:36)

So, this is about this inverted R-2R ladder D to A converter. There are some D to A converters, which are available in IC form; also, they are called as monolithic D to A converters. In this again, the output of this D to A converter can be current or voltage or both. If I take this MC14xx family, this will produce the output in the form of current.

And if I take this xx family output is voltage. If we take datal family output is voltage, both voltage and current is called hybrid D to A converter.

$$\begin{aligned}
 I_0 &= - [I_1 + I_2 + I_3] \\
 &= - [0.5 - 0.25 - 0.125] \text{ mA} \\
 &= +0.875 \text{ mA}
 \end{aligned}$$

$$\begin{array}{r}
 0.5 \\
 0.25 \\
 0.125 \\
 \hline
 0.875
 \end{array}$$

$$\begin{aligned}
 I_0 &= \frac{V_0 - 0}{R_f} \Rightarrow V_0 = I_0 R_f \\
 &= 0.875 \times 10^{-3} \times 10^3 \\
 &= 8.75 \text{ V}
 \end{aligned}$$

Monolithic D/A converters

MC 14xx family \Rightarrow o/p is current
 LM 50xx " \Rightarrow " " voltage
 DATEL " \Rightarrow " " voltage & current (Hybrid)

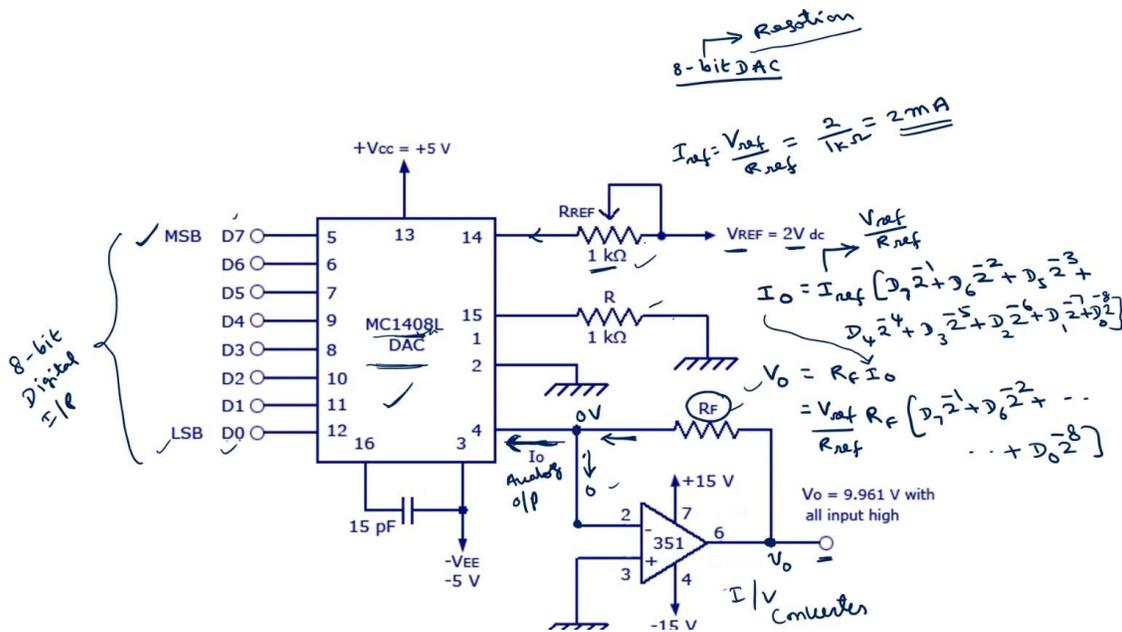
(Refer to the slide at 28:30)

I will consider one of these monolithic D to A converters and I will discuss the details of this particular D to A converter. This is MC1408. So, the last two digits 08 stands for 8-bit D to A converter. This 8 bits is also called as a resolution; I will define what is resolution at the end of this lecture. See here you can see that the output will be in the form of a current.

To get the output voltage, we need a current to voltage converter. This is basically current to voltage converter. This you have to connect externally. This is available in IC form these components you have to connect externally. So, this I_{ref} will be simply V_{ref} by R_{ref} .

Here, if I take 2V DC $R_{ref} = 1k\Omega$, we will get $I_{ref} = \frac{2}{10k\Omega} = 2mA$. For this MC1408, the $I_{ref} = 2mA$. And the expression for the output current in terms of this MSB bit as D_7 , LSB bit as D_0 . So, in the previous discussions, we have assumed this lowest D_0 as MSB

and D_7 as MSB, but in this particular IC, D_7 is MSB and D_0 is LSB. Then, the expression for the output current this output current produced by this MC1408 is given by $I_0 = I_{ref} [D_7 2^{-1} + D_6 2^{-2} + D_5 2^{-3} + D_4 2^{-4} + D_3 2^{-5} + D_2 2^{-6} + D_1 2^{-7} + D_0 2^{-8}]$. This is the expression for the output current produced by this D to A converter subjected to this 8 bit digital input. This is the digital input; this is analog output. As I have told, analog output will be in the form of current. If you take the other family, it may produce the output as a voltage and there are some ICs which produce both current as well as voltage.



(Refer to the slide at 33:18)

So, this I_{ref} is nothing, but again, this $\frac{V_{ref}}{R_{ref}}$. And, if you want to expression for the output voltage here after this current to voltage converter. So, what is the expression for the v_0 in terms of I_0 ? Because this current is I_0 , this is 0; this entire current I_0 will be flows through this R_F . So, this is v_0 ; this is 0. So, the expression for $v_0 = R_F I_0$.

This is equal to I_0 is this expression if you substitute this here, this is $\frac{V_{ref}}{R_{ref}} R_F [D_7 2^{-1} + D_6 2^{-2} + D_5 2^{-3} + D_4 2^{-4} + D_3 2^{-5} + D_2 2^{-6} + D_1 2^{-7} + D_0 2^{-8}]$. So, this will produce the analog output correspond to the digital input D_7 to D_0 . As I have told, there is one important term like resolution of this D to A converter. This is one of the very important parameters for D to A converter as well as A to D converter. For D to A converter, the resolution is defined as the smallest change in the output voltage, which

may be produced at the output of converter.

Converter here is D to A converter. You can define this in a similar manner for A to D converter also. So, in order to better understand this, I will take an example. If I take 3-bit D to A converter with a full scale voltage of 5V. So, this will be having $2^3 - 1$ equal time intervals.

That is, if I take this input as digital. So, this is correspond to the line 1 1 1. This is correspond to 1 1 0. This is 1 0 1, 1 0 0, 0 1 1, 0 1 0, this should be equally placed 0 0 1, 0 0 0. Total will be having 8 levels, but 7 equal time intervals. This is important. So, this is one time interval; this is another time interval, this is third one, fourth one, fifth one, sixth one, seventh one.

There are 7 equal time intervals. This is correspond to digital input, but D to A converter output is analog output. If I assume that the full scale is 5V. So, the minimum voltage is 0V and maximum voltage is 5V. Now, what will be the voltage corresponding to one time interval, this voltage? So, you can easily see that there are total 7 time intervals. We are going to distribute 7 equal time levels are there for 5V; 7 equal time intervals is equal to 5V.

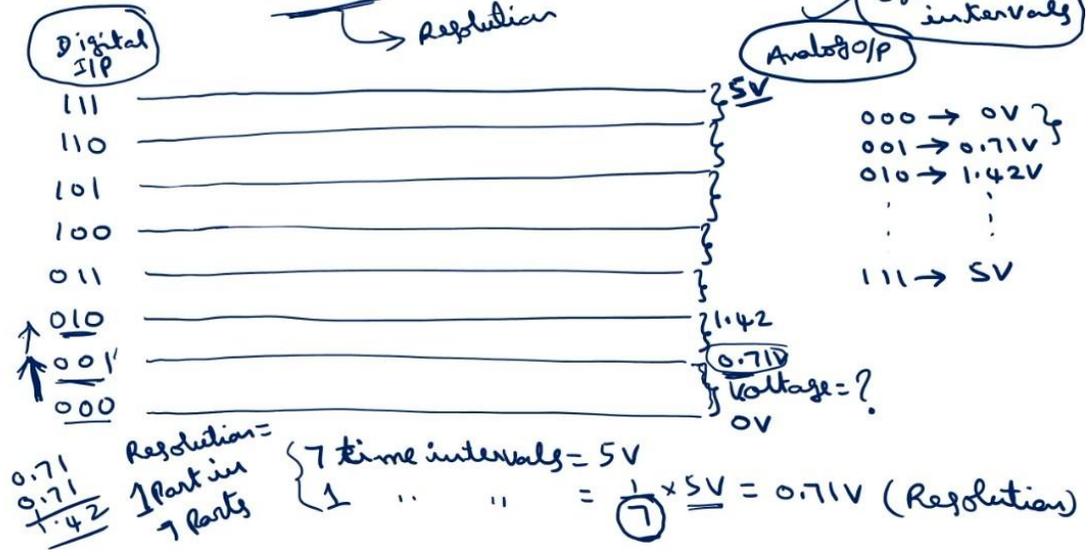
Then what is one time interval is equal to $\frac{1}{7} \times 5V = 0.71V$. This will come to say 0.71V. So, the meaning of this one is if I change from 0 0 0 to 0 0 1 or 0 0 1 to 0 1 0 with the minimum or the smallest change in the output voltage is this should be 0.71V. If I change this digital words by one increment or decrement, there will be smallest change in the output is 0.7V also this is called resolution. Now, this is 0.71 voltage corresponding to 0 0 1 corresponding to 0 1 0 0. $0.71 + 0.71 = 1.42$, like that if you goes on adding 0.7 0.71 finally, you will get here corresponding to 1 1 1 5V. So, if you find out this 0 0 0 is corresponding to 0V, 0 0 1 is corresponding to 0.71V, 0 1 0 is corresponding to 1.42V so on, 1 1 1 is corresponding to 5V. So, this smallest change that will be a produced at the output of the D to A converter is called as a resolution.

Resolution of D/A converter

N-bit D/A converter
 $\text{Resolution} = \frac{V_{FS}}{2^N - 1}$

The smallest change in the output voltage which may be produced at the output of D/A converter.

Ex:- 3-bit D/A converter with $V_{FS} = 5V$.
 $\frac{3}{2^3 - 1} = 7$
 Equal time intervals



(Refer to the slide at 41:39)

So, what is the expression for the resolution here? This is full scale voltage divided by 7 if it is a 3-bit D to A converter. In general, for a N bit DAC, the resolution is defined as $\frac{V_{FS}}{2^N - 1}$, here, N is equal to 3. This is 7 means $2^3 - 1$. In general, $2^N - 1$. So, for N bit D to A converter the resolution will be $\frac{V_{FS}}{2^N - 1}$.

Sometimes, this 3-bits this itself will be called as resolution. Sometimes the resolution is called as here in this case 1 part in 7 parts from here is equal to 1 part in 7 parts. There are different ways to represent the resolution, but the most commonly used resolution expression is this resolution of a N bit D to A converter is $\frac{V_{FS}}{2^N - 1}$, that is the smallest change in the output. If I change from 000 to 001 or any two consecutive code words, if I change from one code word to another adjacent code word then the change in the output voltage will be 0.71V. If I take an example, suppose there is a 9-bit D to A converter has a resolution of 10.3mV. If 000000000 produces 0V. What is the output voltage correspond to 10110, say 1111?

