Problem Solving
Lecture – 33
PLL Applications

In the previous lectures, we have discussed about the PLL, the components of the PLL such as a phase detector, VCO etc. And also, we have discussed about the PLL IC which is NE/SC 565. And this PLL is having lot of applications especially in communication. Today we will discuss some of the applications of this PLL. So, the first application is we can use this PLL for performing frequency multiplication or division. That is if input frequency is f_s we can obtain $\frac{f_s}{N}$ or Nf_s.

Block Diagram of IC 565:
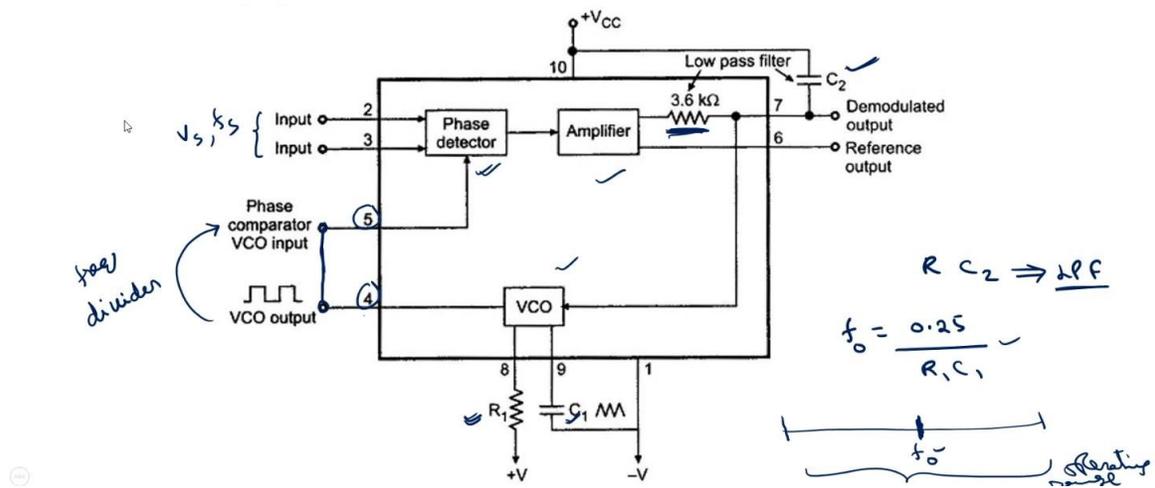
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If you consider the block diagram of the PLL, so the first block will be phase detector, input signal f_s, then low pass filter, error amplifier, VCO. Here the final output is taken. Now, as I have discussed in the previous lecture that the output of the VCO and the input of the phase detector, they are available as separate pins. Here you can see that between this 5, 5 is the input of the phase detector, 4 is the output of the VCO, these two are

opened.

As I have told in this frequency multiplication application, we have to connect one block such as a frequency divider or divide by N network. So, these two 4 and 5 are not connected. You have to connect a block between these 4 and 5. So, block here is divide by a network, if this frequency is f_0, here this frequency will be $\frac{f_0}{N}$. So, we know that at lock what happens? The input frequency and the VCO output in fact, the second input of this   phase   detector   will   be   same.

So, f_s becomes $\frac{f_0}{N}$ or $f_0 = f_s N$. This is what is called frequency multiplication. So, this $f_0 = N \times f_s$, where f_s is the input signal frequency, output signal frequency is equal to $N \times f_s$. By properly choosing the N value, we can multiply the input frequency by a factor of N. Basically, here divide by N network is a counter.
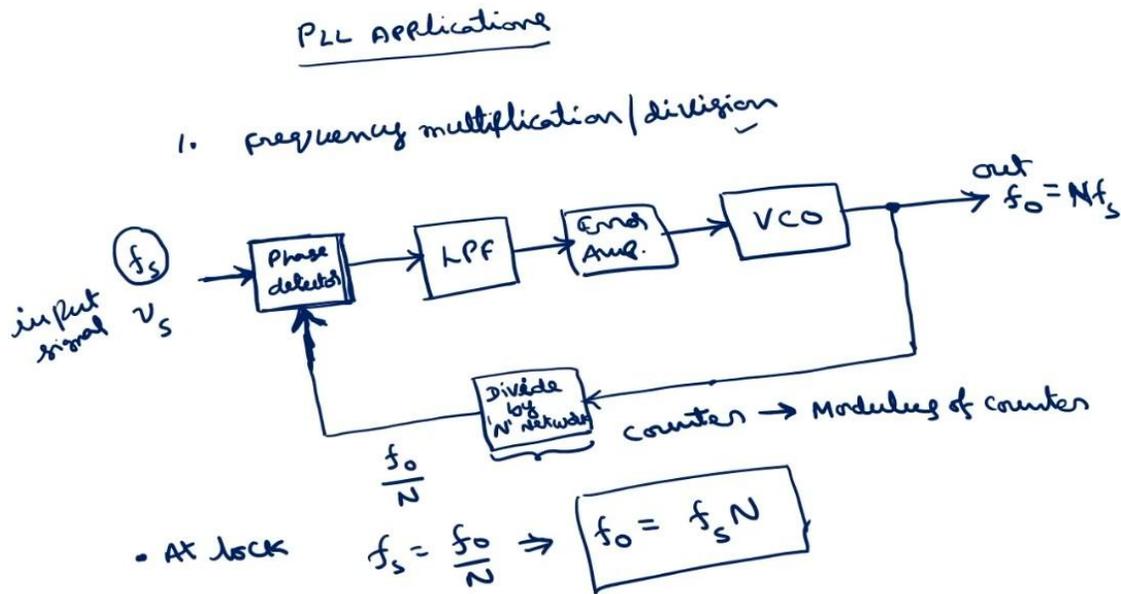
Then use a counter IC here. So, by properly choosing this counter, we can set N value. So, N value is actually the modulus of the counter. So, so we can perform the frequency multiplication using PLL. The second application is frequency translation.

If you want to shift the frequency of the input signal by a small amount, then we can use

PLL to perform this shifting of the frequency of the input signal. Here basically we will take this PLL block diagram. This is the phase detector, low pass filter, error amplifier, VCO. This is basically the PLL block diagram. The component that we have to connect externally are we will use a mixer or the multiplier whose one input frequency is f_s, another   is f_0.

Then low pass filter. These two blocks are external to this PLL. This is PLL block diagram. And the second input of this phase detector, we are going to choose f_1, where $f_1 \ll f_s$. This is the amount by which the frequency of VCO has to be shifted.

So, mixer is basically a multiplier. So, the output of this multiplier will be $f_s + f_0$, $f_s - f_0$. We can filter this $f_s + f_0$ by using this low pass filter. So, output here will be $f_s - f_0$. With lock what happens? This frequency and this frequency will be same that is $f_s - f_0 = f_1 \Rightarrow f_s = f_0 + f_1$.

So, we are going to shift the input frequency by a small amount of frequency deviation which is equal to f_1. This is what is called the frequency translation application using phase locked loop.
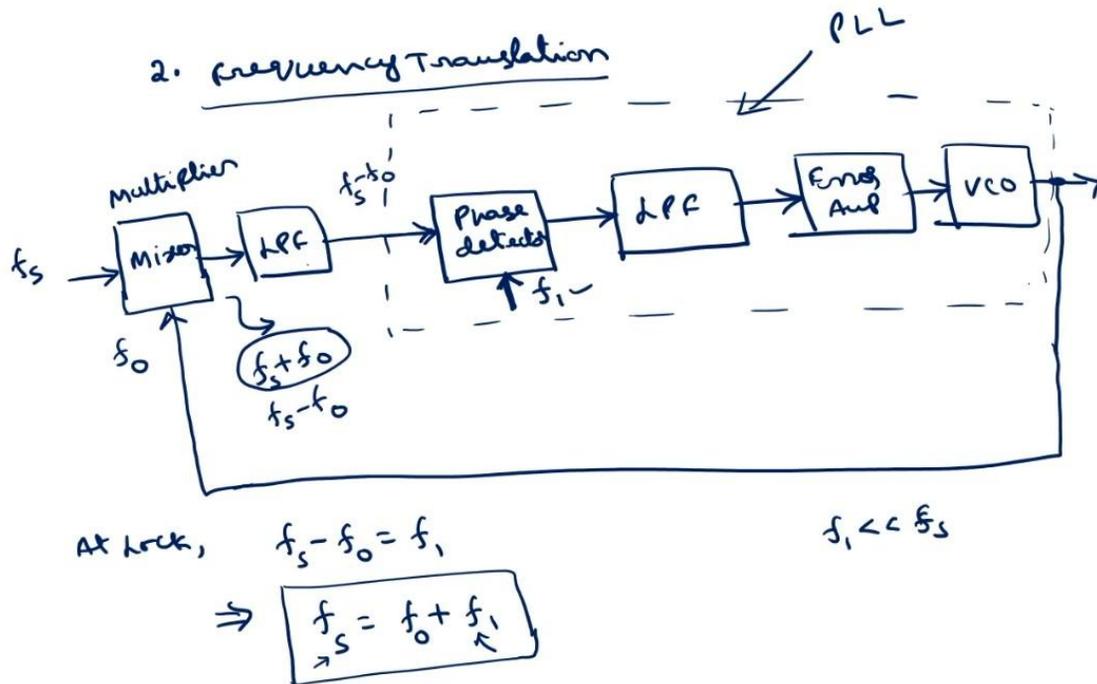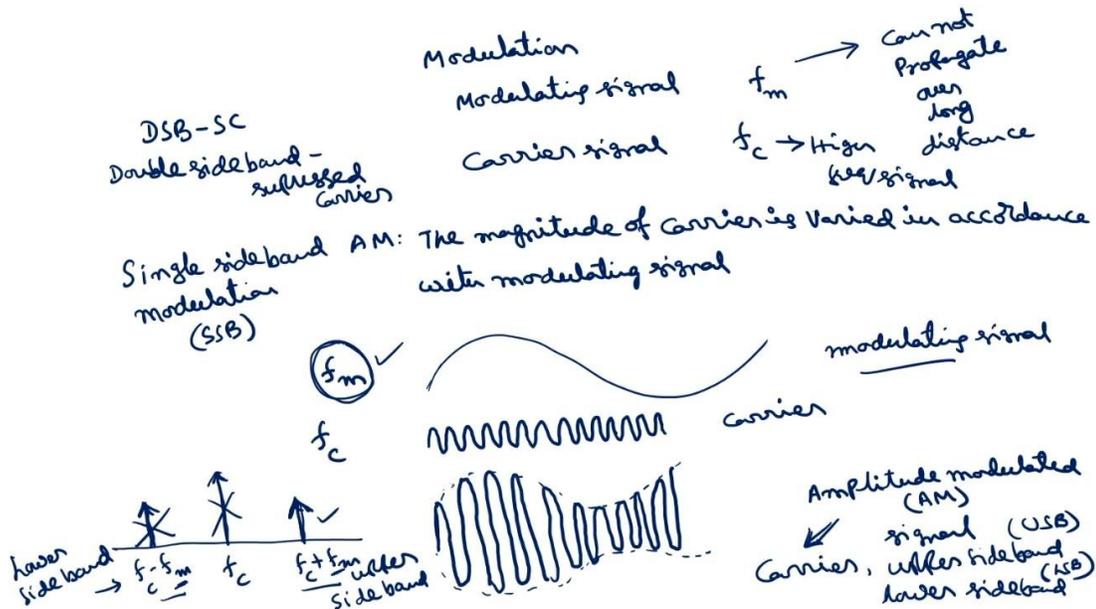

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The third application is AM demodulation or you can also call detection. Before going to draw the block diagram of AM demodulation, first I will discuss some basics of this AM and how this AM will be generated, what are the frequencies present in the AM signal. Modulation is process of carrying this information signal through a high frequency signal called as carrier.

So, there will be modulating signal, normally audio or video signal this is low frequency signal say FM is the maximum frequency component. If it is audio communication this frequency will be around 20 to 20kHz, but this cannot propagate over the long distance because of this low frequency cannot propagate over long distance. So, what we will do is we will take a carrier signal which is high frequency signal which is high frequency signal. In amplitude modulation the magnitude of carrier is varied in accordance with modulating signal. Suppose, if this is the modulating signal and this is carrier this is high frequency signal then amplitude modulated signal will be having envelope which is in the form of modulating signal, but the frequency is carrier frequency.

So, this envelope we are basically interested in order to demodulate this AM signal, you have to extract this envelope which is nothing, but demodulating signal. See in the time domain if you consider in the frequency domain if this is having frequency of f_m, if this is having frequency of f_c then this AM signal will be having frequency spectrum this consists of f_c as well as $f_c + f_m$ and $f_c - f_m$. There are different types of the amplitude modulations one is in full AM we will transmit both the sidebands this is called sideband, upper sideband and this is called lower sideband. So, AM signal consists of carrier upper sideband and lower sideband USB and LSB lower sideband, but actual information is present in only sidebands carrier does not have any information because actual interested is the actual the information is present in FM. So, there are different types of the techniques where we can suppress the carrier.

So, in one technique called as a DSB SC double sideband suppressed carrier as the name implies this will be deleted only these two sidebands will be sent through the transmitter. So, at the receiver from these two sidebands we can extract this modulating signal FM. So, in the other type of the AM we will suppress one of these sidebands also because here also we have this FM signal here also FM signal is there. So, one sideband is enough to extract the original modulating signal. If I suppress this lower sideband also then only one sideband is left that is called SSB single sideband modulation.

3. AM Demodulation (Detection)

Modulation
Modulating signal f_m → Can not propagate over long distance

DSB-SC
Double sideband - suppressed carrier

Carrier signal f_c → High frequency signal

Single sideband modulation (SSB)

AM: The magnitude of carrier is varied in accordance with modulating signal

f_m ✓

f_c ~~~~~~~~~~~~   carrier   modulating signal

lower sideband → $f_c - f_m$ f_c $f_c + f_m$ upper sideband

Amplitude modulated (AM) signal (USB)
Carrier, upper sideband (LSB), lower sideband

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So, this is how we can transmit the signal. So, at the receiver so, from this single sideband we have to extract the original modulating signal. So, how to achieve this modulating signal from the AM signal using PLL? If you consider the block diagram of the PLL for AM demodulation or detection this AM is first applied to the PLL. This is the complete PLL and here we require a 90 degrees phase shifter then this is applied to the multiplier whose one input is PLL output other input is 90 degrees phase shifter. Then you have to pass through the low pass filter then you will get demodulated AM.

Here we are going to apply AM signal. If I consider this AM as say SSB type of waveform then what will be the frequency here? $f_c + f_m$. Here what is the need of this 90 degrees phase shifter is we know that this PLL introduces 90 degrees phase shifter. So, in order to avoid that we will use 90 degrees phase shift so, that the two signals which will be applied for the multiplier these two will be in phase because this introduces 90 degrees phase shift. So, if I pass this AM signal also to 90 degrees phase shifter then this and this signal will be in phase.

So, this output is nothing, but VCO output inside this PLL we have VCO, VCO output we are going to apply to the multiplier. If I choose this VCO output $f_0 = f_c$ then what will be output of the multiplier is basically gives the sum and different components. So, here the frequency component is $f_m + f_c$ and here the frequency component is f_c. So, output

will be $f_{m+}f_c \pm f_c$ this is equal to $f_m + f_c - f_c$ is one component and other component is f_{m+} $f_c + f_c$. So, here this f_c, f_c will get will get f_m and this will be $f_m + 2 f_c$ this is large frequency and compare with this f_m. So, we can use the low pass filter to filter this larger frequency component. So, that output will be having frequency of f_m which is the modulating signal. This is how we can demodulate AM.
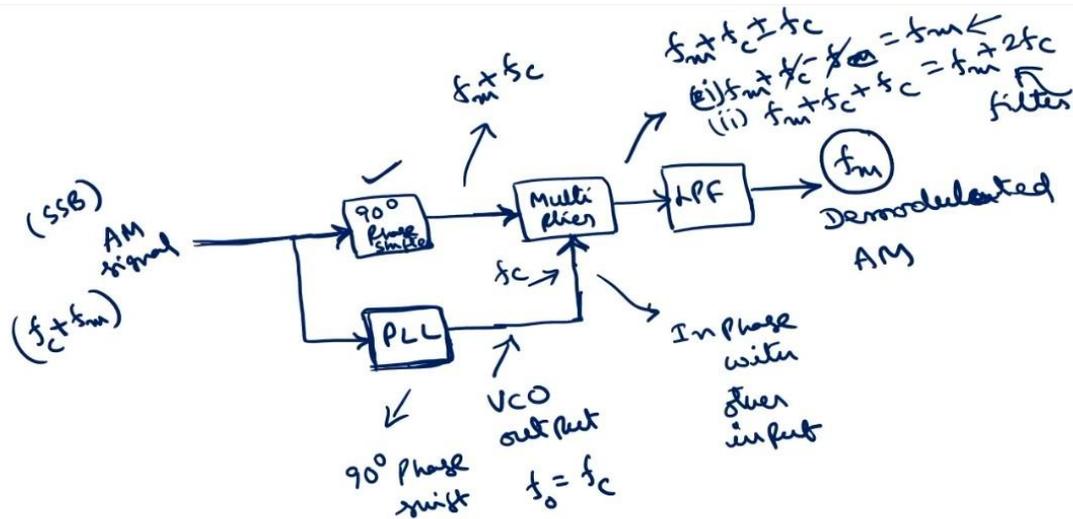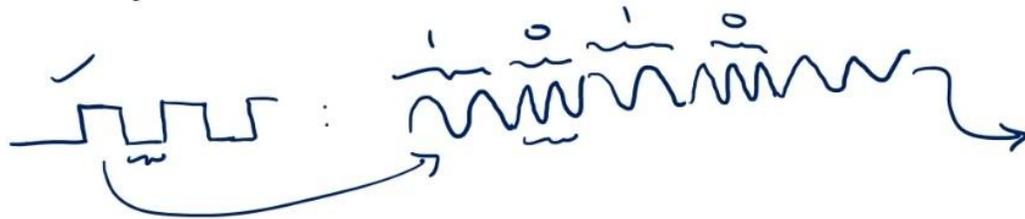

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So, the fourth application of PLL is PLL can be used as FSK demodulator. We know that the FSK can be modulated by using triplet 5 timer IC where we have seen that there will be two frequencies 1070 and 1270. This will be used for transmitting logic 0 this to logic 1. So, in FSK if I want to transmit 1 and 0 1 0 like that then this 1 will be transmitted by 1070 signal which is frequency is less means time period will be more this will be something like this and for logic 0 the second frequency which is 1270. For logic 1 again the larger frequency logic 0 smaller frequency like that you can transmit. This is logic 1 this is logic 0 because this is having less time period means more frequency this is logic 1 logic 0 so on. Now, this will be given as a input for the FSK demodulator from this you have   to   obtain   the   digital   data   ok.

 This can be performed by using PLL. So, the diagram of the PLL as FSK demodulator is this. So, this first part is FSK generator this you can use using triplet 5 timer which we have already discussed in the earlier lectures. Here are this IC 2 is IC 565 which is PLL. So, this part is generator which we have already discussed in the previous lectures.

4. FSK Demodulator :-

555 used as FSK modulator

1070 : Logic 1
1270 : Logic 0

So, here you will get this type of two signal this is logic 1 logic 0 so on. So, 1070Hz and 1270Hz signals. Now, this will acts as input for the this FSK demodulator. Here there is a capacitor C_3 and R_5. We know that the PLL will lock with the input frequency after   sometime   ok.

So, whatever the signal that is coming here PLL locks to input frequency and tracks between two frequencies that is 1070 and 1270 and provides two different DC shifts at the output of low pass filter. So, we know that the output of low pass filter will be connected to the VCO. This is v_c output voltage and here the frequency of this one varies with the v_c. Here you can see that in the circuit diagram the 7 we are going to take the modulating demodulated output for IC 565. So, this will be passed through this RC ladder   filter   which   removes   the   larger   frequencies.

So, we know that if you use a comparator you will get some frequencies and difference frequencies. The larger frequencies can be filtered by using this RC ladder filter. Then it is applied as one input for the comparator. The other input here is this is reference output.   You can see that for this 565 pin 6 will acts as a reference output.

So, we are going to choose this reference output as the average of these two DC shifts corresponding to this 1070 you will get some v_{c1}, it is the output of the low pass filter corresponding to this let v_{c2}. So, you will choose this reference voltage as the average of this v_{c1} and v_{c2}. So, depends upon the available signal here if this is corresponding to 1070 then you will get it the output logic 1, corresponding to 1270 you will get logic 0.

So, you will get here this type of logic 1 and 0s the output of this.

This is how you can demodulate the FSK. So, you will take here this logic 1, this is correspond logic 0. So, correspond to these two frequencies you will get two different DC shifts. The some or higher larger frequencies will be filtered by using this RC ladder filter. So, here we will be having two voltage levels v_{c1} or v_{c2} and here difference. So, we are going to choose this as a middle of this v_{c1} and v_{c2}.
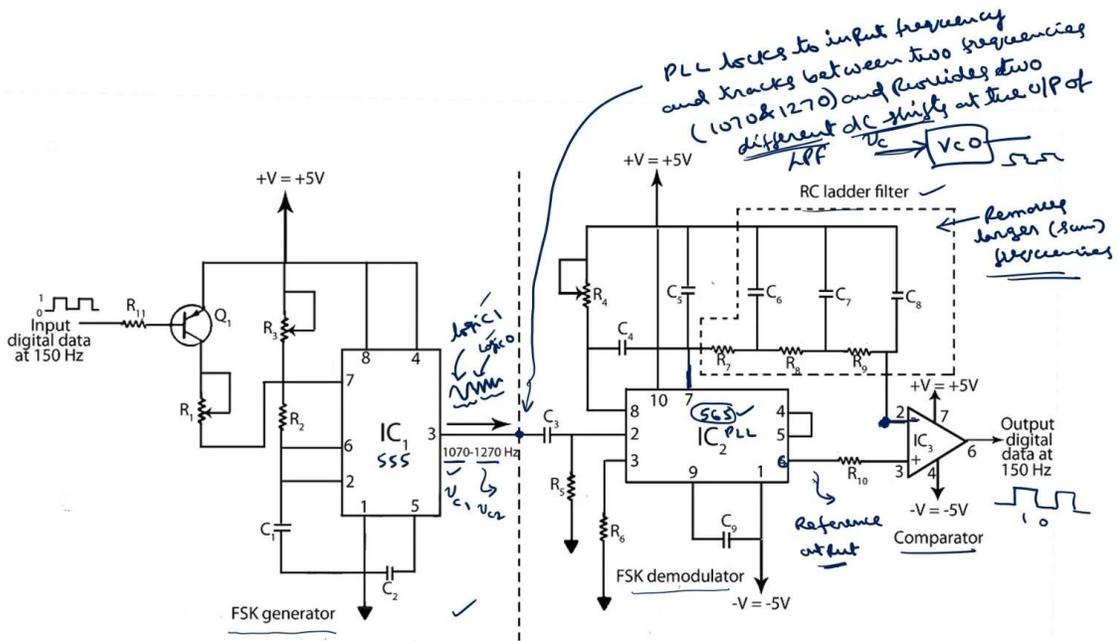
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So, depends upon whether this received signal is v_{c1} or v_{c2} output will get logic 1 or logic 0. This is how you can demodulate the FSK. Thank you.