Integrated Circuits and Applications
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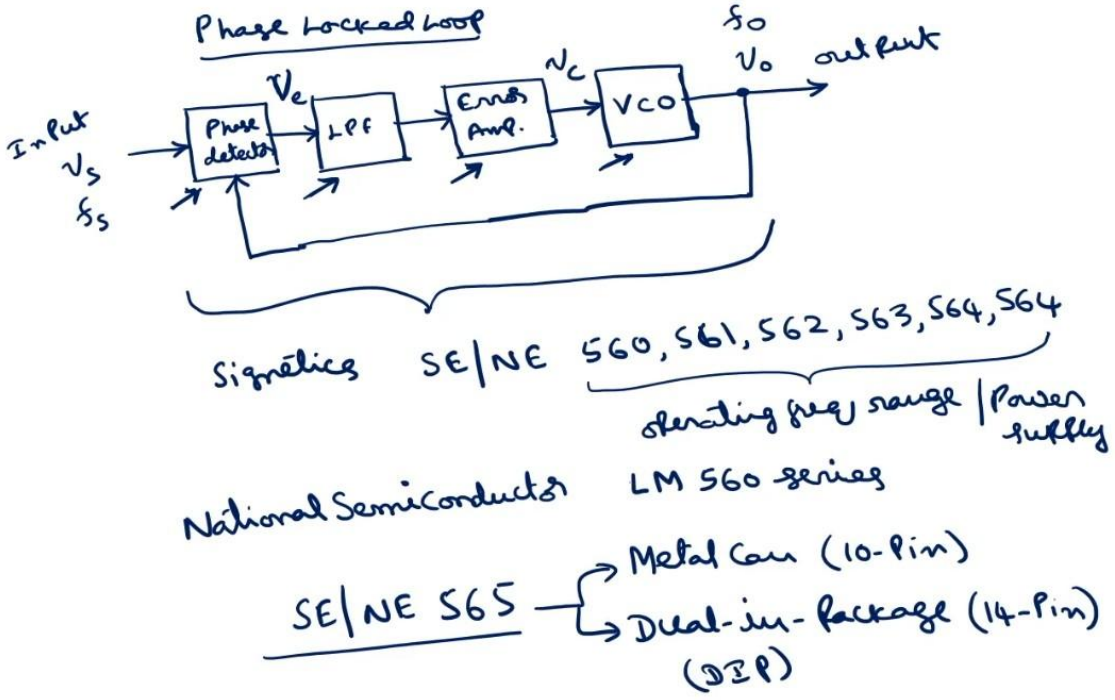
Problem Solving
Lecture – 32
PLL IC 565 Operation

In the last lectures, we have discussed the various building blocks of phase locked loops. First, we discussed about the phase detector, both analog type as well as a digital type. Then, low pass filter we have already discussed in the earlier lectures, then followed by error amplifier. Amplifiers also we have already discussed. Then, we discussed in detail about the voltage controlled oscillator. So, if we consider the PLL block diagram again here.

So, the first block is phase detector, followed by low pass filter, followed by error amplifier, voltage controlled oscillator, and this is the output, and a part of output will be compared with the input signal, this is the input signal. v_s is the input signal with the frequency of f_s, v_o is the output signal with the frequency of f_o. This phase detector will produce error signal, and error amplifier will produce control signal which controls the frequency of the VCO.

Now, we can construct this phase locked loops using the discrete components such as the phase detector, low pass filter, error amplifier and VCO. So, this phase detector can be again constructed using either discrete components or we have direct ICs. Similarly, for low pass filter also, we can use the ICR discrete components same for error amplifier and VCO. Whereas, this phase locked loop is also available in IC form. The signatic company has fabricated this phase locked loop in the form of a SE\ NE 560, 561, 562, 563, 564 and 565; they are called 560 series.

So, the only difference between these versions is the range of the frequency; operating frequency range is different, as well as the power supply, etc. There is another manufacturer called National Semiconductor. The PLL manufactured by a national semiconductor will be is LM 560 series. If I consider this SE\NE 565, this is available in two forms. One is metal can package 10 pin or dual inline package DIP this is 14 pin.



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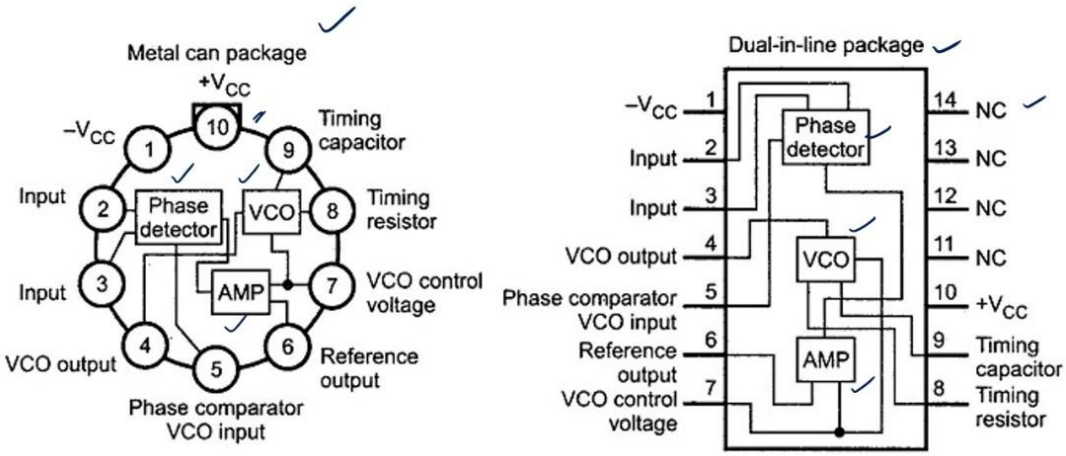
So, the pin diagram of this SE\NE 565 is like this. So, this is metal can package 10 pins, and this is dual inline package 14 pins. So, you can see that the internal blocks are phase detector VCO amplifier. Here, also you have phase detector VCO amplifier and the low pass filter you have to connect externally using R and C components. So, if you see the detailed block diagram of this 565 IC, you can see that here there is a $3.6k\Omega$ resistor is there, this will acts as R of a low pass filter and C we have to connect externally. So, this R and C_2 forms low pass filter. So, remaining blocks are already present phase detector amplifier VCO. This low pass filter will be implemented by using this $3.6k\Omega$ resistor and this capacitor.

Pin Configuration of IC 565:



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And another thing is here, the output of the VCO has to connect one input for this phase detector. That connection is missing here, 4 is available where the output of VCO can be taken, and 5 is the pin where the second input for the phase detector can be applied. So, these two inputs are basically for the input signal v_s the frequency of f_s; you can apply the single-ended input or a bipolar input. So, if it is single ended, then you can ground one of the inputs, if it is differential signal then you have to apply it two terminals. Now, why this connection is not made is in some of the applications, this VCO output will not be directly connected to the phase comparator.

We have to use some frequency dividers in order to implement the frequency multiplication application which we are going to discuss in the coming lecture. So, in such applications, we need to connect some external components between this pin number 4, which is the VCO output and pin number 5, which is the phase detector input. But for that, in the remaining applications, we can directly connect VCO output to the phase detector input by using a wire. Here this R_1 C_1 is going to decide the free running frequency of this VCO or PLL you can call as. So, for this IC565 this free running frequency will be given by $\frac{0.25}{R_1 C_1}$. So, this R_1 and C_1, you have to properly choose such

that free running frequency is $\frac{0.25}{R_1 C_1}$. As you have discussed in the earlier lectures, also you have to choose this free running frequency such that. So, it will be middle of the operating range of the PLL. If this is the operating range of the PLL, then at the center, you have to choose this f_o .

So, this can be designed by using proper values of R_1 and C_1. So, these are some details of IC565. So, we know that there are two important parameters for the phased locked loops: one is called capture range another is called lock in range. Now, we will derive the expressions for this capture range and lock in range of IC565. Before that, I will just recall the definitions of lock in range and capture range.

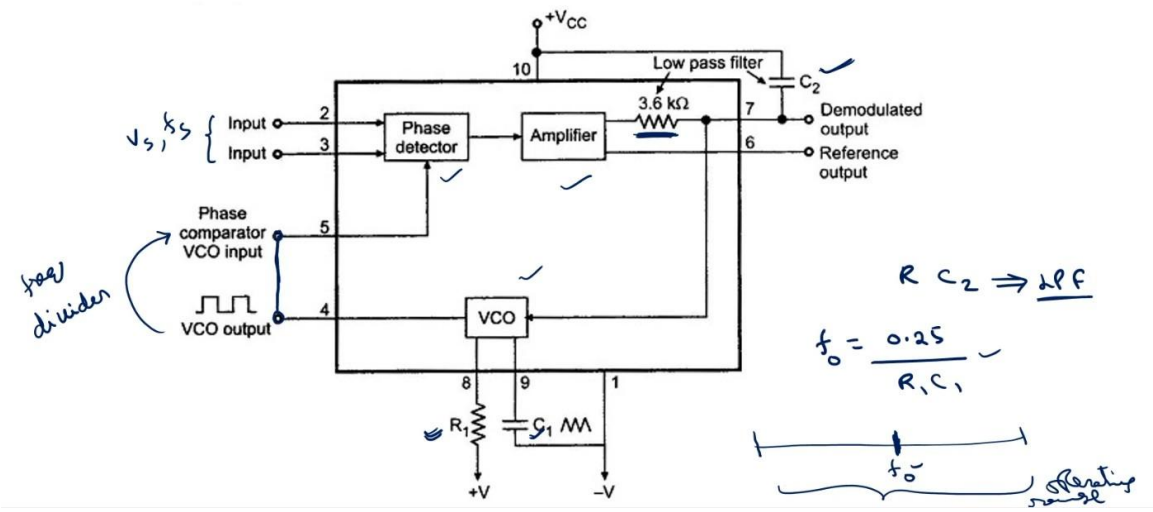
So, we know that the operation of this PLL is. So, you have the phase detector which compares the frequency and phase of the input signal and VCO output. Let phi is the phase difference. So, this will compare this f_s f_0 as well as the phase difference between these two signals. Accordingly, this will generate an error signal.

This error signal will be first low pass filtered and then amplified to generate a control signal, v_c which controls the frequency of VCO. So, that the phased locked loop can enter into the lock range. So, if I recall the operation of this PLL. So, this phase detector compares frequency and phase of the input signal and VCO output signal and generates an error signal v. This error signal will be low pass filtered and then amplified to filter high frequency component.

As we have discussed in the previous lectures that the phase detector is basically a multiplier. So, if you multiply two signals, one with a frequency of f_s another with a frequency of f_0, this will produce $f_s + f_0$ as well as $f_s - f_0$. So, these are the two frequencies present in the error signal v. So, this low pass filter will passes the low frequency that is $f_s - f_0$ and filters the $f_s + f_0$. So, this error signal frequency will be now $f_s - f_0$, and so is the frequency of this v_c also.

Error signal is amplified to generate control signal v_c. So, v_c also now will operate at $f_s + f_0$ only. So, this v_c will shift this control signal v_c shifts the frequency of VCO in a direction to reduce the frequency difference $f_s - f_0$. Initially, this VCO will operate at f_0, which is the free-running frequency. Now, the frequency will be shifted so as to reduce the frequency difference.

Block Diagram of IC 565:



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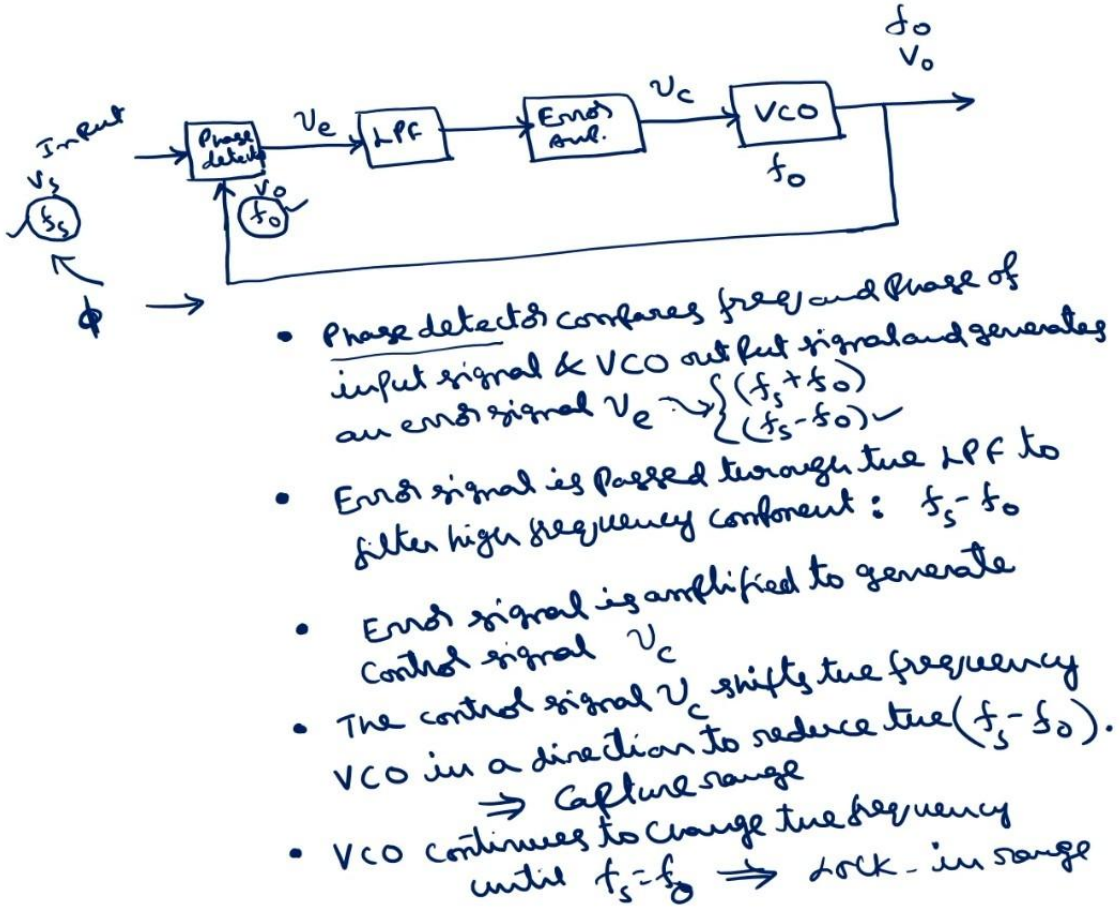
Once the stage is reached then the signal is said to be in capture range. In the capture range this v_c changes the frequency of VCO in a direction to reduce the difference between f_s and f_0. And the VCO continuously changes its frequency until $f_s = f_0$. So, once $f_s = f_0$ then the signal is said to be in lock in range. Once locked, whatever the variations of this input signal, f_s will be followed by the VCO output v_0.

So, this is the basic operation of this PLL. Now, we define this capture range as the range of frequencies over which PLL can acquire lock with input signal is called capture range. This lock in range is the range of frequencies over which PLL can maintain the lock with input signal. So, based on this background, now, I will derive the expressions for this lock-in range and capture range, especially for the IC565. First, I will consider the lock-in range derivation.



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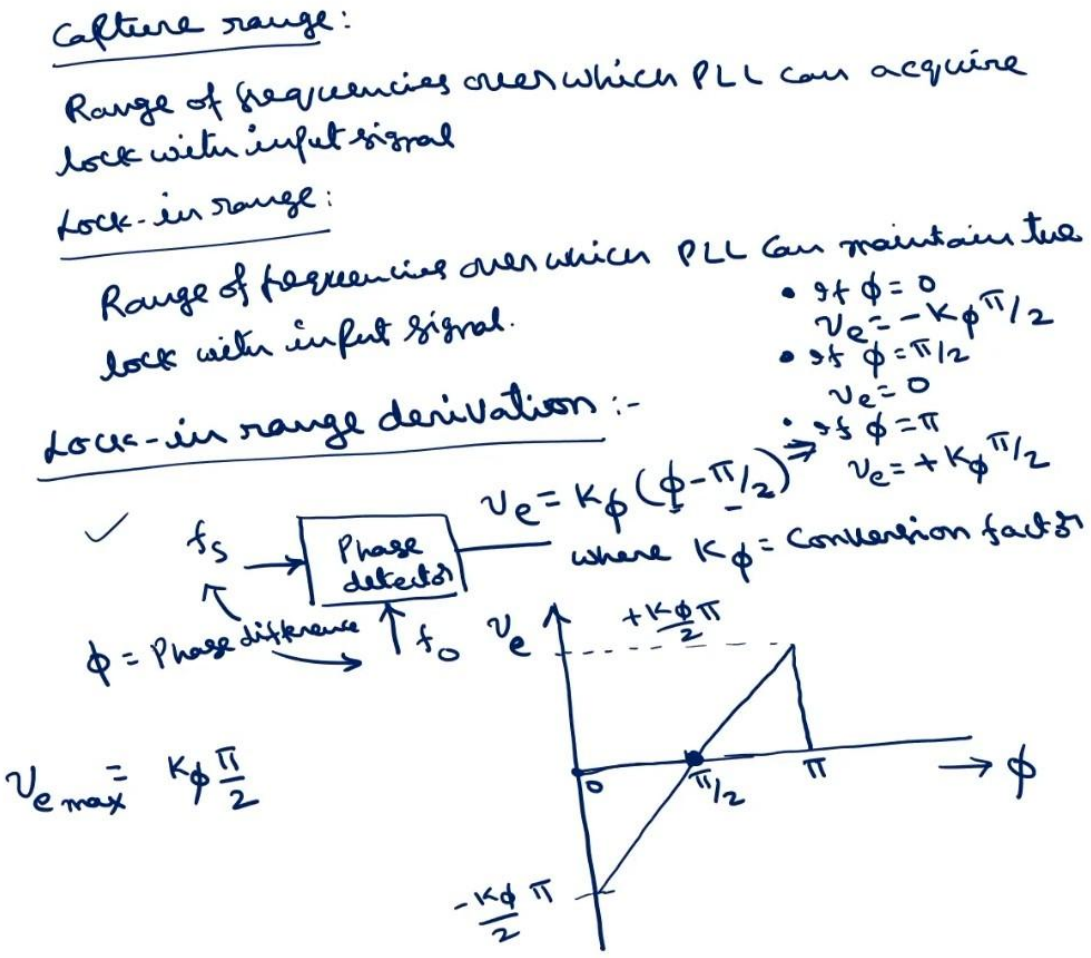
So, the first block in this PLL is phase detector. So, this will compare the frequency and phase of the input signal and VCO output and produce the error signal v_e. And the phase difference between the input and VCO output is ϕ. Then, in the previous lectures, we have discussed the various steps of the phase detector where this output error voltage $v_e = K_\phi(\phi - \frac{\pi}{2})$. So, the relation between the error voltage and the phase difference between the input and VCO output signal is $v_e = K_\phi(\phi - \frac{\pi}{2})$ where K_ϕ is conversion factor.

And if you plot this variation this will be something like this. This is ϕ, and this is v_e. We can see from here that at $\phi = 0$ here. This becomes 0. So, $v_e = -K_\phi \frac{\pi}{2}$.

So, if I take $\phi = \frac{\pi}{2}$. So, this phi by 2 pi by 2 get cancel will get $v_e = 0$. And if $\phi = \pi$, this value and then this $\pi - \frac{\pi}{2} = \frac{\pi}{2}$ as a result of that $v_e = +K_\phi \frac{\pi}{2}$. That is, the error voltage varies between $+K_\phi \frac{\pi}{2}$ and $-K_\phi \frac{\pi}{2}$.

At $\frac{\pi}{2}$ this is 0. So, this is the variation of this v_e. So, what is v_e? Maximum is the positive value which is equal to $K_\phi \frac{\pi}{2}$. So, this is the first block of this PLL. Now, the second block is low pass filter. Let us assume that low pass filter is having a unity gain ok.



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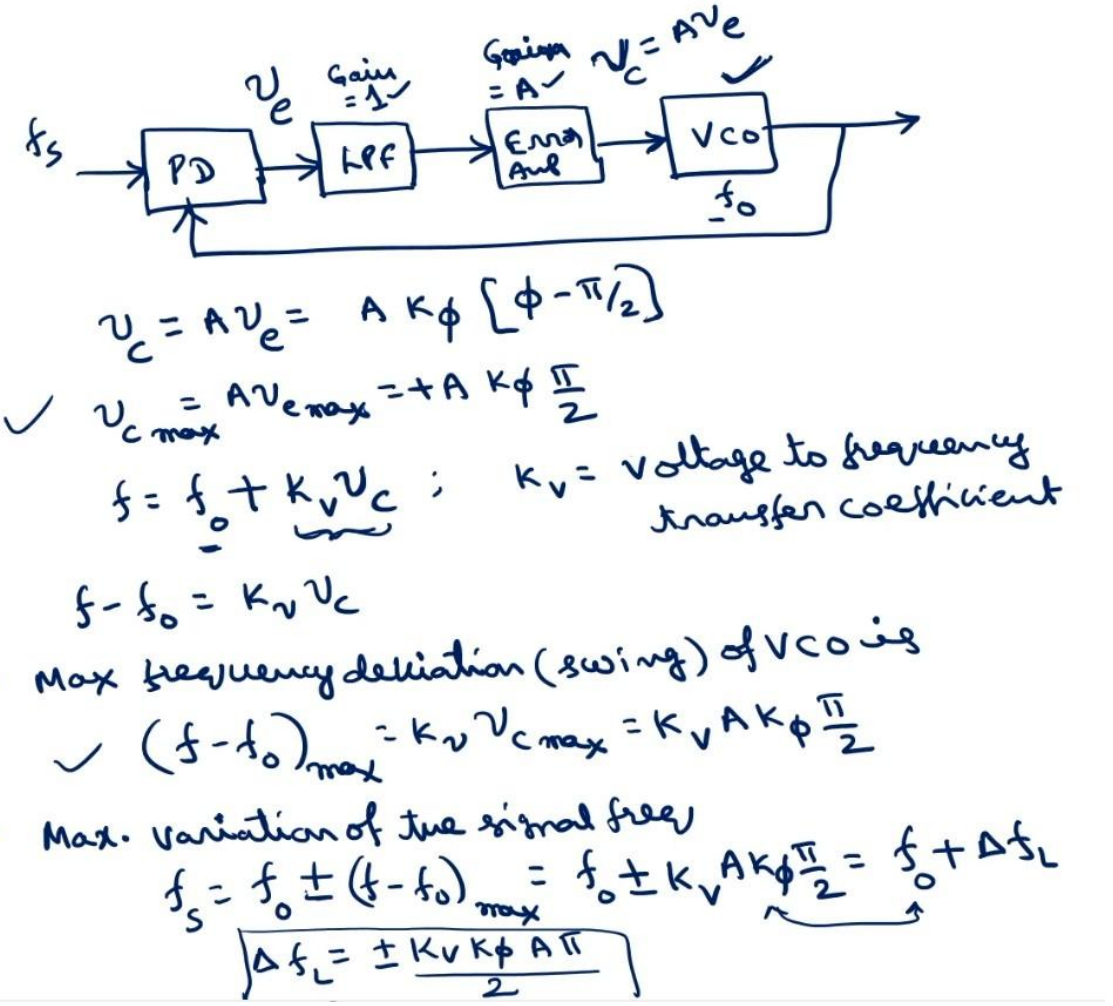
Then it will be passed through an error amplifier. This is phase detector, then low pass filter, then error amplifier. Now what is the expression for this PLL? Now let us assume that gain of this low pass filter is unity and the gain of error amplifier is say A and this will produce a control signal. So, this control signal $v_c = Av_e$.

Now, this gain is 1; this gain is A. So, v_c and v_e relation is this. $v_c = Av_e$ that is equal to

$AK_\phi(\phi - \frac{\pi}{2})$. And what is $v_{c\,max} = Av_{e\,max}$, which is equal to $+AK_\phi \frac{\pi}{2}$. This is the expression for the $v_{c\,max}$ which is the control voltage applied for the VCO. And let us assume that the VCO is having free running frequency of f_0, which will be decided by R_1 and C_1 the external components.

Now if I take the instantaneous frequency of VCO. So, it deviates from f_0 by a factor of $k_v \times v_c$. This is expression for the VCO instantaneous frequency where f_0 is the free running frequency. From this free running frequency, it will shift in either direction using this control signal v_c where k_v is voltage to frequency transfer coefficient. So, what is $f - f_0 = k_v \times v_c$. So, what is the maximum frequency deviation of VCO, also called as swing, is $f - f_0 = k_v \times v_{c\,max}$.



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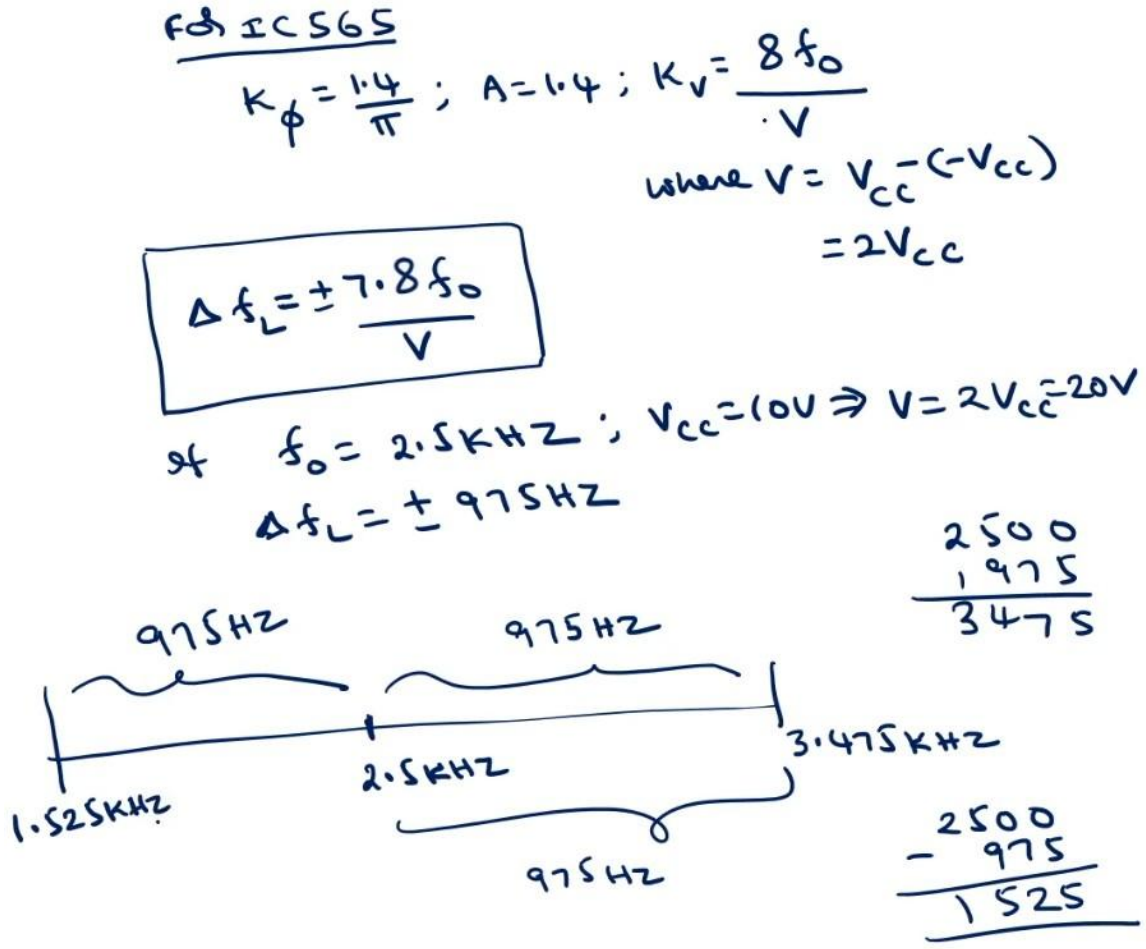
This is equal to $k_v \times v_{c\,max} = k_v A K_\emptyset \frac{\pi}{2}$. Now, if I take this variation of the signal frequency f_s maximum variation of the signal frequency is given by $f_s = f_0 \pm (f - f_0)_{max}$. So, initially, f_0 and that will vary between the limits f_0 to $f_0 - f$, $f - f_0$, $f_0 + f$. So, this is equal to $f_0 \pm k_v A K_\emptyset \frac{\pi}{2}$. So, in general, if I write this, should be in the form of $f_0 + \Delta f_L$, where Δf_L is the lock-in range.

The range of the frequencies over which the PLL can maintain the lock with the input signal frequency. So, if I compare these two expressions, what is the expression for the lock in range $\Delta f_L = \pm \frac{k_v K_\emptyset A \pi}{2}$? This is the expression for the lock in range of PLL. If I consider the IC 565 this $K_\emptyset = \frac{1.4}{\pi}$ and $A = 1.4$ and $k_v = \frac{8 f_0}{v}$ where $v = V_{cc} - (-V_{cc}) = 2V_{cc}$. If you substitute these values, then we will get the lock in range $\Delta f_L = \frac{7.8 f_0}{v}$. This is the expression for IC 565 means if I take this f_0 free running frequency as 2.5kHz then Δf_L will get as plus or minus and say VCC is 10 volts implies V is equal to twice VCC that is 20 volts.

Then we will get $\Delta f_L = \pm 975 Hz$. That is, this is the operating range. The central frequency is, say, 2.5kHz. So, this will be +975, that is 2500, + 975, that is 3.475kHz. So, this difference is 975Hz this difference is also 975Hz and this will be how to subtract 2500 - 975.



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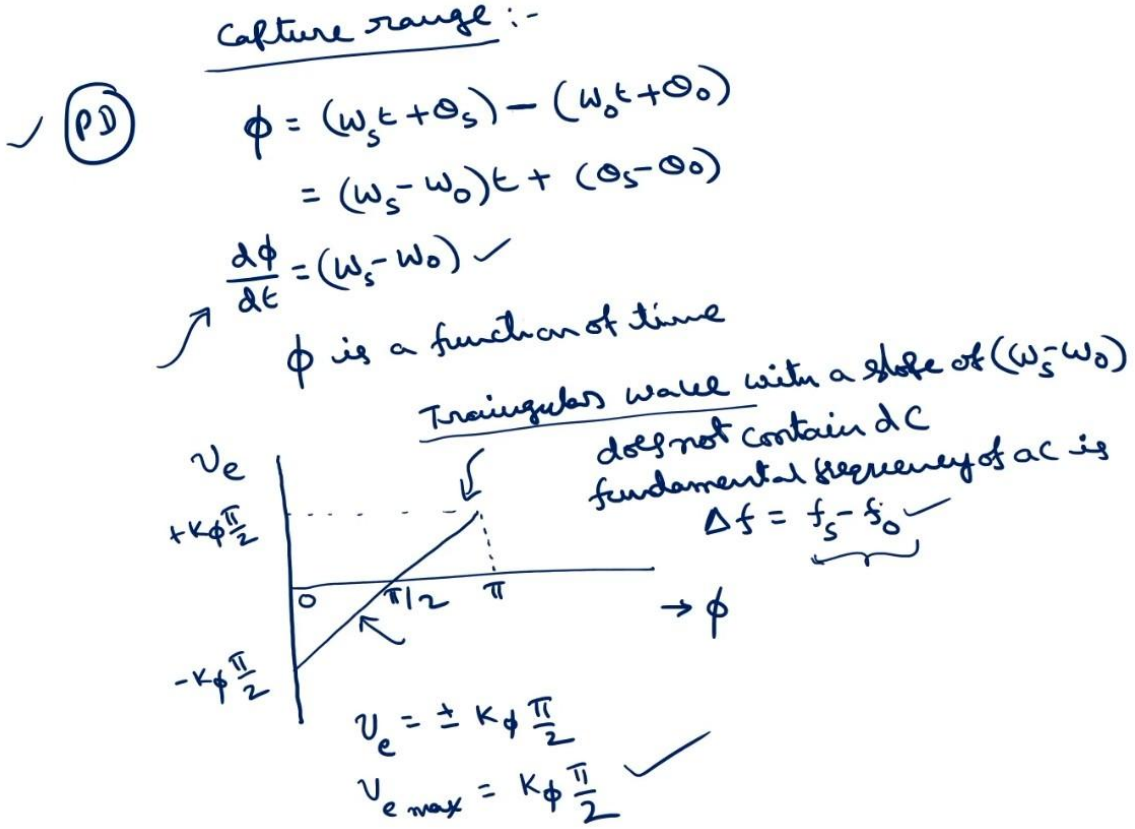
This is around 1525Hz, 1.525kHz. So, this is about the derivation of lock in range. So, the next derivation is capture range. So, the phase difference between the input and VCO output will be in the general form as $\emptyset = \omega_s t + \theta_s$ is this a the input signal frequency and corresponding phase minus VCO output is $\omega_0 t + \theta_0$. This will be the difference component will be filtered by low pass filter and some components will be filtered by low pass filter difference component will be passed through the low pass filter. So, if I take this difference as $(\omega_s - \omega_0)t + (\theta_s - \theta_0)$.

So, this phase difference between the input signal and VCO output is not a constant, it is a function of time. If I take the $\frac{d\emptyset}{dt}$, you will get as $(\omega_s - \omega_0)$. That is, $\emptyset$ is a function of time and the variation of $\emptyset$ with t. If I plot it will be a triangular view with a slope of $(\omega_s - \omega_0)$. This we have already discussed in the previous slides also, and see the error

voltage produced by this phase detector as a function of ∅. This is the range of the frequencies. The slope of this one is $(\omega_s - \omega_0)$. So, this is $+K_\emptyset \frac{\pi}{2}$ at π, 0 at $\frac{\pi}{2}$, this is $-K_\emptyset \frac{\pi}{2}$.



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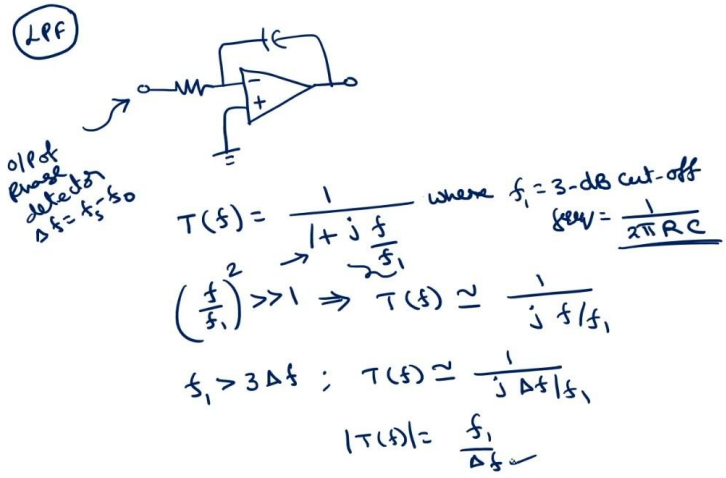
So, this is the output of the first block. So, in the derivation of lock in range, we assumed that low pass filter is having unity gain, whereas, here in the capture range derivation it is important to consider the frequency characteristics of low pass filter also. Because in the lock-in range, once the lock is achieved. So, the output simply follows the input variations. There is no change in the frequency, whereas, in the capture range. So, the difference between the frequencies will produce a control signal which changes or shift the frequency of the VCO in a direction to reduce the difference between the f_s and f_0. So, we need to consider the frequency characteristics of low pass filter also.

So, this is about the phase detector the first block of PLL where $v_e = \pm K_\emptyset \frac{\pi}{2}$ or $v_{e\,max} =$

$\pm K_\emptyset \frac{\pi}{2}$ first block. Second block is low pass filter. So, we know that the low pass filter can be constructed using R and C components. Here, the input to this one is output of the phase detector. So, what is the output of the phase detector? This is because this is triangular type of waveform this does not contains DC.

And there are some AC components with a fundamental frequency of $\Delta f = f_s - f_0$. This is angular frequency this is the edge frequency. So, there will be some fundamental frequencies and the harmonics of this one will be there that higher frequencies can be filtered by using the low pass filter. Here the output of the phase detector with a fundamental frequency of $\Delta f = f_s - f_0$ is applied to the low pass filter. The transfer function of the low pass filter is in the form of $\frac{1}{1+j\frac{f}{f_1}}$, which we have already discussed in the earlier lectures, where f_1 is the 3 dB cutoff frequency given by $\frac{1}{2\pi RC}$.

Here, if this $\frac{f}{f_1}$ square, if I take the magnitude of this transfer function, if it is much much greater than 1, we can neglect this 1 when compare with this. So, T(f) will be approximately equal to $\frac{1}{j\frac{f}{f_1}}$. And again, if I consider that this $\Delta f < f$ or $f_1 > 3\Delta f$. Then this TF can be approximated as $\frac{1}{j\frac{\Delta f}{f_1}}$, or if I take the magnitude, it will be $\frac{f_1}{\Delta f}$ is this Δf is the frequency deviation. So, this is about the second block, which is the low pass filter.



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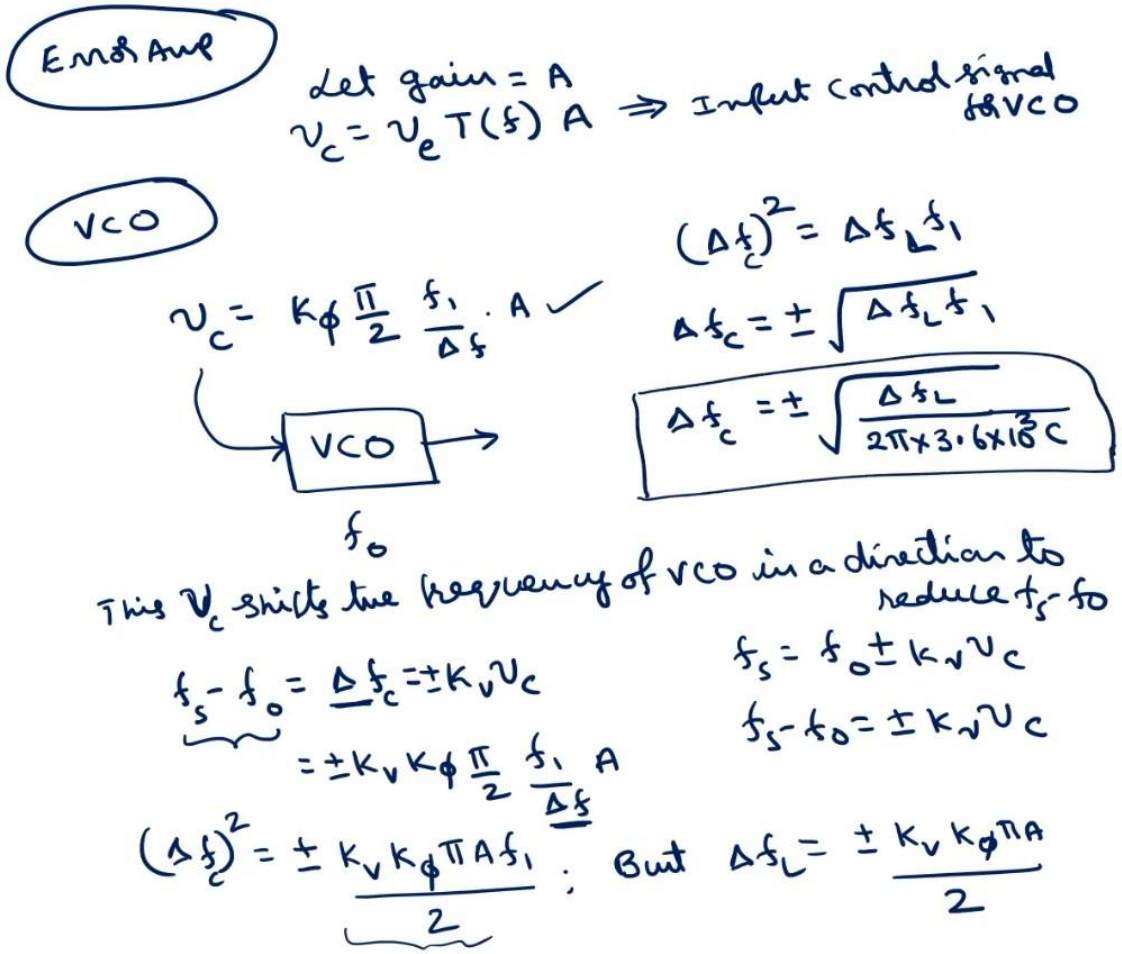
So, we have considered this phase detector whose output is this and consists of various harmonics and fundamental frequency of Δf. Now we will pass through the low pass filter whose transfer function will be in the form of $\frac{f_1}{\Delta f}$. Then the next block is error amplifier. This basically provide some gain let the gain of this error amplifier is A; this is independent of the frequency.

Then the last block is VCO. So, what is the output of the error amplifier then is v_c. So, this v_c nothing but $v_e T(f) A$, here we have considered the transfer function as unity. So, this *T(f)* is not there now *T(f)* is this transfer function then what is v_c? $v_c = v_e T(f)$. So, we will get v_c as v_e is the error signal then pass through the low pass filter whose transfer function is *T(f)* and output of the low pass filter will pass through the error amplifier whose gain is A.

Now this will be the input for the VCO. So, if you substitute these values, v_c is equal to v_e value, will be $K_\emptyset \frac{\pi}{2}$ and $T(f) = \frac{1}{\Delta f}$ into A. This v_c will change the frequency of the VCO from the free running frequency f_0. This v_c controls in a direction to reduce the $f_s - f_0$. So, what is the corresponding $f_s - f_0$ that we will get is proportional to v_c? So, $f_s - f_0$, which also we will calling as Δf, k_v into v_c because we already discussed that $f_s = f_0 \pm k_v v_c$ or $f_s - f_0 = \pm k_v v_c$.

So, what is this v_c is this? This is equal to $k_v K_\emptyset \frac{\pi}{2} \frac{f_1}{\Delta f} A$. So, this is also Δf. This is also Δf. If you take to the other side, this is $\Delta f^2 = \pm \frac{k_v K_\emptyset \pi A f_1}{2}$. But we have derived the expression for the locking range as $\Delta f_L = \pm \frac{k_v K_\emptyset \pi A}{2}$. So, this entire thing except this f_1. So, therefore, what happens to $\Delta f^2 = \Delta f_L f_1$.

So, this Δf which is the different between f_s and f_0 will acts as a capture range then, also called as this Δf or Δf_c . Now, what is $\Delta f_c = \pm\sqrt{(\Delta f_L f_1)}$ this is equal to $\pm\sqrt{(\frac{\Delta f_L}{2\pi \times 3.6 \times 10^3 C}}$), that C is in the farads this is the expression for capture range of PLL.



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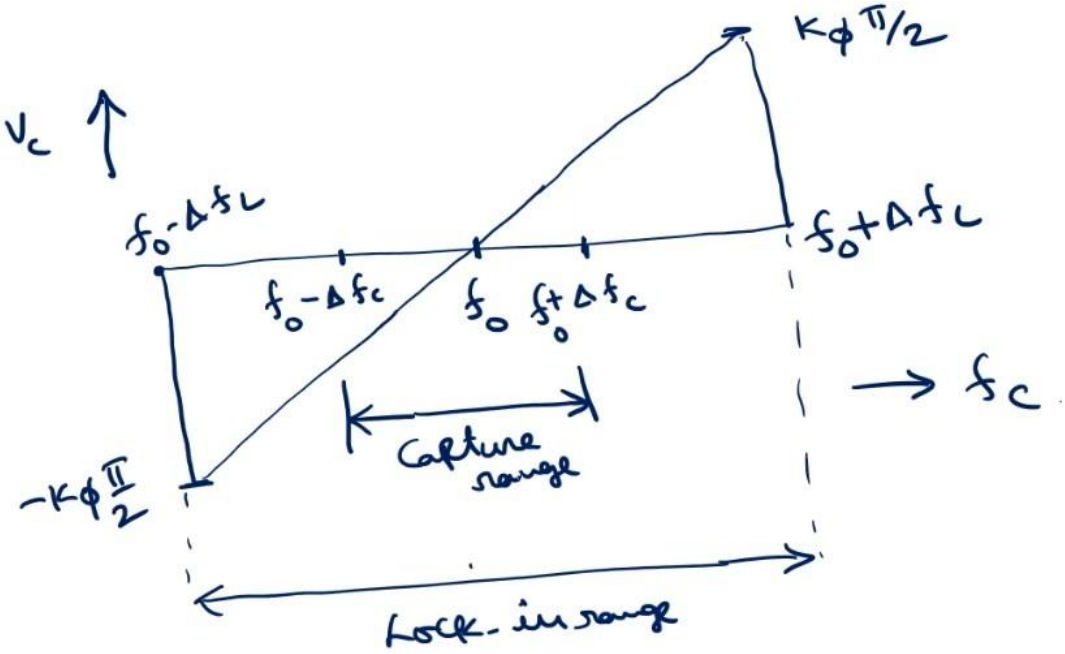
These are the two important parameters of this PLL. Now, if I consider the overall graph v_c versus f_s, this is f_0 this is the range of this is f_0 free running frequency this is $+\Delta f_c$, $-\Delta f_c$ from f_0. So, this particular range is called as capture range and from this f_c from here to here is called lock in range. This will be $f_0 + \Delta f_L$. This is $f_0 - \Delta f_L$, and these peak values are this is $K_\emptyset \frac{\pi}{2}$, this is $-K_\emptyset \frac{\pi}{2}$.



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So, this is the relation between this f_0 and capture range and lock-in a range of 565 PLL. So, this is about the operation of the PLL and PLL is having plenty of applications. Especially we can use this PLL to perform the frequency multiplication division AM demodulation, FM demodulation, FSK demodulation. We have lot of applications of this PLL. We will discuss these applications in the next lecture. Thank you.