Integrated Circuits and Applications
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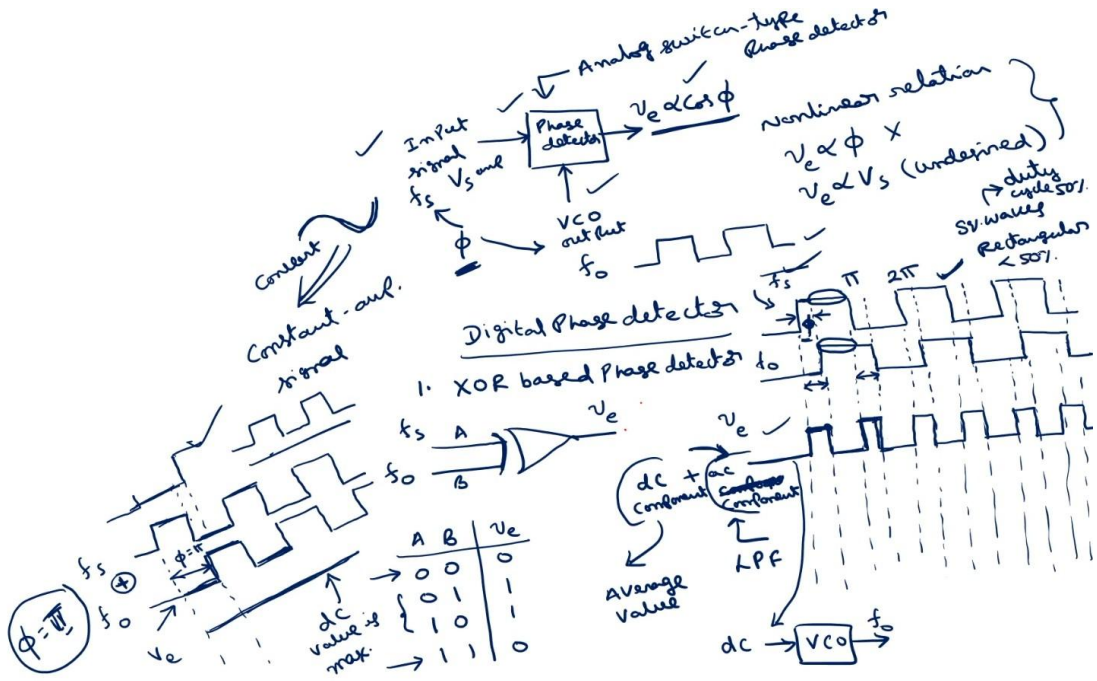
Problem Solving
Lecture – 31
Voltage Controlled oscillator

In the last lecture, we have discussed about the analog switch type phase detector. So, basically, a phase detector have two inputs, one is the input signal with a frequency of f_s and second one is VCO output with a frequency of f_o. You see normally square or rectangular type of waveform; here this is sinusoidal or any other signal this is phase detector, this will produce some error signal. If you have the phase difference between these two signals as $\emptyset$. So, in the last lecture, we proved that $v \propto cos\emptyset$. And we have discussed two drawbacks of analog switch type phase detector, one is this non-linear relation.

It is instead of $v \propto \emptyset$, it is $\propto cos\emptyset$. Second one is this v also depends upon the amplitude of this input signal, which if you call as v_s, V is also $\propto v_s$, which is undesired. To avoid these two problems with the analog switch type phase detector, we have to convert this input waveform into constant amplitude type signal such as square or rectangular wave. So, there are different circuits which converts this type of signals into square or rectangular waves.

So, once if you convert this input signal into constant amplitude signal, then this is also square or rectangular wave, and VCO output is also square or rectangular wave. Now, because these two are pulse type of the signals, we can perform this phase detection using some digital circuits also. There are some digital phase detectors. So, the first digital phase detector is exclusive or based phase detector. Simply exclusive OR gate will acts as a phase detector.



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If it is exclusive OR gate, if I give one signal with a frequency of this f s, another signal with a frequency of VCO output f naught, then this will generate V error signal. So, we know that if A and B are the inputs of the signal, what will be this VE? This is the truth table, which finds out the VE values for different combinations of the A and B 0 0, 0 1, 1 0, 1 1, 0 0 for exclusive OR gate. If the inputs are equal, the output is 0; if inputs are different, output is 1. So, here if I apply this f_s with some frequency, say this is f_s signal. Let us assume that the ∅ is the phase difference between f_s and f_o. If f_o is this signal, f_s will be a differ by ∅, so this difference between these two is ∅ .

Then what will be the output? Output v_e will be so, here during this portion f_o is signal is 0 whereas, f_s signal is logic 1. So, output is logic 1. During this portion, both are 1s. So, output is 0. During this portion one of the input signal is at logic 1, other is at logic 1 input signal is at logic 1, another is at logic 0s output is 1.

So, like that we will get a pulses like that we will get this type of waveform at the output of the exclusive OR gate. So, this waveform will be having both the DC component as well as AC component. Because, you know that any arbitrary signal can be represented as sum of DC and infinite sinusoidals using Fourier series. So, this also will be having DC component as well as some AC components. So, these AC components can be filtered by using a low pass filter. Only DC will be left.

So, we will get the average value of this. So, average value of this waveform can be obtained by passing through the low pass filter and selecting the proper cutoff

frequency. Now, this DC voltage of this one that is average value of this DC value, will be applied to the VCO, which changes the frequency of the VCO. Now, what will be the range of this DC signal and when does this DC signal will be having maximum value? You can easily see that this $\emptyset$ this is the $\emptyset$ difference now this is having high from this point to this point. If I slightly increase this phi what happens? So, this width will be increases if you goes on increasing this width will be increases until $\emptyset = \pi$.

If the difference $\emptyset = \pi$. what type of waveforms will get? We will get something like this. If this is f_s, f_o is having phase angle of π, then this will be having now this phase angle is π. If you exclusive these two, this is exclusive operation. During this portion, this $f_o = 0$ whereas, $f_s = 1$, during this portion $f_s = 0$ whereas, $f_o = 1$ during this portion, $f_s = 1$, $f_o = 0$. So, we will get v_e signal which is a constant signal. So, this will be having maximum DC value.

So, we will get the maximum DC value for $\emptyset = \pi$. So, if I plot the DC voltage as a function of $\emptyset$ phase angle from 0, it will increase up to π again from π it will decreases. You can see that this is $\emptyset = \pi$. If you further increase this $\emptyset$ what happens? We will get some phase difference. If I take this at a phase angle of more than π, then this will be something like, instead of becoming this as high here, it will become high after some time.

So, because during this portion, output is 1 and as during this portion, output is 0. So, you will not get constant waveform. You will get pulsed waveform like this. So, if I goes on increasing the phi from 0 to pi, the DC voltage will increase. After π. Again, the DC voltage decreases up to 2π, and the same cycle will repeat. And if I assume that the maximum DC voltage is V_{CC} and if the V_{CC} is 5V. And what is the conversion factor of this phase detector is the output by input.

For a 0 to π phase difference you are getting the output voltage of 5V. So, $K_\emptyset = \frac{5}{\pi} V/rad$. So, this is the exclusive OR based phase detector, and the DC output voltage can be maximum V_{CC} at $\emptyset = \pi$. But what is desired in the phase detector is this linear variation between the $\emptyset$ and the DC voltage has to be extended over a long range. So, if I want to extend this linear range from 0 to 2π instead of having 0 to π, we can use an edge triggered SR flip flap based phase detector.

So, we can see that here, this edge triggered SR flip flap based phase detector will be having this phi and DC output voltage linear relation up to 0 to 2π. This is one advantage. Another advantage is instead of taking these f_s and f_o square waves, we can take rectangular waves. That means, square wave is having duty cycle of 50 percent, whereas, the rectangular wave will be having duty cycle less than 50 percent. So, because of this, you can increase the linear range. How this linear range will be increased? We can study through this circuit.

So, this is SR flip-flap, this is Q and Q bar, this is clock, and this clock is, say, positive edge triggered, and here f_s is applied, here f_o is applied. So, what is the truth table of SR flip flap? SR Q n Q n plus 1. If it is 0 0 previous state is 0 present state is also 0 0, 0 1 present state is also 1, simply present state is equal to previous state. For 0 1 regardless of the previous state output is equal to 1 because reset input is 1. For 1 0 regardless of the previous state output is equal to this is 0 because reset input is equal to 1 this is 1 and 1 1 is not allowed.

So, this table will be active at the negative edge or the positive edge sub Q. If I take the clock we will be having 4 portions. This is clock the variation from logic 0 to logic 1 is called as positive edge and this particular portion is called as positive level and the variation from logic 1 to logic 0 is called as negative edge or trailing edge and the portion where this is equal to logic 0 is called as negative level. We can design the flip flap which is sensitive to either of these 4 portions. Here, I am assuming that this particular flip flap is sensitive to the positive edge means whenever this S or the R input changes from 0 to 1, then only this follows this two table.

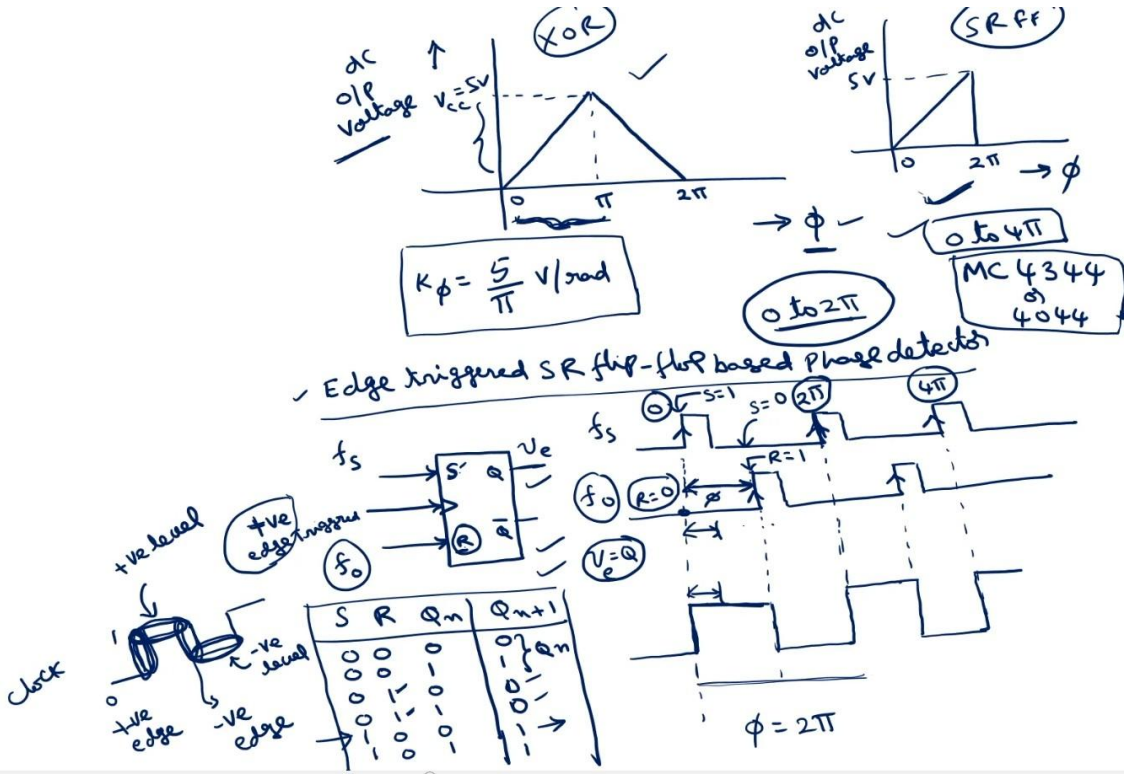
In any other case during this region during this region simply output remains in the previous state. Now, if I apply this waveforms, say this is f_s waveform, and this is f_o waveform. So, the phase difference will be now this much. This is also positive edge. This is also the positive edge between two positive edges. This is the phase difference 5. So, what will be output Q is nothing, but this is output V. So, what is output V or which is equal to Q? So, at this point here, because f_s is changing from 0 to 1 and f_s is connected to the S input.

So, S is becomes 1 and f_o is connected to R. So, here, this $R = 0, S = 1, R = 0$ this makes output is equal to 1. So, output is equal to 1 here, this is either V or Q how long this will be 1 up to this point. So, at this point, this is the R input because f_o is connected to R. So, R becomes 1, but whereas here, S is 0.

So, $S = 0, R = 1$ means output is 0. So, this becomes 0 and again at the second positive edge of this f_s this becomes high second positive edge of f_s it becomes 0, third positive edge it becomes again 1 and so on. Now, this is 0 total, this is 1 time period, 2π , this is 4π and so on. Suppose if this phase angle is 0.

So, this is ambiguity state. So, if you increase this phase angle from 0 towards 2π, now this much is the output voltage for this phase angle. If you decrease the phase angle instead of this if I take the phase angle as this then this portion also will decreases. If you increase this will increase until this 2π. So, when phase angle $\emptyset = 2\pi$, what happens? You will get this as a maximum DC signal. So, if I plot this relation here now this will be 0 to 2π it will raise the maximum.

So, this is the difference between this exclusive R based and SR flip flap based. So, this is having more linear range. So, this is a better phase detector, and if you want to increase this range further, you can have up to 0 to 4π linear range. For that, you can use the phase detector IC such as MC 4344 or 4044. This is a direct IC which performs the phase detection, but the linear range will be more when you compare with exclusive R gate based phase detector and SR flip flap based phase detector. So, this is the phase detector this is one of the important block of the phase locked loop.



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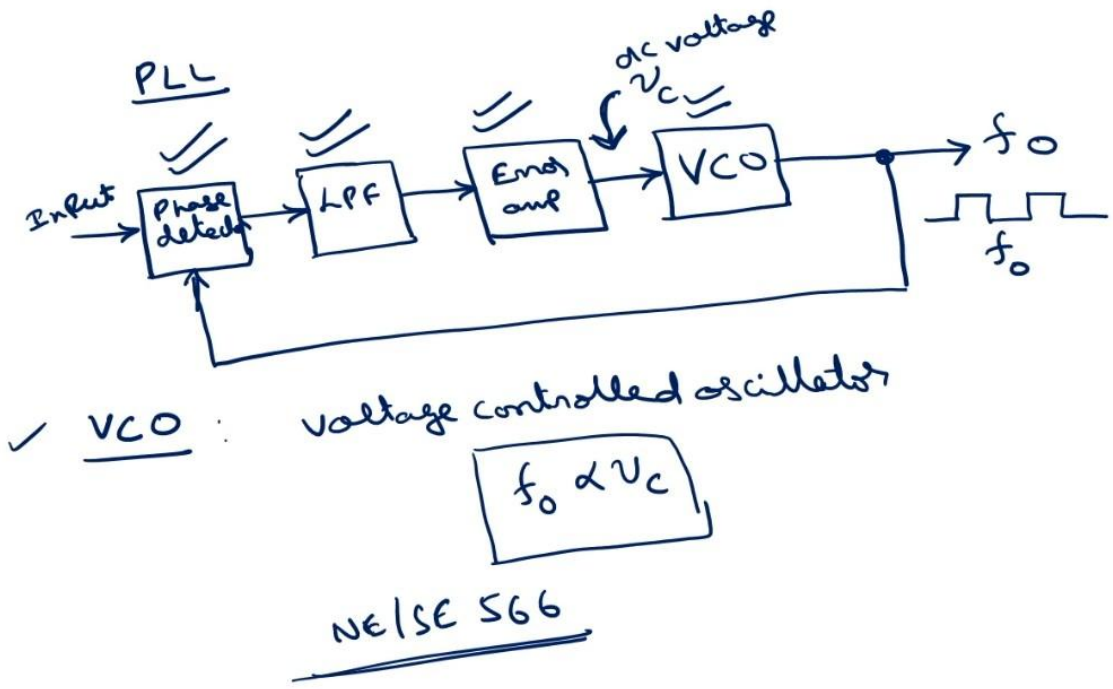
So, what are the other blocks of the phase locked loop? As you have discussed in the earlier lecture, this is the phase detector, which compares the frequency and phase of the input signal and VCO output and generates an error signal will be passed through the low pass filter. So, that you will get the DC signal that will be amplified by error amplifier, then it will be applied to the voltage control oscillator whose frequency varies with input DC voltage, voltage control oscillator. Here this is the final output and a part of this output will be fed back to the phase detector. Now, we have discussed about this phase detector and low pass filter. We have already discussed in the earlier lectures how to design the low pass filter using Butterworth approximation and amplifiers also we have already discussed in the earlier lectures. Now, another important block is VCO.



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So, now, we will discuss about the voltage controlled oscillator. So, the input for this one is DC control voltage output is waveform whose frequency varies with this DC voltage. If I call this DC voltage as v_c frequency as f_o, $f_o \propto v_c$. So, and what is the relation between the f_o and v_c? In order to derive this relation, we will consider the block diagram of VCO, which is available in the IC form of NE/SE 566. This is an IC which performs this VCO operation.

If you consider the block diagram of this VCO which is NE/SE 566 this is the block diagram of VCO. You can see that there are different blocks one is constant current as source, or this can be sink also, and there is a Smith trigger then buffer amplifiers these are internal to this IC external we have one resistor R_1 resistor R_1 capacitor C_1 and there is a provision to apply the modulation input and this is V plus which is nothing, but V_{CC} and this is ground point. So, before going to explain the operation of this VCO I will first revise the operation of the Smith trigger because the main building block of this VCO is Smith trigger. So, in the previous lectures, we have discussed about the Smith trigger circuit this is the circuit diagram of a Smith trigger. Here, the input voltage v_i is applied, and here, the output voltage v_o is taken. A part of this output voltage will be fed back to the input. This is v_{ref}, R_1, R_2, and this will be having $+v_{sat}$, $-v_{sat}$. So, the output of this one swings between this $+v_{sat}$ and $-v_{sat}$. $-v_{sat}$ depends upon the voltage at input and voltage at the inverting terminal. And we have derived the expression

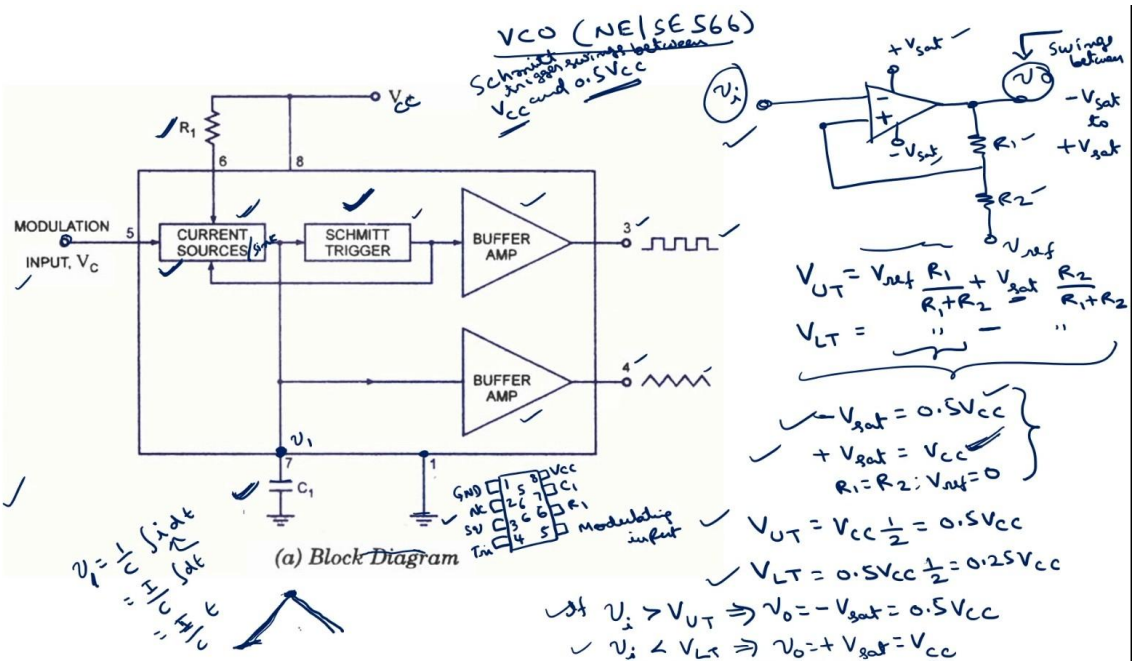
for the upper trigger point and lower trigger point V_{UT}, which we have defined as $v_{ref}\frac{R_1}{R_1+R_2}+v_{sat}\frac{R_2}{R_1+R_2}$, assuming that this v_o swings between $-v_{sat}$ to $+v_{sat}$.

And V_{LT} we have defined as the lower trigger point the same expression here, but minus sign. This Smith trigger, which is present inside this VCO, we are going to design to swing between V_{CC} and 0.5 V_{CC}. That is, in this expression, $-v_{sat}$ will be the lower value that lower value here is 0.5 V_{CC}

The highest value is V_{CC}, so that will be $+v_{sat}$, and inside this Smith trigger, we are going to choose $R_1 = R_2$. So, with these assumptions, what is V_{UT} and v_{ref} also 0 inside this? So, this will be 0, $+v_{sat}$ becomes V_{CC} into R_2 is equal to R_1 means this becomes half this is equal to 0.5 V_{CC}. V_{LT} becomes the first term is 0 because v_{ref} is 0 minus half v_{sat} becomes $0.5V_{cc}\frac{R_2}{R_1+R_2}$ because $R_1 = R_2$ it is will be $\frac{1}{2}$ this becomes $0.25V_{CC}$. So, the upper trigger point is 0.5 V_{CC} lower trigger point is 0.25 V_{CC}. And the operation of this Smith trigger is if the input voltage $v_i > V_{UT}$ the output voltage v_o becomes this is $-v_{sat}$ here $-v_{sat} = 0.5V_{cc}$. If $v_i < V_{LT}$, v_o is $+v_{sat}$. So, in this IC we have $+v_{sat}$ as V_{CC}. So, now, if I discuss the operation of this VCO, there is a external capacitor which is connected at the 7th point, and one is grounded.

So, this is in the IC form. If we take this in IC form, this is an 8-pin IC 566. The first pin is grounded. So, this is connected to the ground second pin is no connection. So, here 2 is not there third one will be the point where square wave is generated you can see that at third point square wave is generated fourth pin triangular wave is generated. Fifth pin is modulating input, this sixth pin will be R_1, this external resistor we are going to connect seventh pin is C_1, this external capacitor you have to connect and eighth pin is V_{CC}. Now, this capacitor is charged or discharged by using a constant current source or it can be sink.

So, whenever this capacitor charges this will acts as a source whenever the capacitor discharges this will acts as a sink, but this will provide the constant current. If constant current is provided if I assume that this voltage is v_1. So, what is the expression for the voltage across the capacitor $\frac{1}{C}\int idt$? If this current supplied by this constant current source is constant say I capital I this you can take outside the integration I is the constant current supplied by this constant current source $\int dt$. So, this becomes $\frac{I}{C}t$, that is, the voltage across the capacitor increases linearly. It will charge linearly as well as discharge linearly.



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But what are these points? What is the lowest voltage? What is the highest voltage? This depends upon the V_{UT} and V_{LT}? So, if I plot this voltage across the capacitor and voltage at the output of the Smith trigger it will be something like this. This is v_1 voltage across the capacitor. So, this will increase linearly and decrease linearly because of the constant current. This is the type of waveform we will get across the capacitor.

And what is the condition for this Smith trigger? If $v_i > V_{UT}$, which is nothing, but 0.5 V_{CC} output is 0.5 V_{CC}, and $v_i < V_{LT}$, which is 0.25 V_{CC}, $v_o = +V_{cc}$. So, here, if this capacitor voltage have the two limits one is upper trigger point, another is lower trigger point.

This will be acts as a lower trigger point of Smith trigger which is 0.25 V_{CC} and this is upper trigger point 0.5V_{CC}. So, whenever the capacitor charges, if it charges to a value which is slightly more than the upper trigger point of this Smith trigger, then what will be the output 0.5 V_{CC}? So, here this was V_{CC} and here this becomes 0.5 V_{CC}. So, from here, what happens is because this output of the Smith trigger will be 0.5 VCC. So, it causes the capacitor to discharge. This is the discharging path whenever this capacitor voltage discharges to a value which is equal to 0.25 V_{CC} which is V_{LT}. If it is slightly less than V_{LT}, what will be the output? If it is slightly less than V_{LT}, output is V_{CC}. So, this Smith trigger output becomes V_{CC}. Similarly, again the same cycle it repeats. So, these are the waveforms at the input and output of Smith trigger. The input waveform is nothing but the voltage across the capacitor, which is a triangular view.

Of course, we require the buffers and here this is a rectangular view. This is now what is the frequency of these signals? As the name implies, voltage control oscillator, this frequency has to vary with the input voltage. So, in order to derive the expression for the frequency if I assume that this is the time period of either triangular view or square view voltage across the capacitor v_1 is given by C into D v_1 by Dt. v_1 is the voltage across the capacitor.

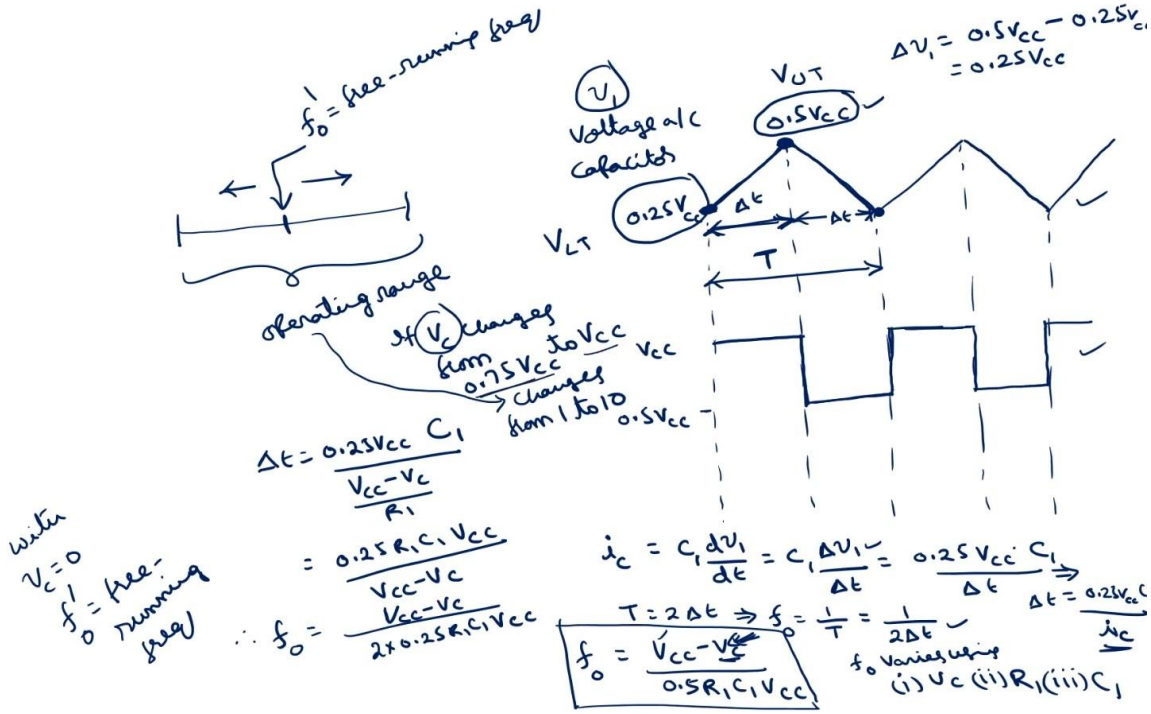
So, this can be written as $C\frac{\Delta v_1}{\Delta t}$. So, what is Δv_1? The change from here to here. Here, this is 0.25 V_{CC}. Here, 0.5 V_{CC}, and this is v_1 waveform.

So, Δv_1 will be the highest value, which is 0.5 V_{CC} minus the lowest value, 0.25 V_{CC}. This will be 0.25 V_{CC}. This is equal to $\frac{0.25V_{cc}C}{\Delta t}$. So, this is the voltage change from here to here we are calling as Δv and the corresponding time change also we can call as Δt. Then what is the relation between the capital T and Δt? This is $2\Delta t$. This is another Δt. So, capital T, the period of either triangular or square view is equal $2\Delta t$, or if I call as frequency $f_o = \frac{1}{T}$, frequency of either triangular or square view is equal to $\frac{1}{2\Delta t}$.

So, from here, what Δt? $\frac{0.25V_{cc}C}{v_1}$, and this is I current through the capacitor i_c. $I = C\frac{dv}{dt}$. This is the current i_c. But what is i_c? i_c is this current which will be supplied to this one. So, this 5 is at voltage of VC, 6 is also at voltage of v_c because there is a capacitor connected between the 5 and 6. We are going to connect a capacitor between the 5 and C externally, that I am going to discuss later.

So, the voltage at 5 and 6 will be same. So, this is v_c, and this is V_{CC}. This current is i_c. So, $i_c = \frac{V_{cc}-v_c}{R_1}$. So, $\Delta t = \frac{0.25V_{cc}\times C}{\frac{V_{cc}-v_c}{R_1}}$ and this is of course, C_1 because we are using the notation C_1 and R_1.

So, imply this is equal to $\frac{0.25R_1C_1V_{cc}}{V_{cc}-v_c}$. This is Δt, and what is f? $\frac{1}{2\Delta t}$, $\frac{1}{2\Delta t}$, $\frac{2\times 0.25R_1C_1V_{cc}}{V_{cc}-v_c}$ that goes to the numerator.



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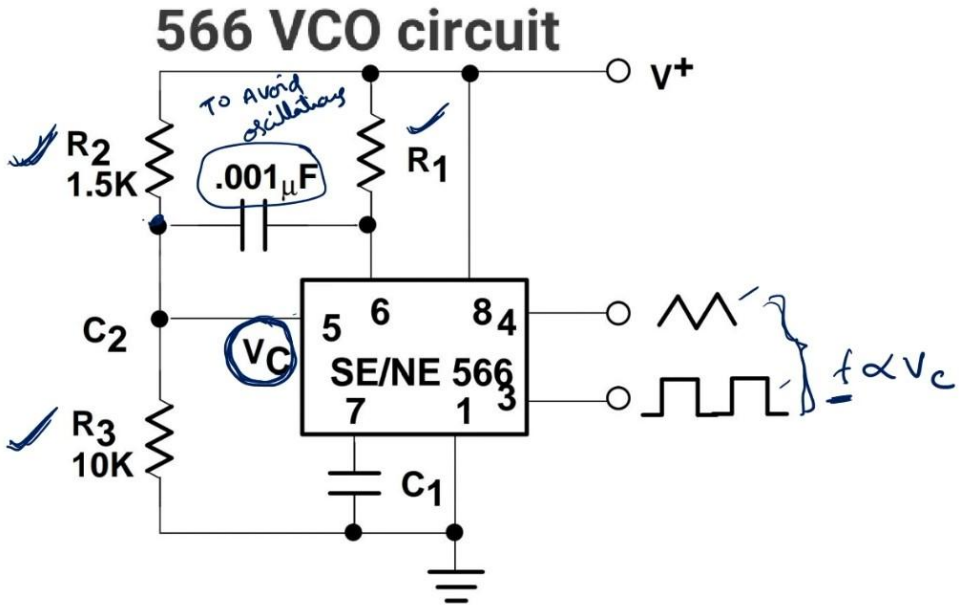
This is expression for the frequency of VCO 0.25 into 2 becomes 0.5. So, we can see that this f_o can be varied by varying either you can vary v_c, V_{CC} is constant, v_c is variable, or you can vary the external resistance R_1, or you can vary external capacitance C_1. So, if I want to operate this VCO over a some operating range, say this is the operating range of VCO. When this modulating input $v_c = 0$, whatever the frequency that you are going to get, you call this one as say, f_c', this is free running frequency when this is 0 that normally we will set in the center, this is free running frequency. Then, by changing this v_c, we can change this f_o' in either directions.

So, it can be shown that if v_c changes from 0.75 V_{CC} to V_{CC} the operating range changes by 10 fold 1 to 10. So, like that by changing the v_c, we can change the frequency of the VCO keeping this R_1 and C_1 as constant. Then, how to change this v_c, say from 0.75 V_{CC} to V_{CC}? For that, we need to connect two more resistors at the modulating voltage and the complete circuitry, which is required to generate the triangular and square wave at the output of the VCO, whose frequency varies with the v_c. This v_c is this one is this R_1 and R_2 we are going to connect here, and as I have told, 5 and 6 will be this is the 5 point, and this is 6 point only capacitor is connected between these two. This is used to avoid the oscillations.

Using this R_1, R_2 and R3, this R_1 is, of course; we are going to fix R_1 and R_2 by varying this R_2 and R3. We can vary the v_c. If v_c varies frequency of this square wave and triangular wave also varies. So, this circuitry is used to generate this

square and triangular wave whose frequency varies with the input modulating voltage v_c.



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So, this will be varied by using R_2 and R_3. So, see about the VCO operation. So, with this knowledge of the all the blocks of PLL. So, we will consider the complete PLL circuit in the next lecture. Thank you.