Integrated Circuits and Applications

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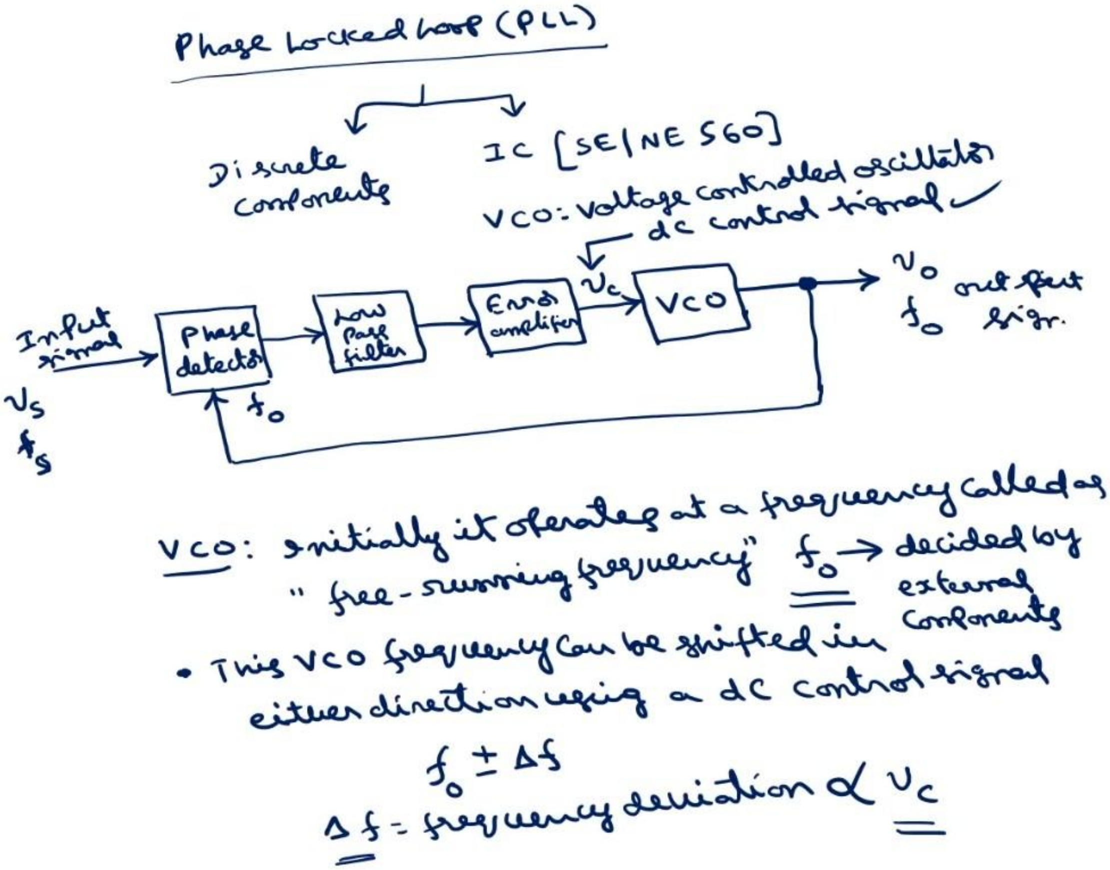
Problem Solving
Lecture – 30
Phase Detectors

Ok. In the previous lectures, we have discussed about a specialized IC called as 555 timer, which generates the precise time delays and is having lot of applications. Today, I will discuss about one more such type of specialized IC called Phase Locked Loop PLL. So, this PLL can be implemented by using discrete components or you can use the IC also. The IC name of this one is SENE 560. First, I will discuss the phase locked loop using discrete components, later I will discuss the IC details. So, if I consider the blocks of this phase locked loop, there will be a phase detector followed by low pass filter and error amplifier.

Followed by VCO, VCO stands for Voltage Controlled Oscillator. From VCO, we will take the output, and a part of this output will be fed back to the phase detector, and there will be another input signal to this phase detector. Say v_s is the input signal, corresponding frequency is f_s, v_o is the output signal, corresponding frequency is f_o. Now, coming to the operation of this phase locked loop, the VCO voltage controlled oscillator.

Initially, this voltage controlled oscillator operates at a frequency called as free running frequency f_o. So, this will be decided by external components such as R and C. So, I will discuss the detailed circuitry of VCO later. So, initially, this VCO operates at f_o. Now, this VCO frequency can be shifted in either direction by applying a DC signal at the input.

This is called DC control signal; we call as v_c. This VCO frequency can be shifted in either direction using a DC control signal that is f_o becomes $f_o + \Delta f$, where Δf is the frequency deviation. And this is proportional to the DC control voltage v_c, that is why the name voltage controlled oscillator. So, this voltage is going to control the frequency of oscillations. So, this is about this VCO.



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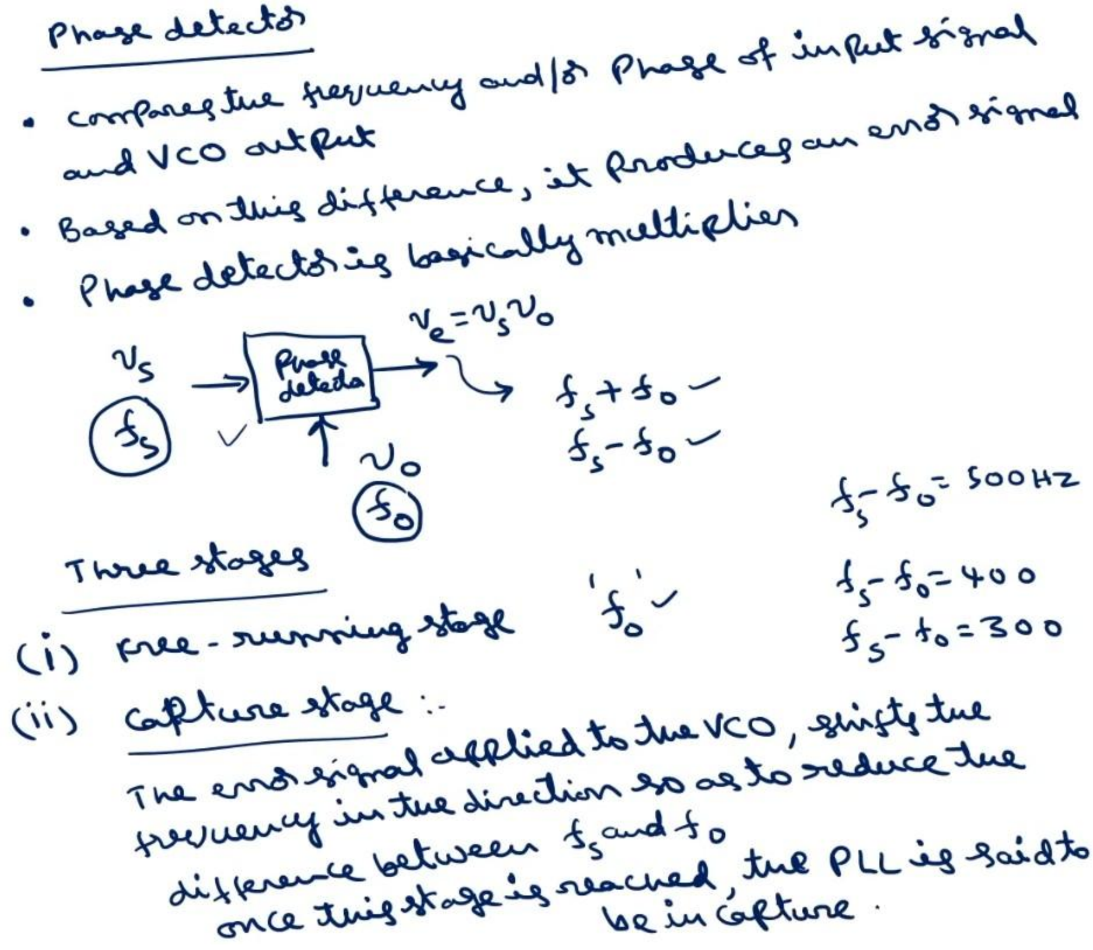
Now, for this phase detector, one input is VCO output, another input is the external input whose frequency is f_s. Now phase detector basically compares the phase and frequency of input and output signal. Now, depends upon the difference it produce a signal called as error signal. And how to implement this phase detector? Phase detector is basically a multiplier it. Is for this phase detector, one input is v_s with the frequency of f_s, the other input is v_o the frequency of f_o output if I call as error signal $v_e = v_s v_o$. We know from the elementary mathematics that if I multiply two sinusoidal signals with the different frequencies, the output will be having sum of the frequency and difference of the frequency.

So, if this frequency is f_s, this is f_o. The output v_e consists of $f_s + f_o$ as well as $f_s - f_o$. I will discuss the mathematical analysis of this phase detector later, but this produces two frequencies. So, between these two, this is high frequency, this is low frequency. So, the output of the phase detector is applied to the low pass filter. So, this filters the high-frequency $f_s + f_o$ and passes the low-frequency $f_s - f_o$.



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Here the frequencies are $f_s + f_o$ and $f_s - f_o$, whereas, here, it will be only $f_s - f_o$. So, this $f_s - f_o$ will be amplified using this error amplifier, which generates a DC control signal which controls the frequency of the VCO. So, as a result of that, what happen this is a closed loop operation. So, this f_o will be shifted in either directions depends upon the DC control signal which in time depends upon the difference of the frequencies. So, here there are three stages of this phase locked loop.

So, one is free running stage as I have told, based on the external components the VCO will oscillate at some frequency of f_o. The second stage is capture stage in this what happens is. So, the difference signal generated by this phase detector is going to change or the shift. So, in capture range, the error signal applied to the VCO shifts the frequency in the direction so as to reduce the difference between f_s and f_o. Initially, with free running frequency, will be having some difference $f_s - f_o$.

Say if this is, say, for example, 500Hz. So, now, the error signal that is going to be generated at the output of error amplifier after filtering the high frequency. So, that will generate a DC control signal to the VCO that DC control signal is going to change the frequency of the VCO such that this difference will be reduced. So, now, this $f_s - f_o$ becomes a 400. Again, this difference signal is going to generate another DC control signal, which again changes the difference to a value which is less than the previous value, say 300.

So, like that the error signal that is going to generate is going to change the frequency of the VCO such that the difference will be reduced. Once this stage is reached, the PLL is said to be in capture range. Starting from the free running frequency, now we are changing the frequency of the VCO in a direction so, that the frequency of the error signal will be decreases. This is what is called capture range. Now, how long this difference will decrease until this $f_o = f_s$?

So, once $f_o = f_s$, this is called lock range. The third stage is lock stage. In lock stage, the output of VCO changes continuously until $f_o = f_s$. That is, the input frequency is equal to VCO output frequency. Once $f_s = f_s$, the PLL is said to be in lock range. After that whatever the variations of this input signal will be tracked by the PLL.

Once the lock is established, the VCO output tracks the changes in the input. So, whatever the changes in the input will be followed by the VCO output. So, this type of tracking is required in many of the applications, especially in communication FSK detector as well as a FM detector and the frequency synthesized transmitters and receivers even in the DC motor control and all. So, this you can call as a tracking range also, after this, will be in tracking mode. This is about the operation of the PLL.

3) Lock stage

- The output of VCO changes continuously until $f_o = f_s$
- At $f_o = f_s$, the PLL is said to be in lock range
- once the lock is established, the VCO output tracks the changes in the input. [Tracking mode]

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Initially, VCO will be at pre-running frequency f_o. Once you apply the input signal, then, the difference between the input and VCO output will be produced at the output of the phase detector, which will act as an error signal. The error signal is going to change the DC input voltage of the VCO such that the difference is going to be reduced. So, once that difference starts reducing that is called capture range and that difference reduces continuously until $f_s = f_o$. Once $f_s = f_o$, the PLL is said to be in lock range.

After that, it will track the VCO output; after that, the VCO output tracks the changes of the input. This is the operation of the PLL. Now, if I take the details of each block phase detector, as I have told, it is basically a multiplier on how to implement this phase detector. Phase detector get me implemented by using either analog circuits or digital circuits. We have analog phase detector digital phase detector. So, if I first consider the analog switch type phase detector, there will be a switch. The on half of the switch will be controlled by VCO output.

This is the output from the VCO, and this is the input signal with a frequency of f_s, and this is error signal V. As I have told basically, the phase detector is a multiplier. So, if you multiply this input signal with the output from the VCO which is in the form of a square wave. So, whenever the VCO output is high during this state, the input will be transferred as it is when the VCO output is low output will be 0. Now, we will draw the input output waveforms for different phases.

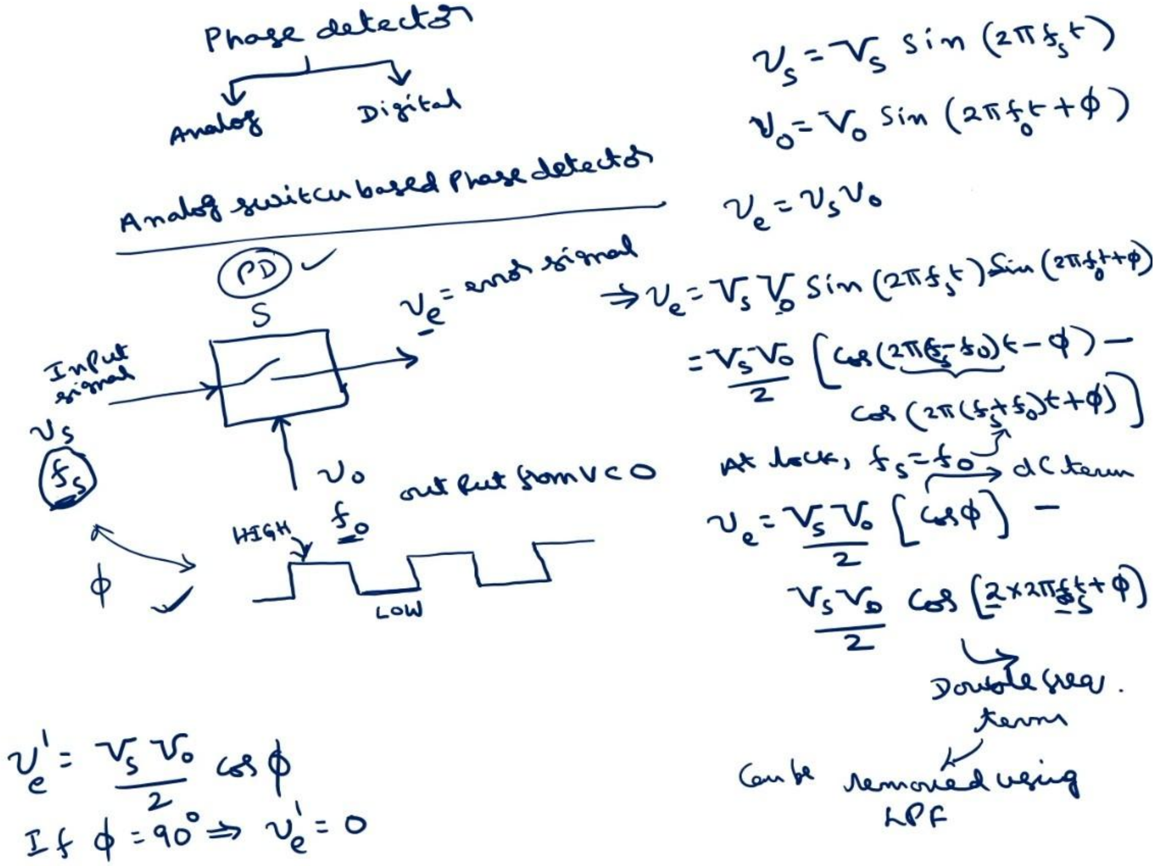
As I have told this phase detector is going to compare the frequency as well as the phase also. So, let us consider $v_s = V_s \sin(2\pi f_s t)$ and $v_o = V_o \sin(2\pi f_o t + \emptyset)$. As I have told this phase detector is going to compare the frequencies as well as the phase. So, the only difference between these two is $\emptyset$. So, what will be output of this phase detector? Basically, multiplication of $v_s v_o$.

So, if you multiply this $v_s v_o$, we will get $V_s V_o \sin(2\pi f_s t)\sin(2\pi f_o t + \emptyset)$. This is sin A sin B form. So, 2 sin A sin B can be written as cos A minus B is cos A cos B plus sin A sin B. If I take minus of cos A minus B, this will be written in the form of $\frac{V_s V_o}{2}[\cos(2\pi(f_s - f_o)t - \emptyset) - \cos(2\pi(f_s + f_o)t + \emptyset)$.

So, at lock $f_s = f_o$. So, what happens to $\frac{V_s V_o}{2}$ and this will become 0. So, only $\cos(-\emptyset) = \cos(\emptyset)$, is one term minus second term, is $\frac{V_s V_o}{2}\cos(2 \times 2\pi(f_s + f_o)t + \emptyset)$. So, this becomes now $2f_s$ or $2f_o$. This is $\frac{V_s V_o}{2}\cos(2 \times 2\pi f_s)t + \emptyset)$.

There are two terms: one is this is DC term and this is double frequency term. If input frequency is f_s, this term will be having $2f_s$. So, this $2f_s$ term can be removed using low pass filter. You take the low pass filter whose cutoff frequency is less than twice the input frequency f_s, then this will be eliminated. Then, after the low pass filter, if I call as v_e' signal, this will be $\frac{V_s V_o}{2} cos\emptyset$.

So, you can see that here this error signal will be 0 if $\emptyset = 90^o$. So, we can explain the same using the waveforms also. Suppose this is the VCO output v_o; I will consider here as a square wave. Those square wave will be having lot of sinusoidal signals using Fourier series representation.



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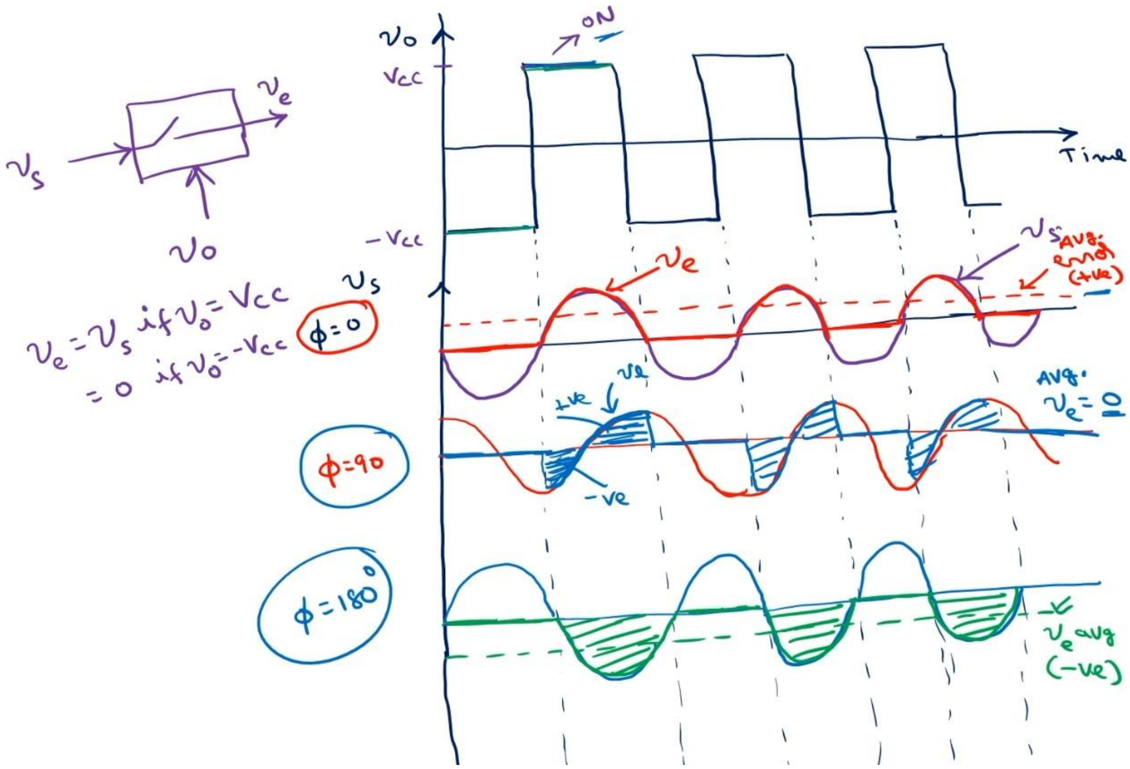
This is a function of time. Now, v_s I will represent for three different phases one is I will take $\emptyset = 0$. So, what type of v_s we will get? This is negative peak, and this is positive peak, this is negative peak, positive peak and so on. So, what will be the output? This is your v_s. What is v_e? The error signal the output of the phase detector will be whenever V 0 is 1, here this will be switch will be on. There is a switch which will be controlled by v_o and here we have v_s .

So, this output $v_e = v_s$ if $v_o = 1$. If I call this as V_{CC}, which is 5 volts, V_{CC} and $v = 0$ if $v_o = -V_{cc}$. So, during this portion, the output is 0. If I call this output of low pass filter using the red signal, this will be 0, and during this portion, whatever the input will be transferred to the output and here 0, and this output here 0, here output here 0, and so on. So, this is red signal is called v_e, that is error signal and if we take the average using the low pass filter, we will get somewhere here the average error, which is positive.



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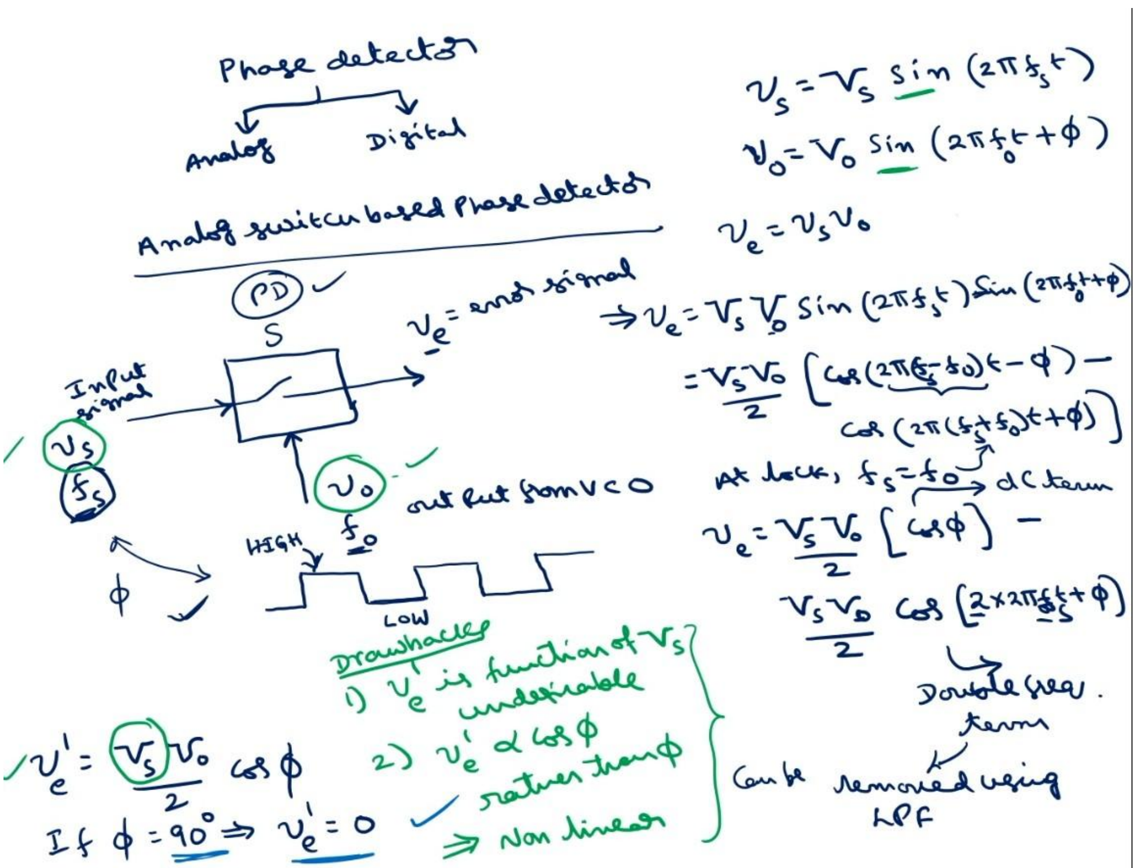
This is average value of error. This is the case of $\emptyset = 0$, and second case is $\emptyset = 90^o$. So, in that case, what happens? The waveform will be something like this. Now, we can see that. So, during this negative portion, anyhow, 0. So, output of this phase detector will be.

So, during this negative portion 0, during the positive portion as it is, it will goes as this portion as it is will be the output v_e and here again negative portion this comes to 0, positive portion as it is and here again 0 here as it is like this. So, if I take this during the positive portion here, this is as it is this will come if I take the average value. So, this value and this value get cancelled this and this is positive this is negative these two will get cancelled. Similarly, here this is negative this is positive get get cancelled. Similarly, here negative and positive will get cancelled as a result of that error signal will be 0V average value is here this was positive now this is 0.

So, which we have already proved from the mathematics also. If $\emptyset = 90^o$ error signal is 0 this is because. So, when $v_o = 1$, which is high. So, a portion of this output signal will be positive another portion is negative with opposite polarity. So, two amplitudes with opposite polarity, the result it is 0 this is the case of $\emptyset$ in 90.

If I take $\emptyset = 180^o$, you will get error as negative. You can see that this is $\emptyset = 180^o$ this is negative this is positive and this is positive this is negative. Now, we can see that during the negative portion as it is this will be output of the error detector. So, this will be output of the phase detector. So, during this negative portion, output will be 0. During the positive portion of v_o output will be input. This will be the output as it is this will be the output and here it is 0 again this output.

So, like that, you will get only negative portions, and if you take the average, you will get somewhere here. This is average v_e, which is negative. So, like that, this phase detector output varies with the so, this is the phase detector output for different values of the phase. Now, the drawback of this type of the phase detector is you can see that here, this v_e' the error signal is a function of the input voltage which is undesirable means this v_e' which is a part of the closed loop gain of the given PLL depends upon the input amplitude. If the input fluctuates, then the error signal, thereby the overall gain of the loop, will be fluctuate. This is undesirable. This is one drawback. Second drawback is this is non-linear in the sense v_e' is proportional to $cos\emptyset$ rather than $\emptyset$.



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So, implies non-linear. So, in order to avoid this drawback. so, we will consider this v_o as a square view instead of sine view and v_s also we can consider as a square view if both if you consider as a square view, then we can avoid this drawbacks. So, if these two are square waves, then we can use a digital circuit to realize the phase detector. So, we will discuss that digital phase detector in the next lecture. Thank you.