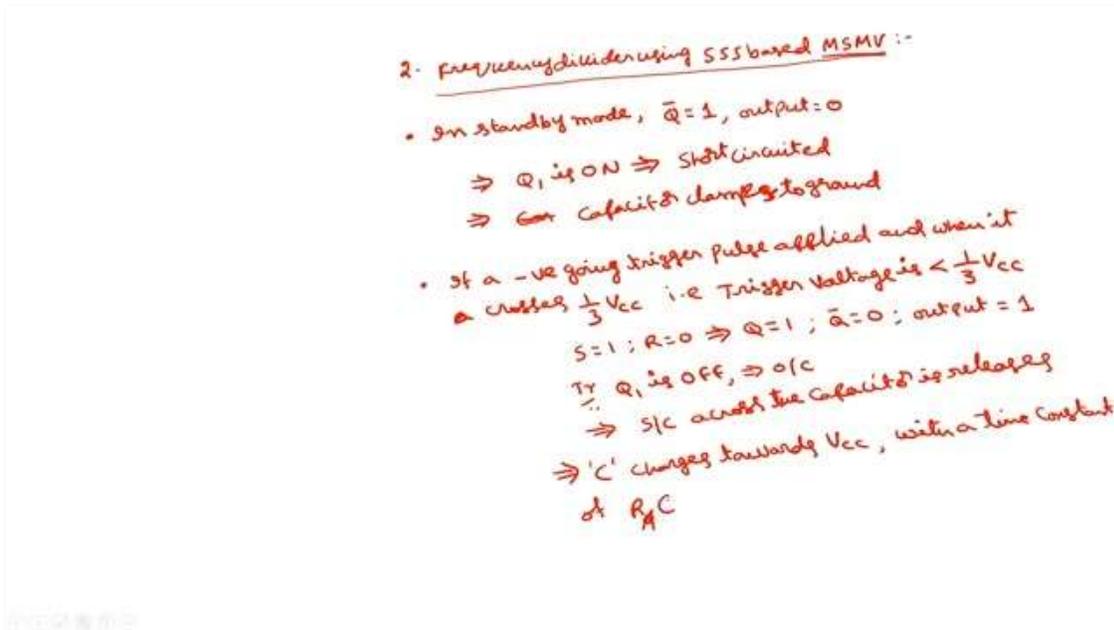


Integrated Circuits and Applications
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555 Timer
Lecture - 28
Monostable applications II

Okay! In the last lecture we have discussed about the pulse width modulation using 555 timer based on monostable multivibrator. So, the next application is we can use this monostable multivibrator to perform the frequency division. Frequency divider using 555 timer based monostable multivibrator, this is monostable multivibrator. So, we know that the monostable multivibrator in standby mode, output \bar{Q} will be high as a result of that output of this 555 timer will be low because there is inverter between the \bar{Q} and Q . And this \bar{Q} is connected to the transistor which is connected across the capacitor. So, implies the transistor Q_1 is ON thereby short circuited, if I consider ideal case implies capacitor clamps to ground.

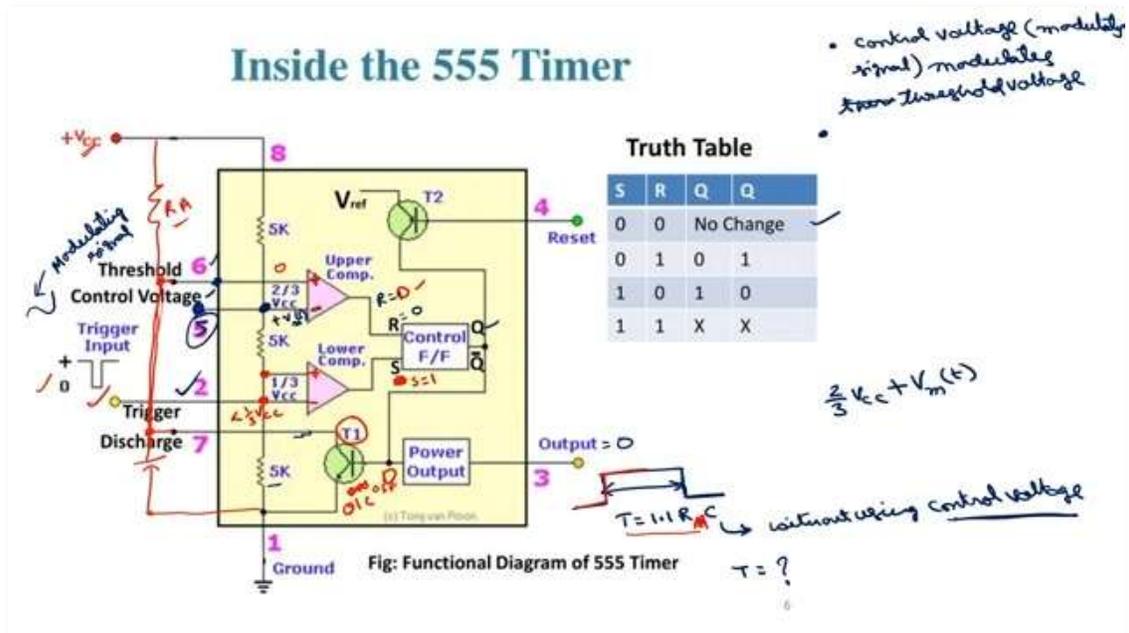
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This is clear from that the diagram that we have considered even if we take this diagram also here in fact, this trigger pulse is applied and capacitor is connected across here between 6 and 1. Here in fact, this capacitor is connected and there is a resistor here R_A in monostable multivibrator. So, if this transistor Q_1 is ON in a standby mode because this \bar{Q} is equal to 1 this will be on this will act as short circuit. So, this capacitor will be short circuited this will be connected here, the capacitor will short circuit.

As a result of that what will be the voltage at 6 point because this is connected to the capacitor. So, here also this is 0 volts. So, the voltage at non-inverting terminal is 0 inverting terminal is $\frac{2}{3}V_{CC}$. So, output will be 0. Now if I apply the negative going trigger pulse, if a negative going trigger pulse is applied and when it crosses $\frac{1}{3}V_{CC}$ that is trigger voltage is less than $\frac{1}{3}V_{CC}$.

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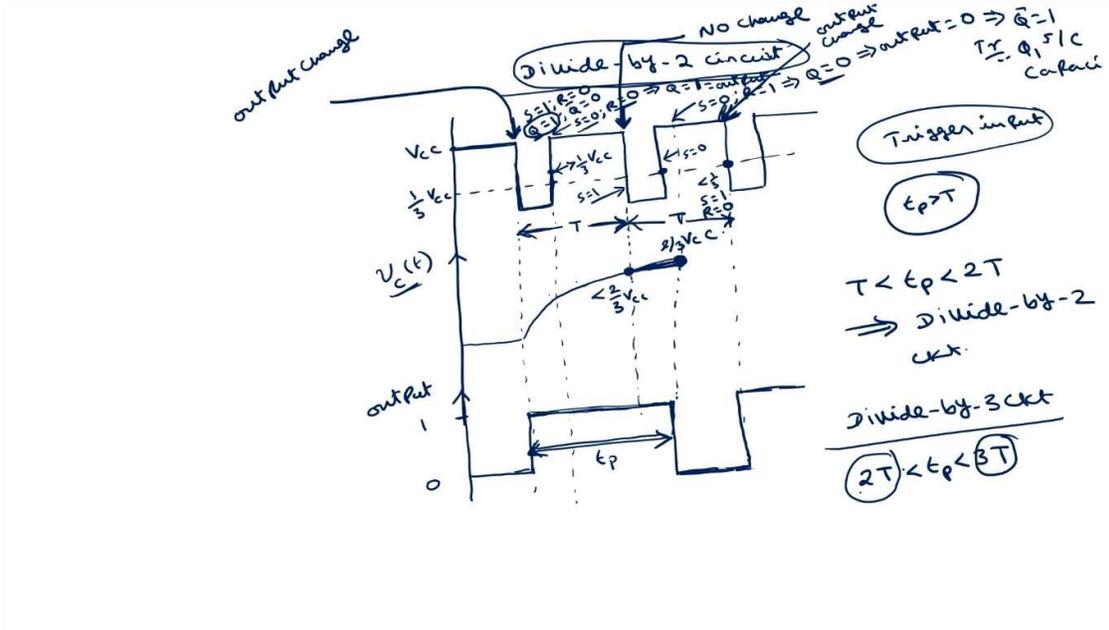
So, what happens here this trigger voltage slightly less than $\frac{1}{3}V_{CC}$ this is $\frac{1}{3}V_{CC}$. So, the voltage at non-inverting terminal is more than the voltage at inverting terminal. So, that S becomes 1 and R was 0. So, what happens to this output of the flip flop? implies Q is equal to 1 and \bar{Q} is equal to 0. So, the transistor Q_1 is OFF and what happens to the output? is equal to Q itself.

So, this is equal to 1. So, this transistor Q_1 is OFF implies open circuited implies the capacitor the short circuit across the capacitor releases, implies capacitor charges towards V_{CC} with a time constant of $R_A C$. So, this \bar{Q} becomes 0. So, this will be instead of ON now will be OFF instead of short circuit, open circuit. So, across this capacitor open circuit means this short circuit was released now the capacitor charges through this R_A towards V_{CC} . And what happens to output? output goes to the high and how long it will stay in high state? is given by T is equal to 1.1 times this $R_A C$.

Now in order to make this monostable multivibrator to divide the frequency by 2. So, what happens to these waveforms? Divide by 2 circuit. This for the trigger signal, a series of triggers are applied here. This is trigger input somewhere here $\frac{1}{3}V_{CC}$ will be there this is V_{CC} this is $\frac{1}{3}V_{CC}$. Initially, when trigger is not applied, trigger is high what will be this capacitor voltage if assume that $v_C(t)$ is the voltage across the capacitor. In standby mode, capacitor will be short circuited as we have discussed. First, I will draw the output after that I will draw this $v_C(t)$. Output will be initially in standby mode 0 whenever the negative pulse going pulse is applied whose

amplitude is less than $\frac{1}{3}V_{CC}$ this will go to high. And how long this will be high this will be decided by the R_A and C values.

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If I choose this R_A and C values such that if this is high for a time period greater than time period of the trigger signal. This is one time period. So, I am going to choose this pulse width slightly greater than T suppose if this is this one. Whenever the output goes to high so \bar{Q} is 0. So, short circuit will be released capacitor will charges towards V_{CC} this is the point where the capacitor starts charging.

Now, it will charges to $\frac{2}{3}V_{CC}$ then this output will changes from high state to low state logic 1 logic 0. So, this is the point where it will changes from high to low state. So, for the transition from 1 to 0 the condition is in order to change from this high to low the condition here will be the voltage at 6th terminal that is the voltage across this capacitor has to be slightly more than $\frac{2}{3}V_{CC}$ otherwise the output stays in high state only. So, output will stay in high state only. So, if I choose this high state even if you apply the second negative trigger here, if this capacitor does not charges to $\frac{2}{3}V_{CC}$ here the voltage is a value which is less than $\frac{2}{3}V_{CC}$ and here only it will charges to $\frac{2}{3}V_{CC}$.

Now, here what happens to output? Now, because you have applied the second negative going pulse here this is the first negative going pulse this is the second negative going pulse. Now, we are assuming that this pulse width $t_p > T$. So, we know that even if a second negative going pulse is applied until this output is high it will not recognize that second negative going pulse. The reason for that one is really if I start from here negative going pulse here really this S is equal to 1, R is equal to 0 that is we are getting Q is equal to 1, \bar{Q} is equal to 0. So, Q is equal to 1 means output is also 1 output is nothing, but Q .

So, you are getting output as 1. So, during this portion S remains 1 because if it is slightly less than $\frac{1}{3}V_{CC}$. So, output goes to S will becomes 1. Now, if this trigger input if it exceeds slightly more than $\frac{1}{3}V_{CC}$ here at this point where the voltage is slightly greater than $\frac{1}{3}V_{CC}$. What happens to this output of the lower comparator? Now, here in the positive going portion this portion whenever it crosses $\frac{1}{3}V_{CC}$ here if the voltage is greater than $\frac{1}{3}V_{CC}$ this is $\frac{1}{3}V_{CC}$.

So, negative voltage is greater than this one. So, S becomes 0, R is still 0 only because this capacitor has not charged up to the $\frac{2}{3}V_{CC}$. So, if the voltage here is less than $\frac{2}{3}V_{CC}$ R becomes 0 only, R becomes 1 only if this voltage is greater than this $\frac{2}{3}V_{CC}$. Now, here what happens is so, at this point actually from here onwards S becomes 0, R was already 0. Now, what happens to the Q ? At this point S is equal to 1, R is equal to 0, Q is equal to 1.

Now, here S becomes 0, R is 0 only. So, what happens to Q ? So, we know that from the truth table this if for S is equal to 0, R is equal to 0 output will not change output remains in the previous state only. So, as a result of that even though you have applied S is equal to 0, R is equal to 0 the previous state of Q is equal to 1 will be retained that is why still at this point also this output becomes 1 only because Q is equal to output itself. So, in order to change this output to lower level state you have to make this R is equal to 1, R is equal to 1 means this capacitor has to charge to $\frac{2}{3}V_{CC}$. So, if I assume that this is the point where the capacitor charges to $\frac{2}{3}V_{CC}$.

So, this is the point where if this is slightly here. So, at this point what will be S and R ? Here this becomes S is equal to 0, again here S is equal to 1, again here of above this S is equal to 0. So, this is equal to S is equal to 0, but R is equal to 1 here because whenever the capacitor charges to a value which is slightly more than $\frac{2}{3}V_{CC}$ this $\frac{2}{3}V_{CC}$. So, positive voltage is greater than negative voltage.

So, R becomes 1. Now, what happens here the output goes to low S is equal to 0, R is equal to 1 implies Q is equal to 0 implies output is also 0. You can see from the truth table also S is equal to 1, R is equal to 0 output becomes 1, S is equal to 0, R is equal to 1, S becomes Q becomes 0. So, this Q becomes 0. Now, what happens is after that the another negative going pulse the third negative going pulse. So, at this point again it will retrigger.

Here also if a voltage is just slightly less than $\frac{1}{3}V_{CC}$. So, at this point what happens R was already 1. So, S also becomes S is equal to 1 and because this output has become \overline{Q} output Q is equal to 0 implies \overline{Q} equal to 1 implies transistor Q_1 is short circuited and capacitor bypasses and capacitor voltage becomes 0. So, as a result of that so, at this point what happens is this R becomes 0. So, because S is equal to 1, R is equal to 0 again the output will be 1.

So, again it will goes to the high like that this will continue. So, one point that you have to remember here is at this point output will change. So, at the second trigger no change why because. So, at the second negative going pulse this capacitor has not yet charged up to the $\frac{2}{3}V_{CC}$ that is why even if you apply the second trigger the output will not change. But at the third negative trigger again the output will change why because now the capacitor already charged to $\frac{2}{3}V_{CC}$.

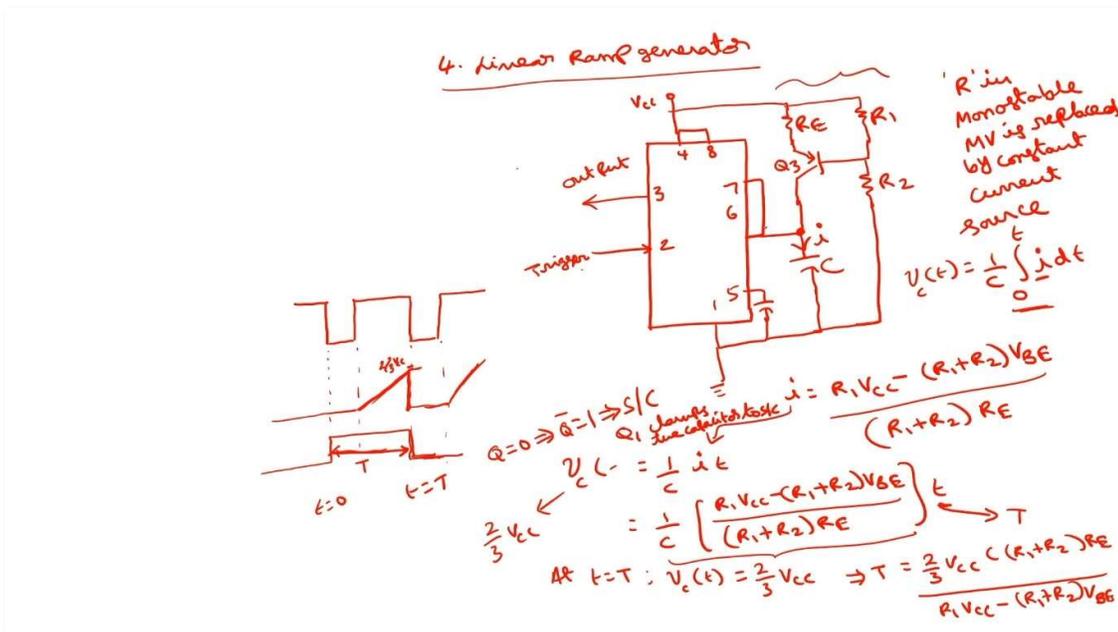
7, 6 here both will be short circuited and this will be connected to the resistor. When the resistor is connected. This is where trigger is applied. At 3 output is taken.

How does this acts as a missing pulse detector? If I consider these are the pulses at trigger input. A negative going trigger signal here will short circuit this transistor thereby the capacitor will charges towards V_{CC} with a time constant of RC . And whenever this negative going trigger crosses $\frac{1}{3}V_{CC}$ as we know output goes to high. These are the places where this negative going trigger is applied. If the capacitor charges here slowly charges here the capacitor will charges. So, before this second negative going clock pulse is applied if it charges to a voltage which is less than $\frac{2}{3}V_{CC}$. And what happens the output was high. So, here it has not charged up to $\frac{2}{3}V_{CC}$ output will remain high only.

So, during this second negative going this one. So, the capacitor will be short circuited will goes to 0 again it will start charging here again after second clock pulse also it has not reached up to $\frac{2}{3}V_{CC}$ this is value less than $\frac{2}{3}V_{CC}$ output remains high only. So, third pulse also if it does not reaches then output is high only will still becomes high only. So, this is the case if all the pulses are detected this is with all the pulses detected. Now what I am going to do is if I miss this pulse if I make this as high only then what happens here this capacitor will get enough time here the capacitor has not got enough time to reach up to $\frac{2}{3}V_{CC}$ because this duration is this T time period is greater than the t_p .

Now here because this pulse has been missed now the capacitor has a time to charge up to the $\frac{2}{3}V_{CC}$. As a result of that this output instead of becoming high if it charges to $\frac{2}{3}V_{CC}$ somewhere here then the output becomes low. Again, at the negative going pulse of this fifth pulse again it will goes to high this is how this will detect the missing pulse.

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And the fourth application is linear ramp generator. This is same as the monostable multivibrator circuit where the capacitor will be replaced by a constant current source. If you consider the circuit diagram of this one this is same a monostable multivibrator circuit. Now, let us consider the circuit diagram of this circuit. This is transistor Q_3 . So, this circuitry will generate constant current to this capacitor C . Previously there was a resistor now we are replacing the R with a constant current source.

R in monostable multivibrator is replaced by constant current source. Now, what will be the voltage across this capacitor? $v_c(t) = \frac{1}{C} \int_0^t i dt$. So, the expression for this i can be obtained here using the transistor analysis as $\frac{R_1 V_{CC} - (R_1 + R_2) V_{BE}}{(R_1 + R_2) R_E}$. Now, what will be $v_c(t)$? $\frac{1}{C}$ the integral of $i dt$ is i will come outside dt 0 to t becomes t only. If I substitute this i here is equal to $\frac{1}{C} \left[\frac{R_1 V_{CC} - (R_1 + R_2) V_{BE}}{(R_1 + R_2) R_E} \right] t$.

So, if I plot the input output waveforms this is the negative going trigger and what will be the capacitance voltage? Here it will be start charging linearly because this current is linear. This slope of this one will be this, this is equal to $y = mx$ type of thing. This is the linear charging and at t is equal to t whenever it charges to $\frac{2}{3} V_{CC}$ the output becomes low and see the output signal. If I start this as t is equal to 0 t is equal to T this duration is say T . So at t is equal to T $v_c(t)$ is equal to $t \frac{2}{3} V_{CC}$.

If I substitute here $\frac{2}{3} V_{CC}$ this is $\frac{2}{3} V_{CC}$ this with T . So, you will get the expression for the T as $\frac{\frac{2}{3} V_{CC} C (R_1 + R_2) R_E}{R_1 V_{CC} - (R_1 + R_2) V_{BE}}$. This is the time period of this ramp signal. Again, when this comes to 0 this will becomes 0 immediately because once the output becomes 0 output is nothing, but Q implies \bar{Q} is equal to 1 which will short circuit transistor Q_1 which we have discussed in the monostable multivibrator which will clamp the capacitor clamps the capacitor to short circuit.

This is it output is 0. Again, it will charge here. So, like that you will get linear ramp at the output of this 555 timer. So, these are some applications we will discuss about the other stable multivibrator in the next lecture. Thank you.