Integrated Circuits and Applications
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555 Timer
Lecture - 26
Monostable operation

So, in the last lectures we have discussed various applications of the operational amplifier such as amplifiers, integrator, differentiator, rectifiers, oscillators, filters etcetera. So, today we will discuss about one of the specialized IC called as a 555 timer. 555 timer is a specialized IC which basically will be used to generate the exact time delays. This is highly stabilized IC used to generate exact time delays. We can generate the time delays using the other circuits such as operational amplifier and all, but in order to generate precise time delays, exact or precise time delays we will use the 555 timer. In many of the industrial applications it is required to generate the precise time delays.

Even a $1\mu s$ also will causes lot of changes in the operation of the industrial processes. So, in such applications we will use 555 timer. So, I will give some special features of this 555 timer. So, this 555 timer was introduced in 1970s using a company called Signetics.

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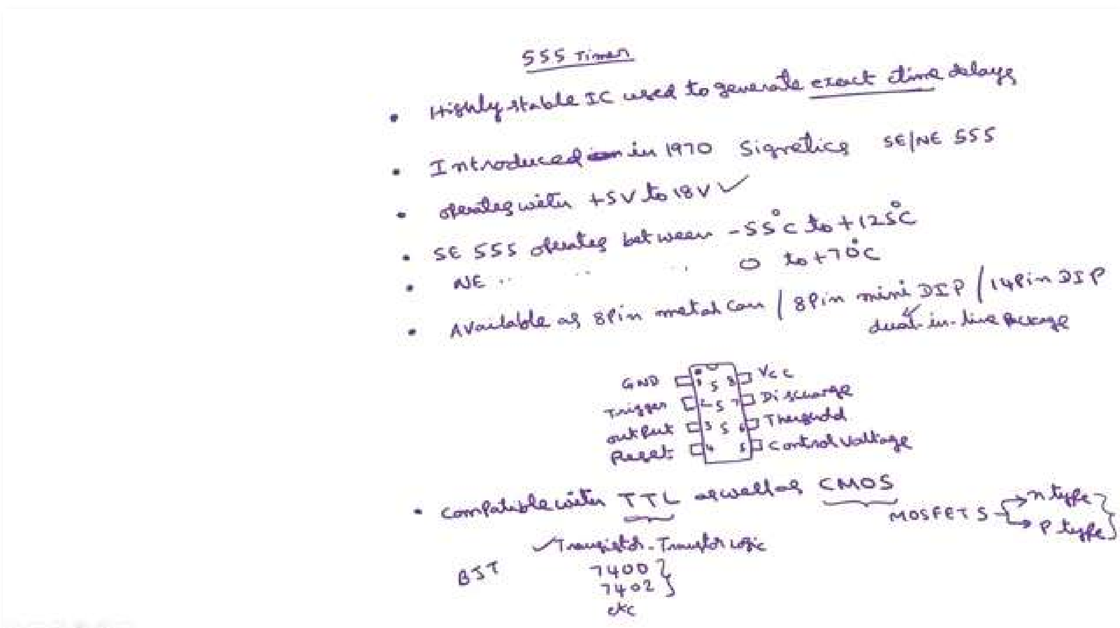

This operates with a power supply of 5 volts to 18 volts and this is available as two different ICs SE slash NE555. So, SE555 operates with temperatures $-55°C$ to $125°C$ whereas, NE555 0 to $70°C$. And this is available as 8 pin metal can in round shape or 8 pin mini DIP. DIP stands for dual in-line package means half of the pins will be on one side, half of the pins will be on the other side.

There is a dot here from here it starts this is pin number 1, pin number 2, pin number 3, 4, 5, 6, 7, 8. This is the ordering of the pins. So, the function of this pin number 1 is this will acts as a ground and this pin number of 8 is V_{CC} which varies from plus 5 volts to 18 volts. And here this will acts as a trigger. I will explain the function of each pin after considering the internal circuit diagram of 555 timer. This will acts as a reset, output, control voltage, threshold, discharge.

I will explain the function of this one even this is available as 14 pin DIP also. Then this is compatible with both TTL logic family as well as CMOS logic family. You might have studied about this TTL and CMOS in your digital circuits course. So, TTL stands for transistor transistor logic. So, basically all the logic functions such as AND gate, OR gate, NOT gate these gates can be implemented by using a TTL logic, but the basic logic circuit is universal gate NAND or NOR.

So, using this NAND or NOR you can implement this AND gate, OR gate and all. So, you might have used this 7400, 7408, etcetera ICs in your digital lab they are belongs to TTL logic family. On the other hand, there is another family called CMOS logic family. This uses MOSFETs. TTL uses the bipolar junction transistors whereas CMOS uses MOSFETs.

MOSFETs are again N type and P type. So, this CMOS uses both N type as well as P type and there are some advantages of the CMOS over the TTL. So, we are going to discuss some of the CMOS circuits in the coming lectures okay. So, this 555 timer IC is compatible with both CMOS logic as well as TTL logic. These are some important features of the 555 timer. If you consider the internal diagram this will be like this. This is reverse, 4 is reset, 3 is output.

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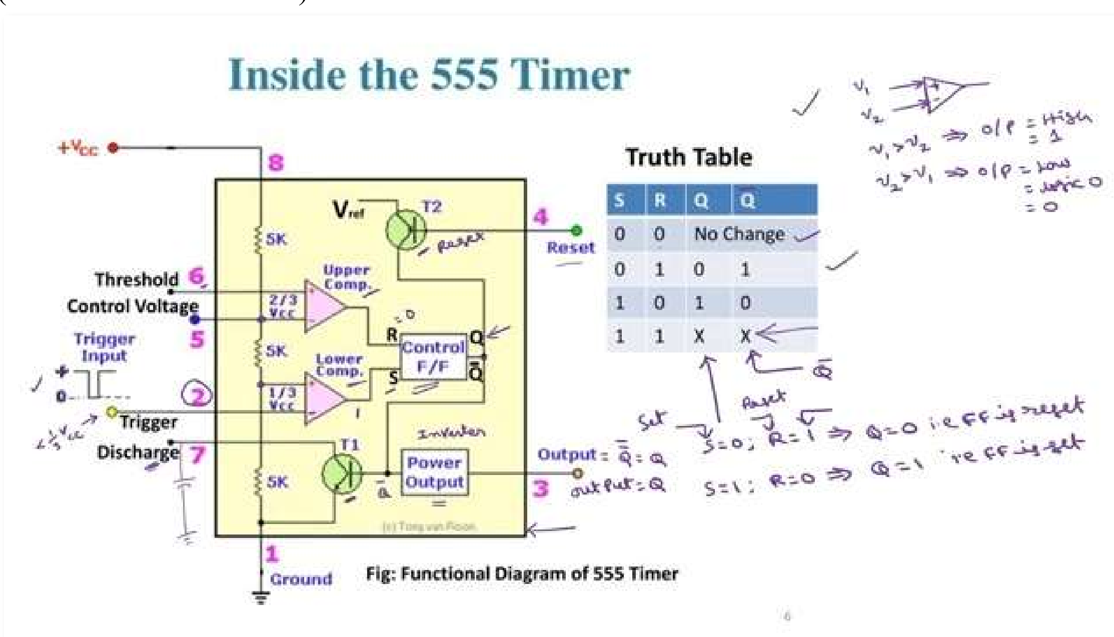

So, we can see that here basically there are two comparators one flip flop. So, this is the upper comparator, this is the lower comparator. So, we know that this comparator acts in open loop configuration. There are two voltages say v_1 is applied to the positive terminal, v_2 is applied to the negative terminal.

If v_1 is slightly greater than v_2, then output will be logic 1, high or you can call as logic 1. In digital we have 0 and 1s. If v_2 is slightly greater than v_1, then output will be low. It is logic 0 and SR flip flop is having this truth table.

We know that if S is equal to 0, R is equal to 0, no change in the output. If S is equal to 0, R is equal to 1, output Q will be 0. $\overline{Q}$ will be of course, the complement of Q. So, this row is $\overline{Q}$ row. So, we will consider only this Q. So, the flip flop is said to be reset if reset input is equal to 1. S is equal to 0, R is equal to 1. This is reset input is 1. R stands for reset, S stands for set implies output Q is equal to 0 that is flip flop is said to be reset. On the other hand, if set input is equal to 1 and R is equal to 0 implies Q is equal to 1 that is flip flop is set. That is why the name set reset flip flop.

If both are 1s, this is not allowed actually. There is a problem with 1 1 in SR, but in this application that condition will not arise. So, we have used the RS flip flop. And there is a power output. This is a power amplifier circuit. This will acts as a inverter basically.

So, for this inverter the input is $\overline{Q}$. So, what will be output of this inverter? This is $\overline{Q}$ passed through the inverter $\overline{\overline{Q}}$ which is equal to Q itself. That means, the output of the IC this 555 timer is same as the output of the flip flop. So, this output is equal to Q which is the output of the SR flip flop, but here there is no connection for this Q only $\overline{Q}$ is connected, but the output that you are going to get here which is equivalent to output of the flip flop Q. And there is a transistor here to reset this 555 timer and there is a discharge transistor here okay.

Now, coming for the operation of this 555 timer, we have two comparators. Upper comparator will be having a threshold voltage of $\frac{2}{3}V_{CC}$ and lower comparator will be having $\frac{1}{3}V_{CC}$. This is 0 volts. We are going to apply a negative going trigger pulse at the pin 2 which is the input applied to the inverting terminal of the op-amp. So, this is some positive voltage, this is 0 volts.

So, whenever it reaches to a value which is slightly less than $\frac{1}{3}$ of the V_{CC}, $\frac{1}{3}$ of the V_{CC} is the voltage applied for the positive terminal. If the negative voltage here is less than $\frac{1}{3}$ of the V_{CC}, what happens? According to this the positive voltage is greater than negative voltage. So, output becomes logic 1 which is S. And at that time we will make this R is equal to 0 as a result of that the flip flop will be set because set input is equal to 1. And this complete operation will be understand if I connect the external components also.

Here this IC pins are left floating okay. There are two modes of the operations in which we are going to connect some components to these pins. So, that time I can completely understand the operation of this 555 timer. Now, I am just I mean explaining the functions of the each pin. So, this discharge pin will be used along with the capacitor.

Here we are going to connect a capacitor to charge or discharge this we can use this discharge pin. And there is a threshold voltage here we are going to apply this threshold voltage through this RC network. So, if this voltage is greater than $\frac{2}{3}V_{CC}$ positive voltage greater means R becomes 1. So, the flip flop will be reset. Then coming for this control voltage. So, this $\frac{1}{3}V_{CC}$ and $\frac{2}{3}V_{CC}$ is going to control the time duration of the pulse that is going to be generated.

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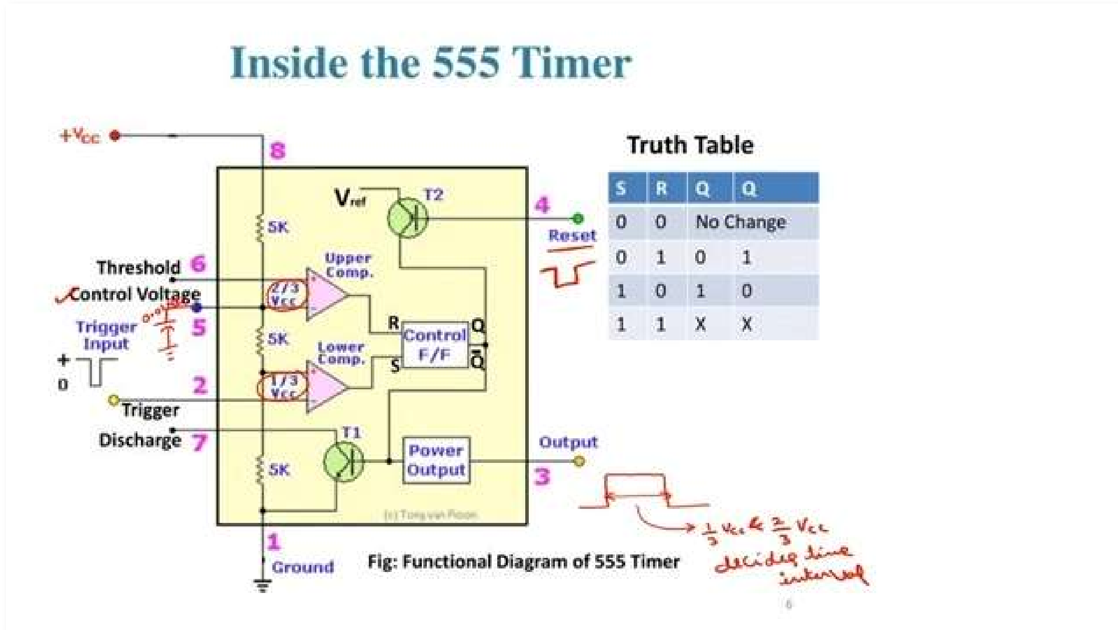

Here at the output we will get a pulse. So, the exact time delays will be generated this output which will be initially low, then will be having high, then it will becomes low. This exact time delay will be decided by this $\frac{1}{3}V_{CC}$ and $\frac{2}{3}V_{CC}$ of this upper and lower comparators. This is going to be decided by the threshold voltages and trigger voltage of lower and upper comparators.

This also can be controlled by using an extra signal called as control voltage. If you do not want to use this control voltage, then the manufacturer recommended that this has to be grounded through the capacitor with $0.01\mu F$. So, in that case this $\frac{2}{3}V_{CC}$ $\frac{1}{3}V_{CC}$ is going to decide this. And then the reset, so at any time if you want to make the output is equal to 0, we can apply a negative going pulse at the reset, so that the output can be forced to 0. So, these are the different applications, different functions of the pins and these functions will be very much clear if I consider the external circuitry also okay.

So, if I consider the application of this 555 timer is monostable multivibrator. This is a circuit diagram of monostable multivibrator. We can operate this 555 timer in two modes, one is monostable multivibrator, another is stable multivibrator. So, in monostable multivibrator, so these are the external things that we have connected. There is a resistor, there is a capacitor and here we are going to take the output. Now coming for the operation of this 555 timer in monostable multivibrator mode. Initially in standby or stable operation output of this flip flop $\overline{Q}$, here the details are not given. So, in the previous diagram it was given this is R and this is S, this is $\overline{Q}$.

So, $\overline{Q}$ will be high. You can make this $\overline{Q}$ is equal to high by using some preset and the clear signals of the flip-flop. So, initially in standby mode $\overline{Q}$ is high. So, what happens to this output? Because this is inverter basically, if this is high this will be low implies output is same as Q because $\overline{\overline{Q}}$ which is equal to Q this will be low. So, this at this output will have the low state, this is low. Now what happens is we have to apply a negative going trigger signal here of short duration at pin 2.

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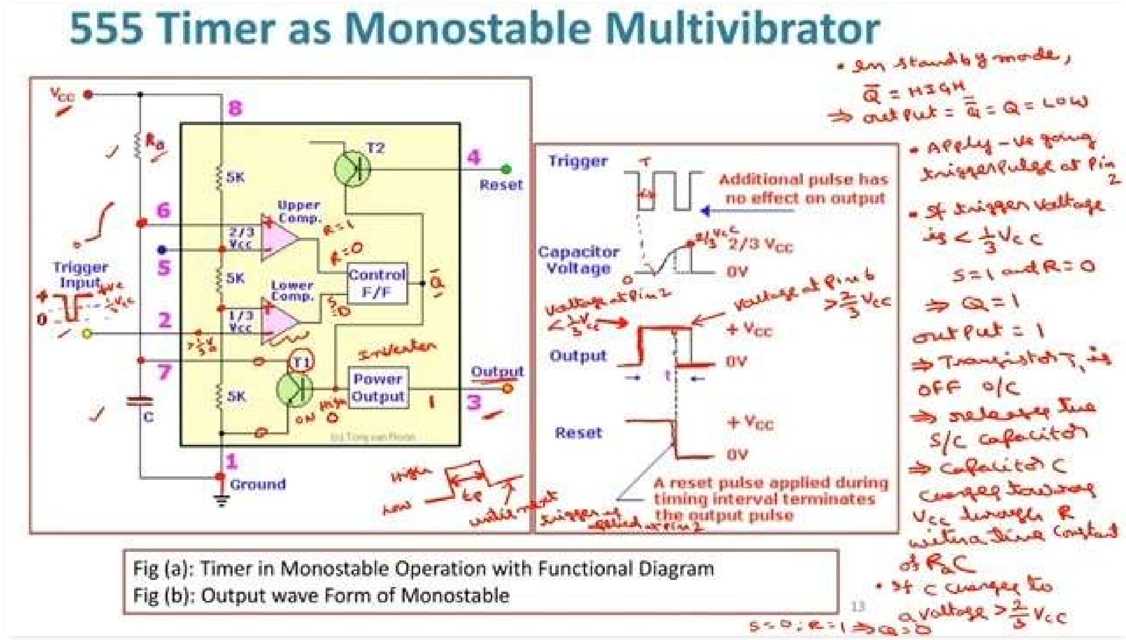

Now, it will start with some positive voltage, then it will go this is 0, this is 0, this is some positive voltage. Now, whenever it comes to a value which is slightly less than $\frac{1}{3}$ of the V_{CC}, if trigger voltage is less than $\frac{1}{3}$ of the V_{CC}. What happens to this comparator? The voltage at non-inverting terminal is $\frac{1}{3}V_{CC}$ and voltage at inverting terminal will be a value which is slightly less than $\frac{1}{3}V_{CC}$. So, what happens S becomes 1 and at that time R will be 0 because. So, in the standby mode or steady state this output is low, this output is high.

So, this high value of this $\overline{Q}$ will turn on this transistor Q_1. So, once the transistor is on this will act as short circuit and this capacitor will be clamped to the ground. So, this will becomes now ground potential. So, this is also ground potential. So, the voltage at non-inverting terminal of upper comparator is 0 whereas, at inverting is $\frac{2}{3}V_{CC}$. So, the voltage at negative terminal is greater than voltage positive terminal. So, this makes R is equal to 0. So, this takes some S is equal to 1 and R is equal to 0. So, you can see from the truth table that the output Q becomes because set input is 1, flip flop is set. So, Q is equal to 1 means output will be Q itself, this output is Q itself as I have discussed earlier 1.

So, this will go to the high state. Now, how long this will stay in the high state? That will be decided by now the value at the 6 pin number 6. So, once the output is equal to 1, what happens to this transistor T_1? So, this is output is equal to logic 1 means this is logic 0. So, T_1 will be off and it will acts as open circuit thereby it releases short circuited capacitor. Now, this will acts as a open circuit. Now, the capacitor C charges towards V_{CC} through R with a time constant of RC. So, this is the resistor R_a it will charges towards V_{CC} with a time constant of R_aC. Now, this voltage is going to rise this is the voltage across the capacitor with respect to the ground between 6 and ground we have the capacitor. So, initially this was 0 in the standby mode, once if you apply a trigger pulse whose amplitude is slightly less than $\frac{1}{3}V_{CC}$. So, this transistor T_1 will be switch off as a result of that the capacitor charges. So, here the voltage is going to be this is voltage across the capacitor that charges from 0 to towards V_{CC}.

So, whenever this voltage reaches a value which is slightly more than $\frac{2}{3}V_{CC}$ slightly more than $\frac{2}{3}V_{CC}$ what happens? So, this voltage which is voltage at non-inverting terminal of op-amp is slightly more than that of inverting terminal. So, what happens R becomes 1 and what will be S? S was 1 if I apply this negative going trigger, but this is of short duration after that this becomes some large positive value because this value is $\frac{1}{3}V_{CC}$ this is a value which is greater than $\frac{1}{3}V_{CC}$. So, at that time what happens to this voltage here? This is more than $\frac{1}{3}V_{CC}$. So, negative voltage is greater than positive voltage.

So, output will becomes 0. So, what happens now? S is equal to 0, R is equal to 1 implies Q is equal to 0. So, this output becomes again 0. Now, this will remain in 0 until the next trigger is applied this is 0 until next trigger is applied let pin number 2 and the same operation will repeats. As a result of that here this is going to be decided by this R_a and C we are going to derive the relation for this pulse duration if I call this as t_P we are going to derive this t_P expression in terms of this T if this is T duration this negative going trigger is having T duration okay. So, the same operation is explained with the help of the waveforms here.

So, whenever this reaches to a value two-third this capacitor charges from 0 and it will charge up to only $\frac{2}{3}V_{CC}$ only. Once if charges to $\frac{2}{3}V_{CC}$ the output becomes low. So, this is the starting point where this trigger value will be less than $\frac{1}{3}V_{CC}$ and it will stops here where the voltage at 6 pin is greater than $\frac{2}{3}V_{CC}$. This is the point where the voltage at pin number 2 is less than $\frac{1}{3}V_{CC}$.

In between if I want to make this to 0 even if you apply this trigger pulse again it will not respond. So, only way to bring this in between to the ground is you can apply a reset signal if you apply reset signal here. So, what happens this output becomes this output becomes 0 here itself it will becomes 0. So, you see the operation of this 555 timer.

Now, we can derive the expression for the time period t_P of this monostable multivibrator. So, for that we know that the voltage across the capacitor is $V_{final}[1 - e^{-\frac{t}{RC}}]$. So, what is V_{final}? This capacitor charges towards V_{CC}, but of course, if it charges up to the $\frac{2}{3}V_{CC}$ the output state will changes, but the final value will be V_{CC}. So, this will be $V_{CC}[1 - e^{-\frac{t}{R_aC}}]$.. So, see the output initially in standby mode 0 and whenever you apply the trigger whose amplitude is greater than $\frac{2}{3}V_{CC}$ it will go to high, it will stay in the high till the voltage at pin number 6 is slightly greater than $\frac{2}{3}V_{CC}$ after that it will goes to low. This is the pulse duration t_P. If I call this as t is equal to 0 and this as t_P. So, at t is equal to t_P what is this voltage this is $\frac{2}{3}V_{CC}$ output across the capacitor is $\frac{2}{3}V_{CC}$.

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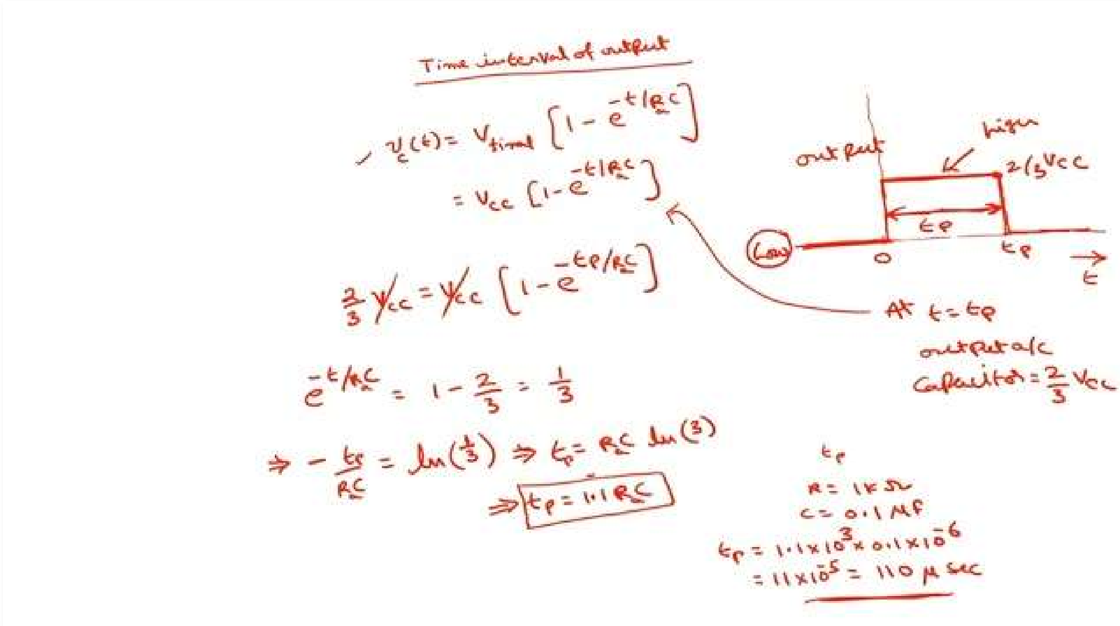

You can see from here also this is $\frac{2}{3}V_{CC}$ at $t = t_P$. This is the expression for voltage across the capacitor. If I substitute this condition here we will get $\frac{2}{3}V_{CC}$ is equal to V_{CC} times 1 minus e to the power of minus t becomes t_P this t_P which we are interested. V_{CC} V_{CC} get cancelled.

So, $e^{-\frac{t}{RC}} = 1 - \frac{2}{3} = \frac{1}{3}$ implies $-\frac{t}{RC}$ is equal to $\ln(\frac{1}{3})$ or if I make this as positive sign t is equal to $RCln(3)$ because this minus sign becomes plus if I take this as $\frac{1}{a}$ if it is $\frac{1}{a}$. So, a is $\frac{1}{3}$. $\frac{1}{a}$ becomes 3 this value will be this is of course, t_P $\ln(3)$ is approximately equal to 1.1

Of course, in the figure we are calling as R_a I have written as R both are same only you can write R_a only. So, this is the expression for this time period okay. By properly choosing R and C we can precisely generate the time delays. If R is equal to $1k\Omega$, C is equal to $0.1\mu F$ then what will be t_P? $1.1 \times 10^3 \times 0.1 \times 10^{-6}$. This 11 if I take this as 1 this is equal to $110\ \mu s$. You can precisely generate the delays of the order of milli as well as a microseconds also. So, this is monostable multivibrator this is having plenty of applications. So, before going for the application why this is called a monostable multivibrator? Because there will be only one stable state this is called low state this is high state.

So, this high state is temporary. So, whenever you apply the trigger pulse then it will go to high and finally, it will comes to low only. So, one stable state is low that is why it is called as monostable multivibrator. So, I will discuss some of the applications of this monostable multivibrator in the next lecture. Thank you.