Analog Electronic Circuits
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Lecture – 17
Differential amplifiers – I

Welcome to Analog Integrated Circuits, today's lecture 17 and I am going to talk about Differential Amplifiers continuing from the earlier class. So, in the earlier class we came up with our basic differential amplifier and over here you have 2 inputs v in plus v in minus and the expectation is that, the amplifier is going to amplify the difference between these 2 voltages and at the same time it is going to suppress the average of these 2 voltages.

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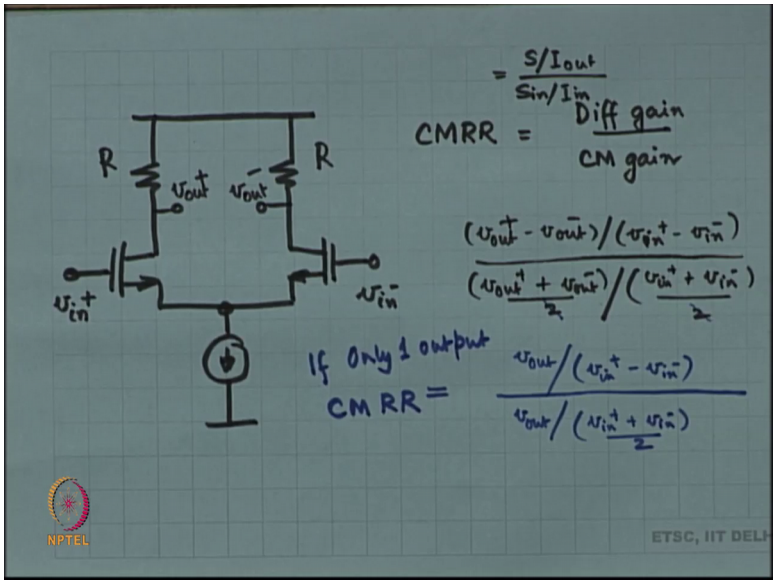

So if there is anything in the average of these 2 voltages that should get suppressed at the output whereas, if there is a difference between these 2 inputs then that should be amplified at the output.

Now, what is the output? There could be two ways of having the output one possibility is that the output is the difference of v out plus and v out minus. The other possibility is that the output is any one of the 2 output terminals any one of them. So these are the two possibilities, so output has two possibilities the input is the difference between the 2 inputs ok. Then we looked at we discussed the commonly used phrases, so the phrases

are the common mode signal, the differential mode signal, then the common mode half circuit, the differential mode half circuit, common mode, input differential mode input, common mode output, differential mode output, common mode gain, differential mode gain. And whenever I talk about common mode we are referring to the average, whenever I am talking about differential mode we are referring to the difference.

So, for example, differential mode gain is the difference of the 2 outputs divided by the difference of the 2 inputs that is differential mode gain ok. Common mode gain could be the sum the average of the 2 outputs divided by the average of the 2 inputs, could be if there is only 1 output then the average of the 2 outputs is just that 1 output divided by the sum of the average of the 2 inputs ok.

So, it depends on the context whether you have got 1 output or 2 outputs whether you have got common mode or differential mode ok. Now we also were discussing one more term called CMRR, so that is the Common Mode Rejection Ratio and we said that this is equal to the common mode gain divided by the differential sorry the differential mode gain divided by the common mode gain.

And in this case the differential mode gain if it is a perfectly the differential output differential input amplifier then the differential mode gain is v out plus minus v out minus by v in plus minus v in minus. And the CM gain is the average of the output divided by the average of the input all right and is by 2's cancel out just letting you know so it looks nice, the expression looks very nice.

So, this could be CMRR and this is basically also happens to be equal to the signal to interference ratio at the output divided by the signal to interference ratio at the input all right. Now suppose it is not a fully differential amplifier where the output has 2 terminals suppose the output only has 1 terminal, then there is no possibility of talking about interference at the output.

So this interference at the output is really not relevant any motion ok, so we are going to fall back to this and in such a situation where there is only 1 output. Then what is going to be CMRR? Once again it is going to be something like the differential gain by the common mode gain, but in this case the differential mode gain is v out by v in plus minus v in minus whereas, the common mode gain is v out by v in plus plus v in minus

by 2. Here the by 2 does not cancel out, here it canceled out nicely here it did not have the chance to cancel out, so beware all right.

So, this is going to be the CMRR, now when you do when you find out these common mode gains and differential mode gains then you have to do the superposition experiment, you have to turn off the differential mode signal to find the common mode gain. And if you are trying to find the differential mode gain you have to switch off the common mode signal ok. So, be careful do not have both running and then expect some nice answer it is not going to work out ok.

So, far so good let us try to analyze this circuit nicely right. This is the context I have over all right now given you the context so, far how this circuit came into being right. Now, let us try to analyze the circuit.

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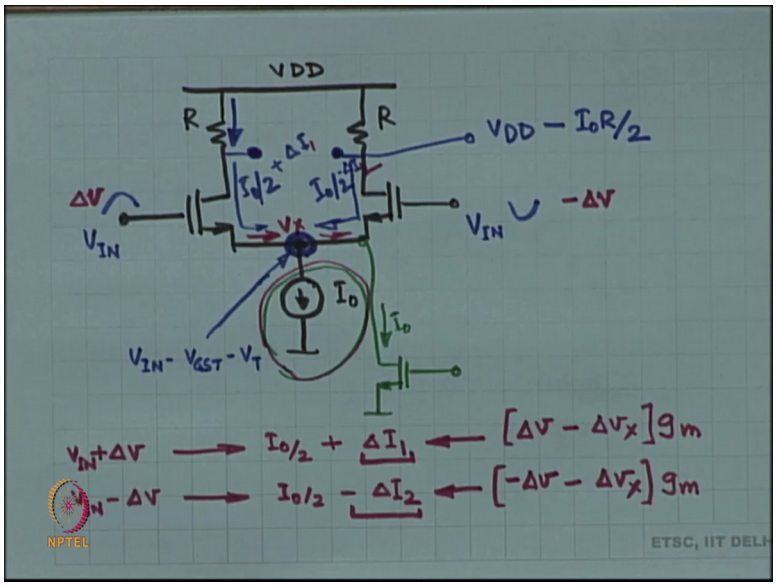

So as soon as you have a current of I naught and the circuit is symmetric, so therefore, what is going to be this current; I naught by 2 and here I will get another I naught by 2 all right so this is just by virtue of symmetry ok. Now, let us assume that the voltage here at the source of the input MOSFETs these 2 are the input MOSFETs, at the sources of the input MOSFET the voltage is flexible, because this voltage is the voltage across the current source right. Whatever that voltage is the current source is still going to conduct the same current, if it is an ideal current source let us assume it is an ideal current source ok.

So, this voltage the voltage over here at the source is flexible, so whatever is the DC operating point of the voltage at the 2 gates. Let us assume those are equal right they have to be equal because this is a symmetric situation, so suppose the DC operating point over here is V capital IN that is the DC operating point voltage. Now, the voltage at the source is going to be just right, so that I naught by 2 current comes through the MOSFET ok.

If I naught by 2 requires an overdrive of V GST gate overdrive of v GST; that means, the voltage over here is going to be nothing, but V IN minus V GST minus V T the absolute DC operating point voltage. And it does not matter what the value of this voltage is V IN could be V DD it could be something else right it could be V DD by 2 right now it does not matter ok. Right now as long as this current source is ideal this voltage is going to adjust itself just to the right value so that you get the right correct is this ok.

And therefore, the entire system is already biased, you do not have to worry about the DC operating point any further whatever DC operating point voltage this has needs to have something, you apply that voltage and you are done no specific value is required. However, later on you are going to replace this current source with a MOSFET right with an actual current mirror output right 1 or 2 maybe cascaded current mirror or maybe a single current mirror.

So this is going to be replaced later on there is no such thing as a an as an ideal current source, this later on we are going to replace with a MOSFET with the right biased value, such that I naught current flows through it right. In such a case you will have to make sure that V IN minus V GS minus V T is sufficient to maintain this device in saturation in it is flat region, like this device has to remain in it is flat region of operation otherwise it would not behave like a current source anymore, is that all right.

So, we understand that right now as long as we think of this as an ideal current source this voltage at this source of the input MOSFETs is flexible, it can be any arbitrary voltage. However, later on when you replace it with a MOSFET or cascaded MOSFETs whatever you want to do right there is going to be a limit to how low this voltage can go to, it cannot go to arbitrarily low voltages can go to higher voltages not lower voltages right. So this could be anything which is above V GST of this MOSFET right any higher

voltage is acceptable not lower. So it behaves like a current source as long as this voltage is higher than V GS minus V T of this green MOSFET is this all right.

Now, let us assume that we have picked the voltage source or rather the DC operating point value of these 2 inputs, such that this device is indeed in saturation and there is room right you keep some margin some headroom over here. So that maybe you know if the signal is larger or smaller it still remains in saturation ok. So for example, if I pick V GST of this device to be 0.2 volts then this should be something above 0.2 may be 0.3 volts is sufficient in which case V IN should be a V T plus V GST of this device above 0.3 volts right.

What is the voltage here at the output, what is the voltage, what is it? V DD minus minus I naught by 2 current is flowing through the resistor this should be straightforward and both sides are at the same voltage. And what needs to be done to make sure that these devices are in saturation in their flat regions of operation, what needs to be done? We have to make sure that this voltage minus the bottom voltage V V this source voltage is more than V GST of the input devices, so that is also crucial ok. We have to make sure not only is the current source in saturation we also have to make sure that the 2 input devices are also in saturation.

So, this has to be carefully arranged all right. Now once you have arranged this then you proceed further you are going to think about what happens when I apply a signal. So suppose I slightly increase this signal and at the same time I slightly decrease the voltage over here equal and opposite. So I increase this voltage a little bit, I decrease the voltage on the other side a little bit by the same amount. What is going to happen? This voltage has gone up so therefore, the current is going to increase so I will get I naught by 2 plus some delta I ok, but this is the current source.

So, therefore, on the other side I have to have I naught by 2 minus the same delta I you have no choice because the bottom one is a current source ok. And because they are going equal amounts up and down this probably make sense that one is plus delta I the other is minus delta ok. In which case the voltage over here did not have to change at all if these two had not been equal. If this was not if this was plus delta I and this was not minus delta I if this was something else, then the voltage here would have to adjust ok.

The voltage here is not guaranteed to be the same because you went up by some amount down by equal amount and you got different changes in the two halves.

So; that means, the something happened over here as well ok. Now that is not the case the change on both currents is equal so therefore, this voltage over here is constant did not change at all did not need to change at all ok. This is understood or not? It is not understood let us try to do it yet again. I increase this voltage by delta V, I decrease this voltage change this voltage by minus delta v on one side I increased it by delta v on the other side I decrease it by delta v all right. Presumably the current on this MOSFET is going to increase it is not going to decrease right if I increase the voltage the current is going to increase ok.

So, this is delta I let us not worry about this current source, let us say there is something else over there for now. And let us say this is not minus delta suppose this is delta I 1 and this is minus delta I 2, so when I increase by plus delta v I get a response and when I decrease on the other side by minus delta v I get a response and why did the current change because V GS changed.

So, let us call this sum V X all right so the response over here is so this delta I 1 is a response of delta v changing minus the source voltage let us say it changed. This created delta I 1 and minus delta I 2 is the incremental change caused by minus delta v and the source voltage changed by delta v X all right. Now these two happen to be equal so some g m ok.

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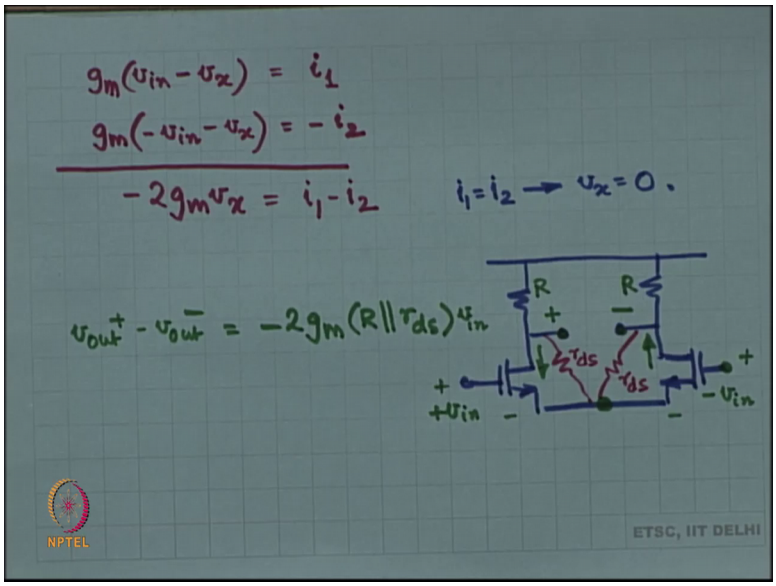

In other words small signal plus v in is applied to the gate of the right hand transistor or left hand transistor right. Let us say the center node changed by small signal v x so v gs is v x this times g m is the incremental change in the current on the left side ok.

And on the other side I had I applied a small signal minus v in and the source changed by v x and this was minus i 2 ok. If I add these two expressions what do I get add them g m v in g m minus v in they cancel out g m minus v x gm minus v x so it comes out to minus 2 gm v x is equal to I 1 minus I 2. And what is I 1 minus I 2? It is 0 I 2 is the incremental current in this direction, I 1 is the incremental current in this direction because this happens to be a current source I 1 minus I 2 is absolutely 0. If it is not a current source then we had a problem , but if it is a current source then I 1 minus I 2 is 0 in which case v x is 0 all right.

So, there is no change this node is static this node is sitting idle static, I increase this voltage by delta v decrease the other voltage by delta v this did not change and that we saw by virtue of symmetry as well ok. Now when I increase this current responded plus delta I 1, when I decrease this the current responded minus delta I plus delta I minus delta I. So the plus delta I caused an extra current plus delta I through the resistor so an extra drop across the resistor which means that this node v out plus node went down extra by delta I times R and that delta I went up over here which means that this node went up by delta I times R ok, or in other words ok.

So, I am not drawing the current source, because this is the small signal equivalent picture and in the small signal equivalent picture I know I just prove to you that v x is a constant, the v x is equal to 0. So this node is not moving at all ok, there is a current source over here, but this node is not moving which means that the entire v in, that you applied across the first device creates an extra current g m times v in this creates a current g m times v in the other way because this is minus v in ok.

So, so circulating current signal current the voltage here drops by g m times v in times R, the voltage here dropped increases by g m times v in times R of course, right now I am assuming that r ds is infinite. Now if you also had r ds then r ds would appear in shunt with R would not it, because this node is not moving all right in which case this voltage is going to drop by g m times R in parallel with r ds whereas, this voltage is going to increase by g m times R in parallel with R ds.

And net if you look at the difference of these 2 voltages you will get 2 times minus 2 times g m times R in parallel with r ds times v in of course, your input differential signal is 2 times v in over here because one was increased by v in the other was decreased by v in. So, the difference between the 2 inputs is 2 times v in which means v out plus minus v out minus divided by the differential input is nothing, but minus gm R in parallel with r ds is this ok.

Now, you could have solved this using the half circuit method as well right, in the half circuit method what you declare is that this is a perfectly symmetric circuit, this is a perfectly symmetric circuit. And if I increase the input and decrease the input by equal amounts, when that automatically means that this node is at ground.

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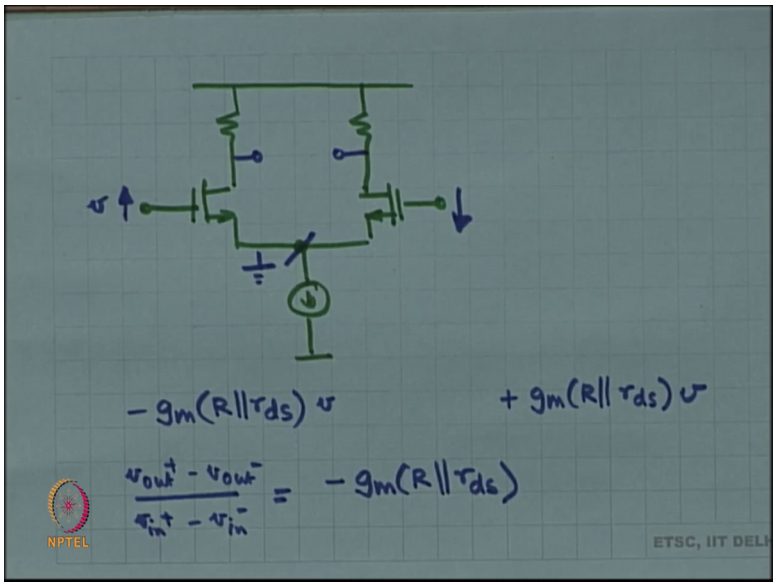

Now the two halves of the circuit are decoupled from each other if I increase one side by v then the response at the output is going to be the output impedance is R in parallel with r ds, the transconductance is g m so the response is going to be minus g m times R in parallel with r ds. This is one output voltage times v the other output voltage is also easy the same right, but with minus v, fine all right.

And then what do you do then you say that the total differential output is the difference between these two which is 2 times this result ok. The differential gain is the difference between the 2 outputs divided by the difference between the 2 inputs, which happens to be just so much. Now if you are smart then you are going to see that this result and this result are pretty much identical, so you are just going to solve half of the circuit and declare victory you are not going to follow through you can declare victory straight from here you can identify the answer right away ok.

Then the signal the 2 inputs can always be broken up into a common mode part and a differential mode part, so some average signal and some differential signal like we did in the last class. And then you have to do super position between the differential part and the common mode part right we did this in the last class.

So, v 1 and v 2 are the 2 inputs let us say v 1 can be broken up as v 1 plus v 2 by 2 plus v 1 minus v 2 by 2 you remember ok. So, one is the common mode part the other is the differential mode part. So in general v and v are not going to be anti symmetric all the

time there might be some common mode component to it as well so they could have some average as well. So, you also have to find out the response to the common mode.

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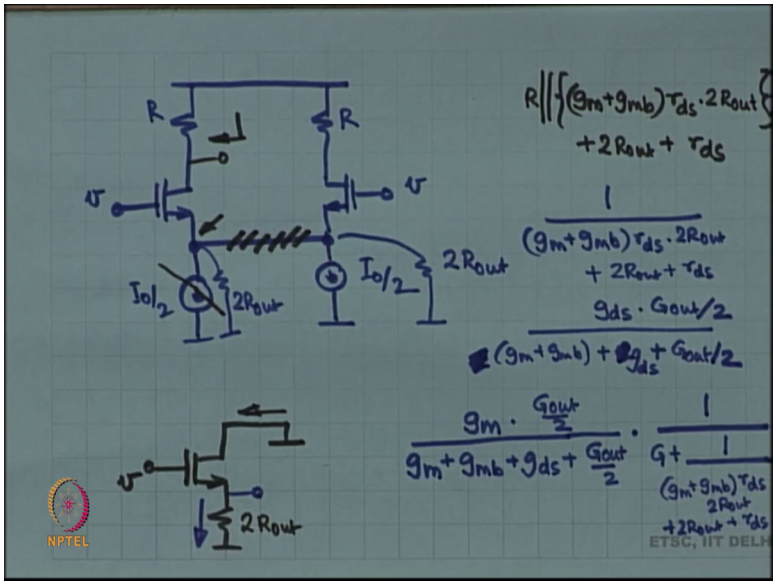

So, now what we are going to do is instead of that one current source I am going to split it up into two current sources what I naught by 2 each or in other words if that one current source had some output impedance, some finite output impedance then that finite output impedance whatever it was R out let us say that splits up into 2 pieces in parallel 2 times R out 2 times R out ok, that is the non ideality of the current source.

And then you say that if both the signals are equal, then no current flows through the wire in the middle and you cut it off and now you have two decoupled half circuits right they do not they are no longer talking to each other, they are isolated from each other. So you just solve each of these they are both the same and what are they in the small signal picture this I naught by 2 does not really matter right in the small signal picture this is a source regenerated common source amplifier and you know how to solve this right.

How do you solve it? First you find out the voltage over here, how you find out the voltage over there? By solving for the common drain remember to solve this you have to do short circuit current and output impedance, two experiments output impedance is very easy looking in from the output you see R on top and what you see on the bottom intrinsic gain of this MOSFET times 2 R out plus 2 R out plus r ds.

So, output impedance is R in parallel with fine so this is the output impedance done and then in the next step you also have to find out the short circuit current. Now when you went go to do the short circuit current this is really your experiment, you are trying to measure this correct. You apply voltage v try to measure the current, now this is the common drain circuit and the way you do it is to work out the voltage over here right in the common drain circuit. The voltage over here was slightly less than v how much less than v was it you can do it again. That is you can find the output impedance and the g m looking in from here short circuit current over here that will give you the voltage or just recollect a little bit all right, think a little bit.

So, if you think you can remember that this common drain circuit has again which is slightly less than 1 slightly less than 1 means it is gain is going to be some g m divided by something, what thing would it be g m plus body effect played spoilsport over here. So, g mb plus g ds plus well the smaller this resistance is the worse it is going to be 2 R out the conductance is G out by 2, 1 by 2 R out. So that is G out by 2 ok, so that is the voltage over here if this is the voltage over here then the current is this voltage divided by 2 R out or this voltage times G out by 2 that is the short circuit current fine.

So, this is the short circuit current this is the output impedance, output impedance could be rewritten as 1 by output conductance g plus 1 over this, what is this I am resolving be effectively I am redoing something that you have done before in this course only right. I am just trying to give you some practice ok, this is how you are going to do it. Output impedance short circuit current, so this was the short circuit current expression, transconductance expression, this is the output impedance expression and when you work with g's sometimes, when you work with conductances sometimes, these parallel things work out much better right.

So, that is why I am I am translating from resistance to conductance ok, so this also has to be translated. So 1 by g m plus g mb times r ds times 2 R out plus 2 R out plus r ds can you convert this to conductance, so multiply numerator and denominator by g ds and multiply numerator and denominator by G out that is all that you have to do. So this is going to be g ds times G out divided by g m plus g mb r ds goes away R out goes away so 2 remains plus 2 R out so 2 remains plus sorry 2 R out 2 gds remains and r ds becomes G out ok.

So, this is this expression converted to conductance so this is the corresponding conductance all right and if you do not like it then divided by a factor 2 and suddenly look it is starting to look like this, that is why we did it this way so your net expression is going to be

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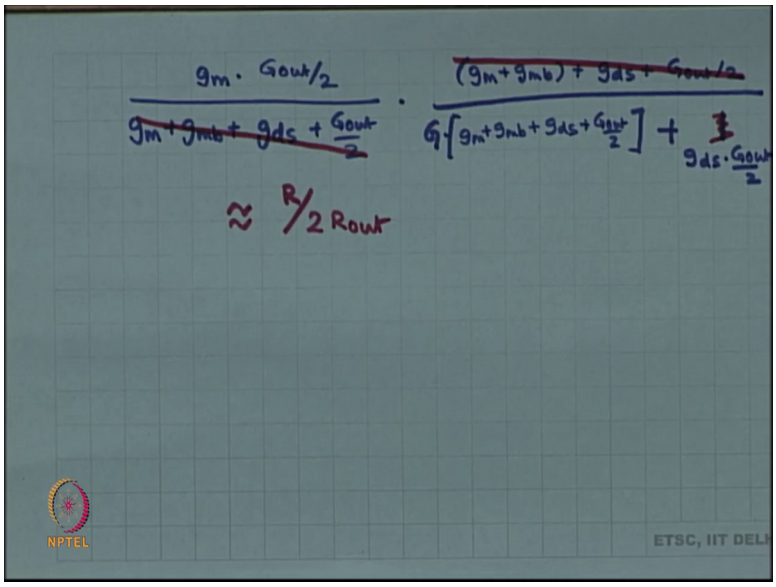

So, this is the short circuit current portion and then no I am sorry all right and then you are going to have some canceling sessions this entire numerator will cancel out with this entire denominator ok. That is number 1 and then number 2 is you are going to see what happens when G out by 2 is small.

So, if G out by 2 is small and also if g m is large so if G out by 2 is small and g m is large compared to g ds then this entire expression boils down to G times g m g r by 2 is small g m is large compared to g ds and G G out by 2. So this is not relevant so all you get in the denominator is G times g m in the numerator you have got G out by 2 times g m the g m cancels out and all you are left with is G out by 2 by G or in other words R by 2 R out ok.

So, this is your sanity check that indeed your expression is more or less correct ok. Why is this because this is the source degenerated amplifier, source degenerated amplifier on the drain you have got R and on the source you have got 2 R out. So the voltage follows this is v this is going to be approximately v so the current is v by 2 R out same current comes through over here, so the voltage over here is minus v times R by 2 R out all right.

And you have to adjust for the sign in all of this you have to adjust for the sign because you do not know which way you took the transconductance ok. So do it just for the sign and then you get the overall gain, from this expression you should also be able to say what is the common mode rejection ratio oh by the way what are we doing sorry, what are we doing. We have so far found the response of this voltage to a voltage v likewise the other voltage also will respond in the same way the average of the 2 is going to be just one of them because they are equal and the average of these 2 is just v ok.

So, average by average is equal to just this fine, so that is your common mode gain when we are saying average of outputs by average of inputs, common mode of output by common mode of input all right. Now sometimes you are also interested in working out, what is the difference of the 2 outputs when you apply a common mode input. So this is a more practical scenario, so in the lab when you work it out especially in the lab right when you are going to measure you are going to measure the difference of the 2 outputs divided by the common mode at the input ok.

So, once again the definition of common mode gain changes based on context, so when you are in the lab you are probably thinking of difference of 2 outputs by the average of the 2 inputs ok. If everything is matched that is if this half of the circuit is identical to the other half of the circuit then the difference of the 2 outputs is 0 all right. So in theory there is no point in trying to measure this it is equal to 0 we know beforehand. In the lab however, this is what is straightaway interfering in your signal right this is the interference that went into your signal and is becoming part of it ok. So, this is not a very nice thing it is not very nice to have common mode leaking into the differential mode.

So, that is what you are going to measure in the lab however, as part of as long as we are doing theory over here the average of the 2 outputs divided by average of the 2 inputs happens to be this. The difference of the 2 outputs by the average of the 2 inputs is equal to 0 is this ok. Now it so happens it just so happens that if there is mismatch in the circuit that is these two halves of the circuit are no longer identical, if that happens if the circuit is no longer completely perfectly matched this half no longer the mirror perfect mirror image of the other half.

Then the common mode at the output that is the average of the 2 outputs starts leaking into the differential mode of the output that is the difference of the 2 outputs. What I am

trying to say is the common mode at the output the average of the 2 outputs is proportional to the average of the 2 inputs by this gain factor, by this gain factor hopefully this is close to 0, but it is still something. So the average of the 2 outputs is proportional to the average of the 2 inputs by this factor.

Now, when the two sides are not perfectly matched then the difference of the 2 outputs also has a proportionality to the average of the 2 outputs and you will get this factor times the mismatch factor right. That will be the difference of the 2 outputs by the average of the 2 inputs, so I am applying a common mode input no differential signal yet I will see a difference in the 2 outputs and that happens to be proportional to the common mode gain.

So if the common mode gain is very low that is the common mode output by common mode input is very low, then that is also going to be very low. However, if that is significant then the leakage of the common mode into the differential mode is also going to be significant ok. And this is I am not going to prove it right away, but this is subject to a lot of conditions however, this is engineering practice.

So, that is why it is very important to suppress as far as possible this common mode gain you do not we do not more like this common mode gain at all, we do not want the average of the output to change when the average of the input is changing after all this is the interferer right. I want to make sure that signal to interferer ratio of the output at the output is much larger than the signal to interferer ratio at the input that is I want to get rid of the interferer altogether all right.

So, far we are we have been studying this basic circuit as our differential amplifier ok, so if I said to say that you can modify this circuit in any way you want and you can still use the same techniques that you have studied for example, I could modify this circuit.

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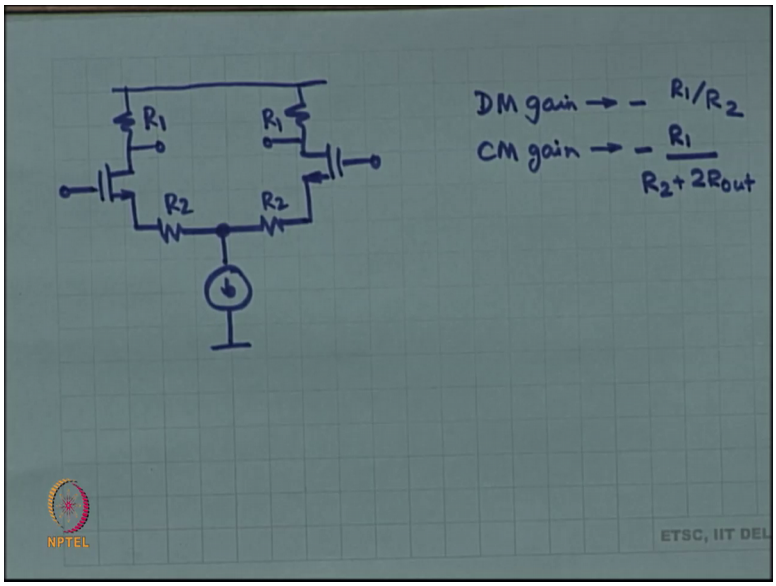

And make a new circuit which is also a differential circuit, because will you be able to analyze this you will yes you will because you are going to use the method of the common mode half circuit and the differential mode half circuit as long as there is symmetry in the circuit ok. If symmetry is not there then unfortunately you cannot use that technique at all right. You have to think of other techniques, but as long as there is symmetry in the circuit you can use the common mode and differential mode half circuits and work it out.

So, in this case the differential mode gain is going to be approximately minus R 1 by R 2 the common mode gain is going to be approximately minus R 1 by R 2 in series with R out by 2. Yes, this is going to split up into 2 pieces R out sorry 2 R out 2 R out and in between you will cut the wire so you will get R 2 in series with 2 R out. So differential mode gain minus R 1 by R 2, CM gain minus R 1 by R 2 plus 2 R out approximately ok, common mode rejection ratio is going to be differential mode gain by common mode gain, so that is going to be R 2 plus 2 R out divided by R all right usually CMRR is expressed in decibels is this all right.

So, any other circuit so this does not have to be the only differential circuit this is not the only differential circuit any other differential circuit, you identify the symmetry in the circuit and then analyze it all right. So you identify the symmetry and you see that this side is totally equal to the other side and then you split it up into 2 halves and analyze the

common mode and the differential mode right ok. Now, we are going to look at the analysis of the same old differential circuit in a different way and this is important.

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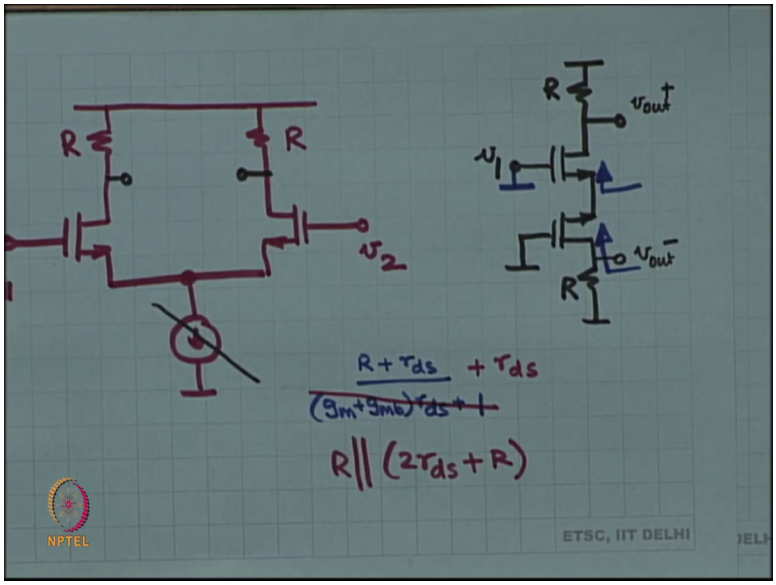

Let us apply a signal v 1 over here and let us apply a signal v 2 over here and instead of splitting up v 1 into v 1 plus 2 by 2 v 2 by 2 and v 1 minus v 2 by 2 and likewise v 2 instead of doing that we are going to do a direct superposition. Once I will apply v 1 and 0 volts and the next time I will apply v 2 and 0 forms and let us see what the responses these are after all simple 2 transistor circuits what is stopping me from analyzing it that way the ordinary way is the result the same it should be the same.

So, this is the analysis that we are going to do now, now it so happens that this is one of the few ways that you can do it naturally when there is mismatch in the circuit. When there is mismatch in the circuit otherwise, you are going to find it very difficult to analyze if these 2 MOSFETs are not identical. If these 2 resistors are not identical then you will be at a loss how to analyze the circuit at all right. So you need to know how to analyze the circuit using brute force superposition that is v 1 and 0 v 2 and 0 ok.

So, let us apply v 1 and 0 and small signal analysis this current source is not relevant all right. So let us redraw the circuit and now I am going to redraw it in a peculiar way. So once, I am going to take the output here I will also have to take the output at the other node and naturally you are not comfortable drawing this MOSFET upside down ok, it is very disconcerting. If you want you can convert it to a PMOS this I mean there in the

small signal diagram the NMOS and the PMOS are identical, so it is to change it over to a PMOS nothing significant is going to happen it is after all small signal circuit all right.

Now, we have to analyze this which one do you want to do first v out minus v out plus let us do v out minus ok. So if I want to do v out minus I need to work out the output impedance from v out minus and I also need to know the short circuit current if v out minus is connected to ground ok. Look it is the same technique over and over again all right same technique the output impedance the short circuit current.

Now, if I look at the output impedance, if I go in from v out minus I look down I see R and I look up what do I see, I am looking into the drain of a MOSFET where the source has some stuff ok. So I have to pick my correct formula, but what is on the source if I look up from this source this is at ground by the way when you are doing the output impedance. This is at ground by the way this output impedance will work both ways this output impedance is the same, whether you look in from v out plus or whether you look in from v out minus. It is the same whether you have applied signal at v 1 or signal at v 2 the output impedance answer is the same no matter what ok, so you better do it right.

So, looking up from here what do you see? So this is at ground looking up from here what do you see this is one of your formulate the 2 formulate right you are looking into the source drain is dominated by R. So you see R plus r ds divided by divided by the intrinsic gain of the MOSFET plus 1 all right. And now you can figure out what is the impedance looking up on this right it is going to be this MOSFET, the intrinsic gain of this MOSFET times the impedance on the back side plus the impedance on the back side plus r ds ok.

Effectively it is this impedance times 1 plus g m plus g mb r ds of this MOSFET which is the same. So this entire portion is going to cancel out plus r ds fine so that is the impedance looking up so 2 r ds plus R looking up and looking down it is just R. So the net impedance is R in parallel with 2 r ds plus R ok. Let us stop here we are going to continue this analysis in the next class all right. And we are going to proceed from here, but think about it whichever way you look you get the same answer; this very special circuit ok.

Thank you.