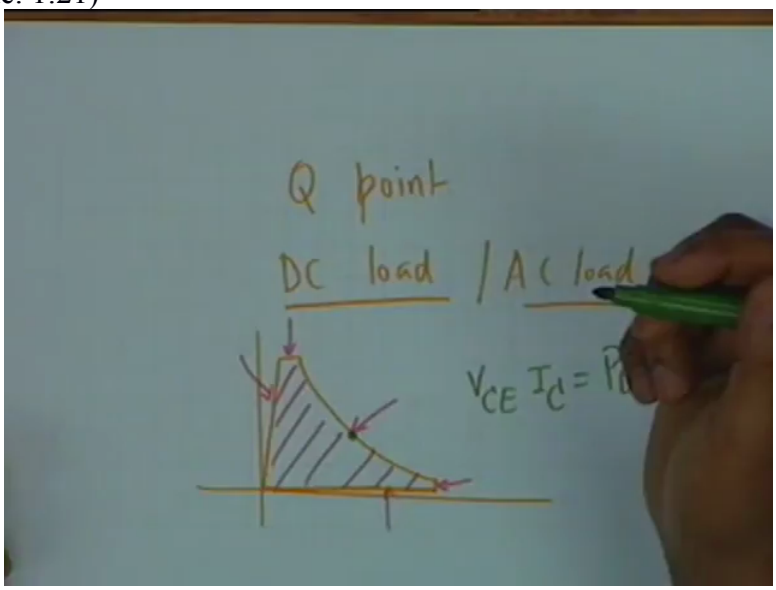
Introduction to Electronic Circuit
Prof. S.C Dutta Roy
Department of Electrical Engineering
Indian Institute of Technology Delhi
Lecture 32
Power Amplifiers (Contd.)

(Refer Slide Time: 1:21)



32nd lecture and the topic is power amplifiers that we started yesterday we continue discussion on power amplifiers. Yesterday's lecture was mainly concerned with determining the Q point and the distinction between DC load and AC load for amplifiers which have to handle a signal the DC load may be different from AC load for amplifiers which have to handle a signal the DC load may be different from AC load and AC load resistance is usually smaller than the DC load resistance.

And these considerations, the other considerations that come into play is the maximum available VCE, maximum available participation, the maximum available collector current I sub C, the minimum available I sub B the base current which is 0 and this saturation line that is the line below which the collector base junction is no longer reversed biased then we saw that in the I sub C versus VCE characteristic the power amplifier operation should be restricted to a region like this.

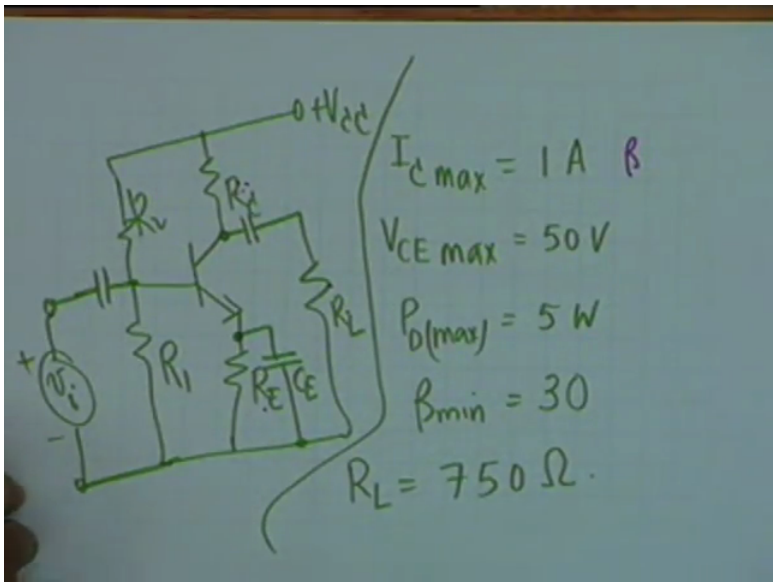
A region bounded like this, this is the saturation line, this is the maximum I sub C line, this is the PD line power dissipation line, this is the maximum VCE line and this is the minimum I sub B line, alright. So this is the region we can reach the operation has to be restricted. Now in this region also the choice of Q point as we have illustrated last time has to be done quite carefully and the transistor in order that you get the maximum possible power to be load the

transition has to be driven to its ultimate limit which constraints that the Q point must be on this line.

Q point must be on the P sub D line that is the line on which VCE I sub C equal to a constant P sub D here also wherever you choose the Q point, the load line should then be tangential to this hyperbola. Now you can choose various Q points and find out find out what load is occurred? The load will now be determined by whether you want the maximum voltage swing or maximum current swing and we decided last time that because of distortion considerations perhaps the voltage swing should be maximize.

Perhaps the voltage swing should be maximized, alright. Let us with this few preliminary remarks let us now illustrate with the help of an example. How one goes about designing a given power amplifier?

(Refer Slide Time: 4:45)



The specifications of a given transistor which is to be used under the circumstances is that I sub C max is 1 ampere, alright. VCE Max these are all specified by the manufacturers, VCE Max is 50 volts, now this is no surprise because you have to deliver power; power transistors usually have a much larger rating than voltage transistor and current transistors. PD Max that is the maximum power dissipation is specified as 5 Watts.

Minimum beta, beta min is specified as 30 and in addition a load RL is specified to be 750 ohms and the design is required to be done in such a manner that maximum power is transferred to the load, maximum possible power. As a kid is the usual self biased circuit that

is you have an RE than R1, R2, R sub C this is plus VCC and the load, load is specified 750 ohms and it is also specified that the load should not carry any VC.

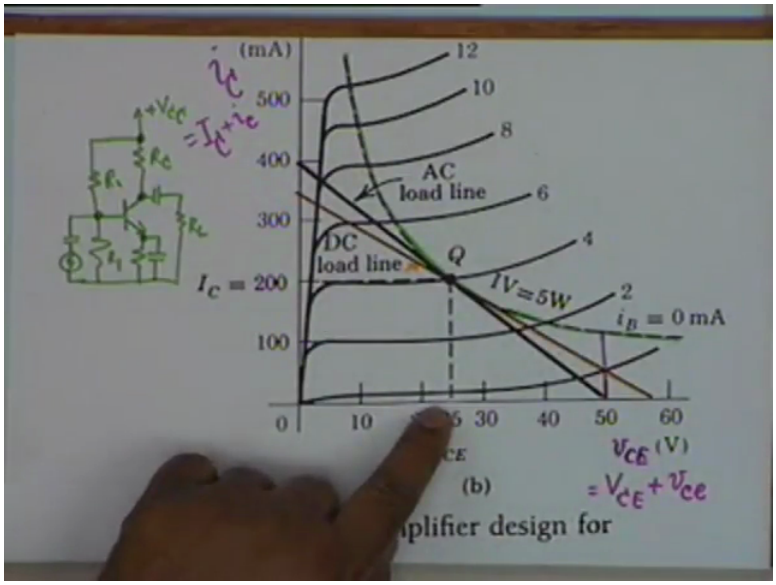
In other words you have to isolate the load by means of a capacitor. So this is a load Rl, the DC load this RE is to be bypassed by a capacitor, this is a blocking capacitor and then the signal is to be applied through another capacitor, alright. This is the input signal; input AC that is a Vi, alright. This can be input AC source Vi, this is a blocking capacitor, this is a blocking capacitor.

This C sub E is a bypass capacitor because this bypasses RE, here reverse for AC RE behaves as a short-circuit because of the capacitor CE. Now you see the power amplifier design has to be compromise between many factors many situations, these maximum specifications, these 3 must not be (()) (7:19) number 1 under such circumstances, how do you choose your Q point and the AC load in order that maximum power is delivered to a part of the equivalent AC load.

The equivalent AC load obviously is a parallel combination of R sub C and R sub L and we do not know, we know RL we do not know RC, RC is to be determined, alright. So power of the some power would be wasted in RC the rest of the power will go to RL but what you to RL must be the maximum possible 1, there is some power wasted in RE also because some VC passes through this, alright.

And we (()) (8:04) you see the DC at DC the effective load is RC plus RE, if beta is large if beta is large then the effective load at DC, at DC RL does not come into operation. So effective load is simply RC plus RE and the effective AC load is RC parallel RL which obviously is less than RC and therefore the AC load is less than the DC load.

(Refer Slide Time: 8:52)



In order to see how to choose the Q point lets appeal to the characteristic curves of the transistor the i sub C VCE characteristic, alright. This is I sub C in milliamperes plotted versus vce you notice the nomenclatures small i subscript capital C this denotes the total collector current, total current that is DC plus any signal current. Similarly small vce is the sum of capital VCE that is DC less any AC, is a would be denoted by small v subscript small c small e.

Similarly I sub C is capital I sub C plus small i sub small c, alright. IC versus vce characteristic and these are the usual characteristics this space that equal intervals of I sub B, this is for 0 milliampere, this is for 2, 4, 6, 8, 10, 12 and so on, line this is a saturation line your VCE should not go below this and then the base collector junction shall no longer be reverse biased.

And you should not exceed a certain maximum VC, VCE maximum is specified to be 50 and therefore this is your ultimate line, this line, what did you call this line earlier? The B line or what was it called? Does not matter there was a line here. So your VCE Max is 50 therefore you must have exceed this voltage, alright. Now the power dissipation maximum is specified as 5 watt.

So what you do is, you draw the 5 watt hyperbola on this characteristic which is the green line, this is the green line gives the lot of IV that is I sub C times VCE equal to 5 volts, so it is a hyper Bola and the Q point must be located on this hyper Bola, alright. Now since 50 is the

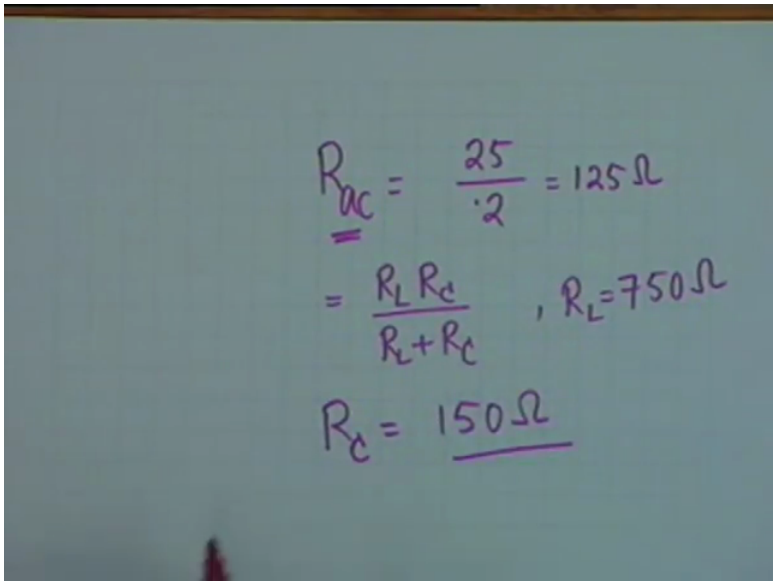
maximum along VCE then you want maximum voltage swing and maximum possible current swing.

Well, in between the 2 we choose the maximum possible voltage swing because the characteristics are more linear in the region of high-voltage swings rather than in the region of high current swings there are many nonlinearities here, alright. So we allow our VCE, we must understand this carefully. We allow our VCE Max to be absolutely the limit 50 volts then what should be the Q point?

If we want maximum possible swing of this that the Q point should be at approximately half VCE Max that does not mean that you can go up to 0, no. You cannot go up to 0, why not? Because there is a saturation line, alright. But approximately your Q point is at 25 and therefore at 25 if you draw a vertical line this cuts the PD hyper Bola that is the green power dissipation hyperbola at this point Q which should therefore VE of Q point and this is how we determined a Q point?

Now you know your Q point and you know what is the maximum VCE? And therefore you know the AC load line also; this orange line is the AC load line. Is that clear? From which you get the effective AC load resistance as voltage swing which is 25 volts divided by the corresponding current swing is 200 milliampere that is 0.2 and therefore what is Rac then?

(Refer Slide Time: 12:54)



The effective Rac will be equal to 25 divided by 0.2 ampere which means 125 ohms, is it clear? How you determine the effective Rac. Now what is effective Rac? It is a parallel combination of RL and RC, where RL is specified as 750 ohms, alright. Therefore you know what is RC, is that clear? RC by calculation it comes out as 150 ohms.

(Refer Slide Time: 13:34)

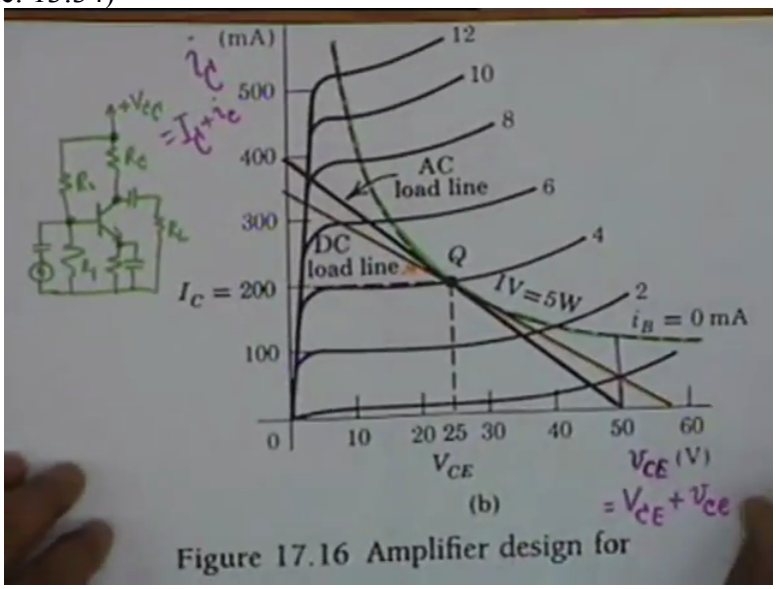
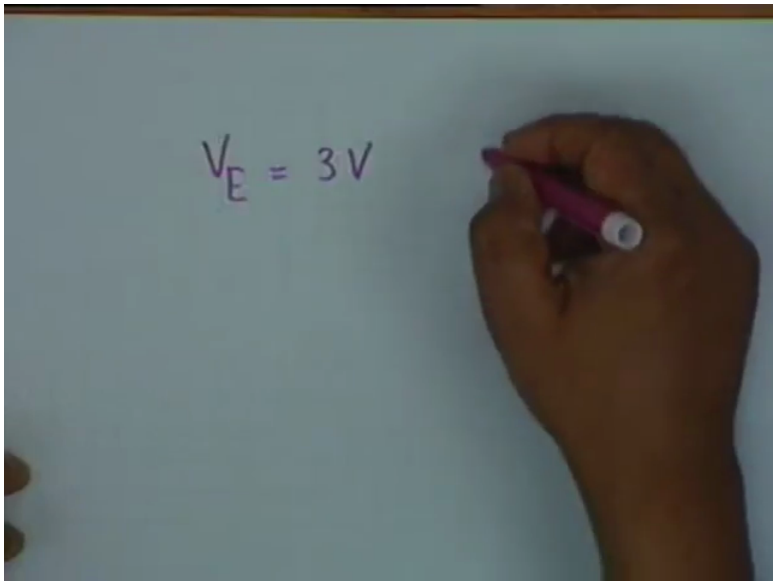


Figure 17.16 Amplifier design for

And therefore in this circuit this is determined this is known, RL is known, all that now one has to determine is RE this resistance, can you see this guideline? Is this okay, visible from the last bench? Yes, here we determine R E, R1 and R2 thus the design is complete, alright. Now to determine RE, to determine this resistance, now we do not know RE, do we know I sub C? Yes we do.

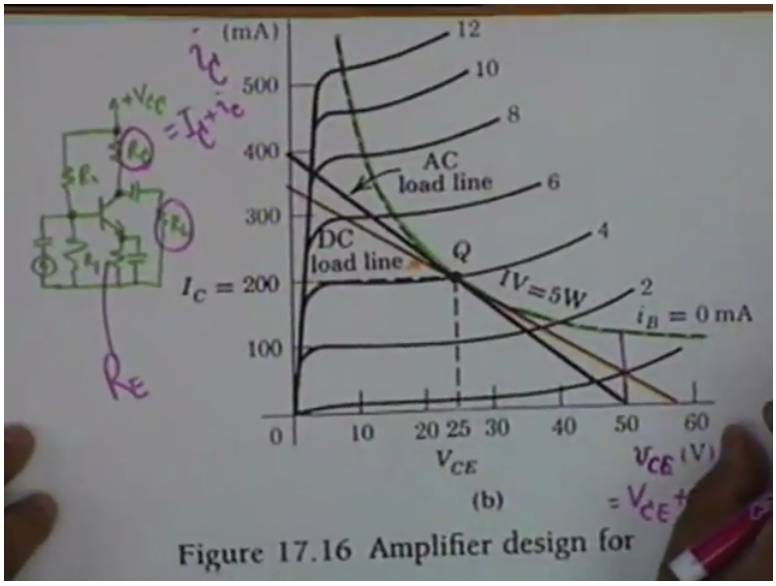
What is I sub C? I sub C is 0.2 ampere at 200 milliampere and therefore we have to arbitrarily fixed V sub E this is a situation where RE is not known and therefore we arbitrarily fixed VE and we can tweak any value that we like, we still do not know what is VCC? And therefore arbitrarily let us put a few volts as VE and typical figure is 3 volts you can choose 4 you can choose to there is nothing sacred about it, provided you choose beta you choose RB that is R1 parallel R2 that has to be chosen as beta minimum times RE divided by 10, alright.

(Refer Slide Time: 15:12)



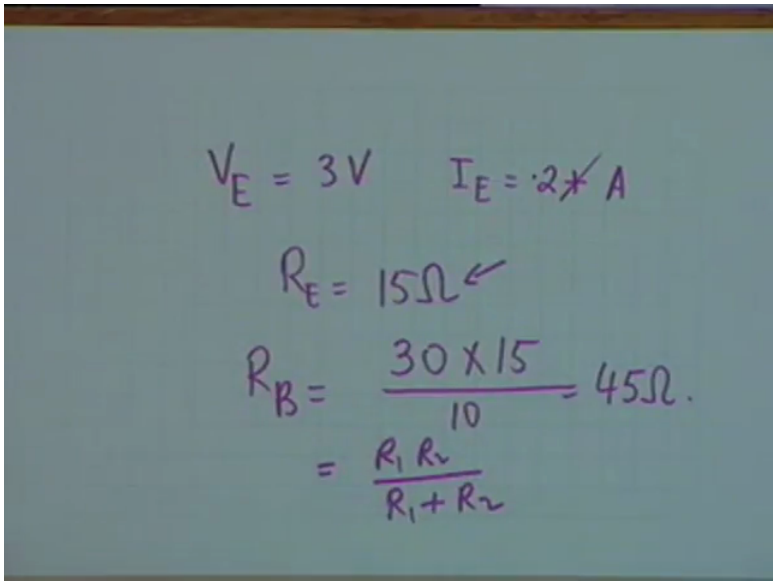
At least it would be better than this, okay. So, what we do is, we assume that VE, we assume that VE is equal to 3 volts then what is I sub E? I sub E is 2 to 200 milliampere, okay. That is 0.2 plus I sub B.

(Refer Slide Time: 15:28)



Now you can see this, what is I sub B at the Q point? It is 4 milliampere that means 0.004, is that correct? Which means that for milliampere can be neglected compared to 200? The calculation would not be absurdly upset by this negligence, alright.

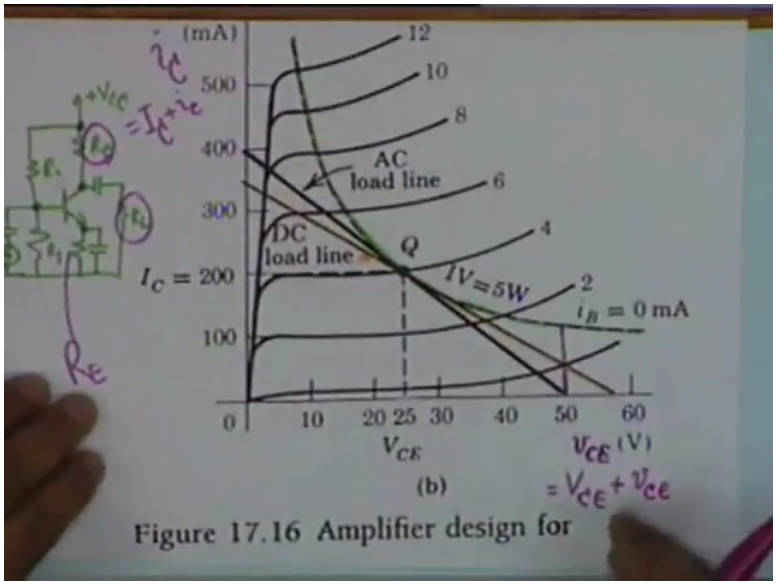
(Refer Slide Time: 15:57)



And therefore we say I sub E is 0.2 ampere which means that RE shall be equal to how much? 15 ohms, now you must be surprised that this low values of resistance because it is a power amplifier and your idea is to deliver power, maximum power to a load is low as 750 ohms, alright. And therefore RE has come out as 15 ohms. If RE comes at 15 ohms then what is RB?

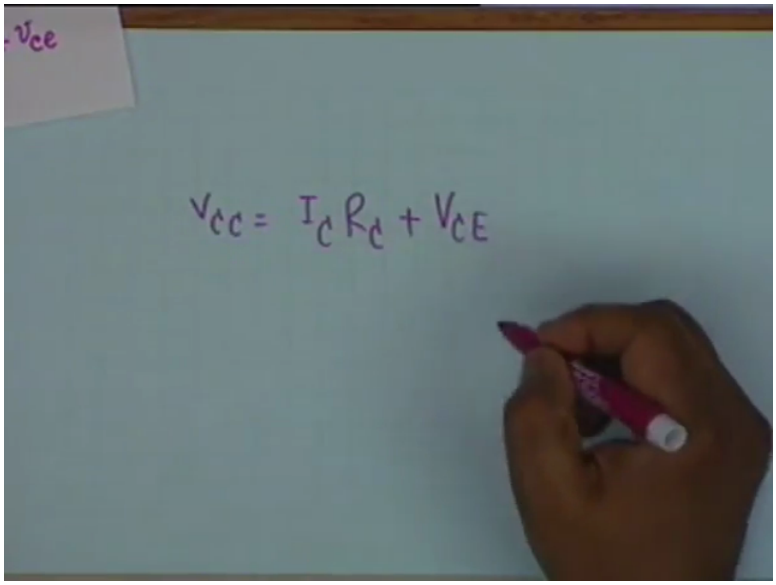
RB shall be beta minimum; beta minimum was specified as 30 times RE that is 15 divided by 10 which is 45 volts, alright. So and this is equal to R1 and R2 divided by R1 plus R2, alright this is one of the equations and other equation would be determined in terms of VBD but to determine VBD, we must find out VCC, what is the power supply needed?

(Refer Slide Time: 17:08)



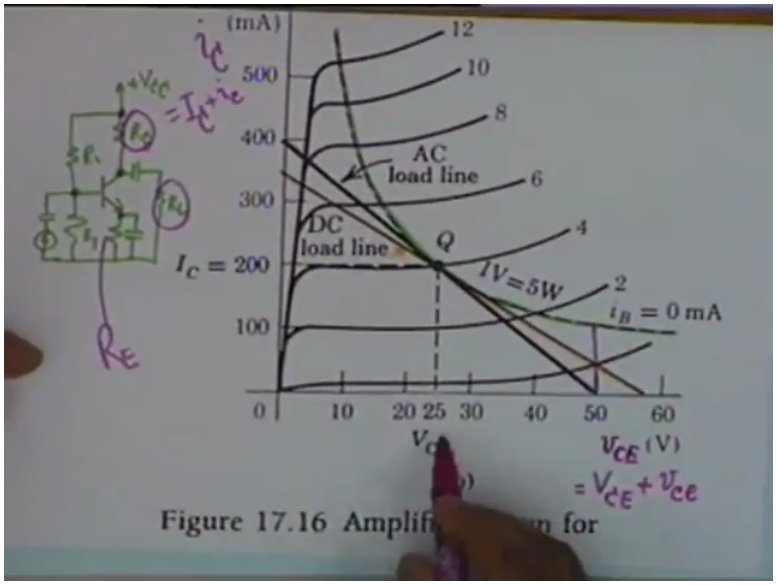
This characteristic curve gives no idea about the power supply that is needed, does it or does it not? Since you know R sub C and you also know RE, do not you know the VC load line? Okay, in fact is line, this orange line is the DC load line it goes right up to some 58 volts, is a point clear? You can get what VCC is needed right from the characteristic cards, why? Because RBC, in the circuit RBC simply RC plus RE and we have ignored, ignored the I sub B component, alright. So one, if you draw a line at Q with a slope of minus 1 by RC plus RE which is 150 plus 15 that is 165 then that will be this orange line and wherever the orange line cuts the VCE axis, it shall be equal to VCC, is that clear?

(Refer Slide Time: 18:35)



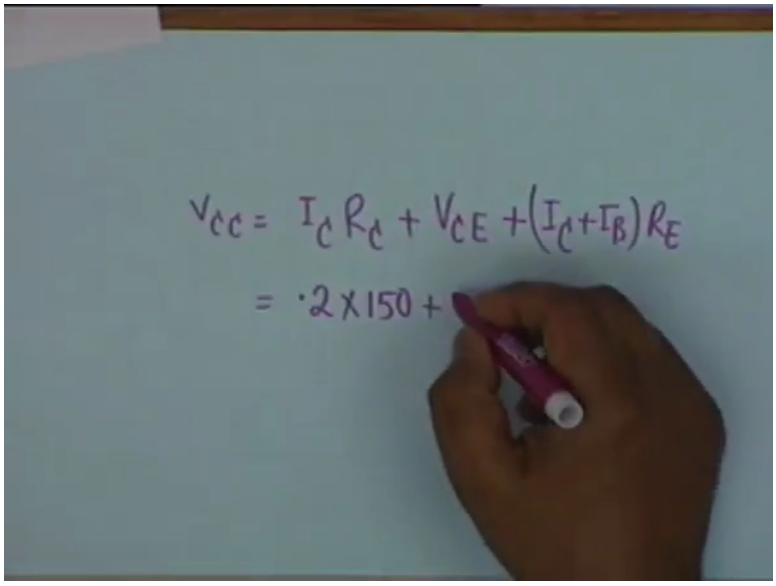
And therefore we know VCC, if that does not appeal to you, if you prefer to calculate this, alright you do calculate, VCC shall be I sub C R sub C plus VCE plus I sub C plus I sub B times RE and you can see that I sub C is 0.2 ampere times R sub C is 150 plus VCE is how much?

(Refer Slide Time: 19:01)



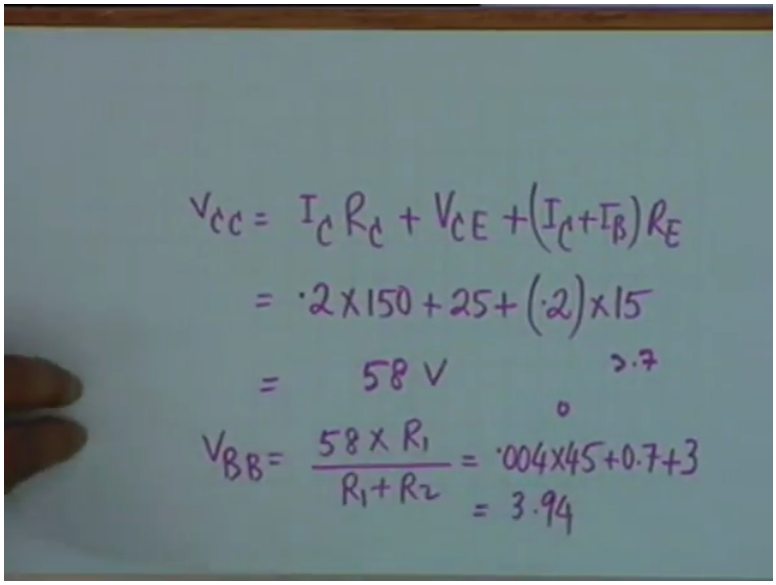
No, VCE is 25 volts.

(Refer Slide Time: 19:03)



So 25 plus I sub C plus I sub B we will take it as 0.2 multiplied by RE is 15 ohms, so how much is this? This is 58 volts.

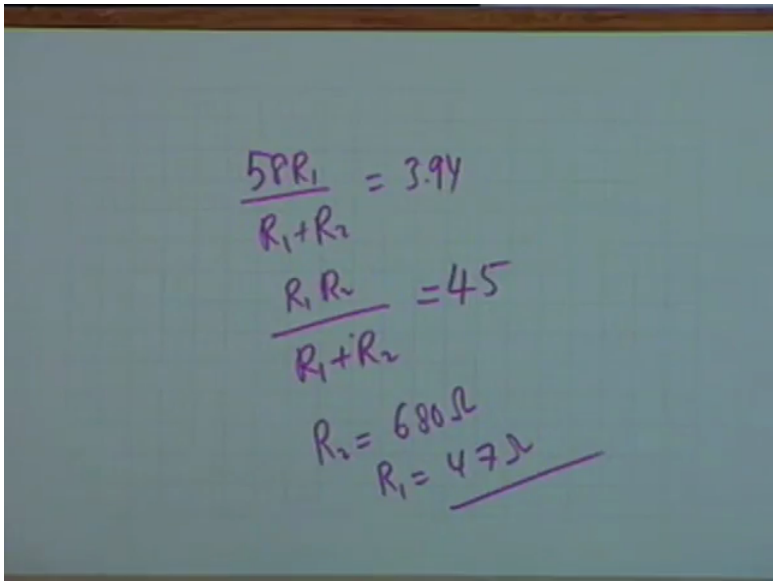
(Refer Slide Time: 19:23)



Now that is what the diagram also gave you 58 volts approximately, 58, okay. So you know VCC, now therefore VBB is equal to this is a 58 multiplied by R1 divided by R1 plus R2, you can also calculate VBB from the base circuit that is equal to IB, what is IB? 4 milliampere, so 0.004, 4 milliampere is, is it okay 0.004 multiplied by RB, we have already chosen RB that is 45 ohms IB RB as VDE is 0.7 plus VE, how much was VE? 3 volts.

And this you can see, how much is this? 3.887, yes, okay. Actually it should be, we ignored that I sub B here, if we had ignored, if we had not ignored it would come to about 3.94 or say whatever it comes there is a figure, alright?

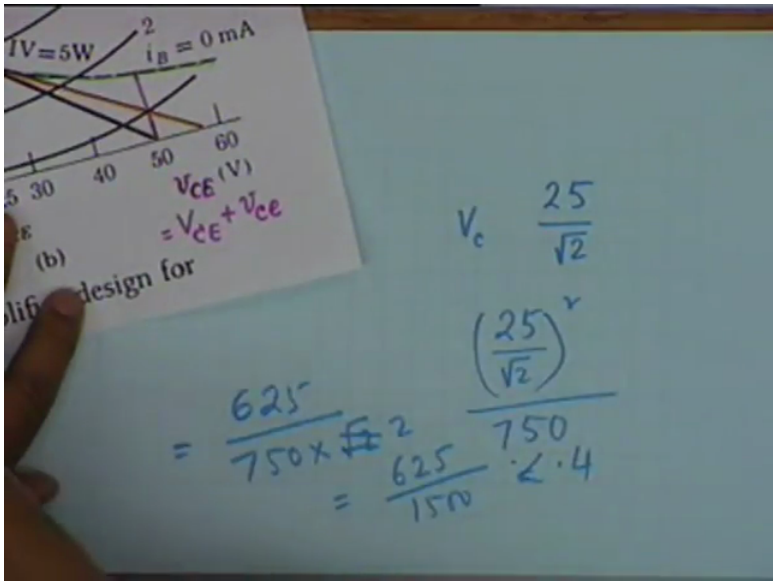
(Refer Slide Time: 21:10)



So we know VBB and therefore we have 2 equations, one is 58 R1 divided by R1 result to equal to 3.94 and the other is R1 R2 divided by R1 plus R2 is equal to how much was this? 45, so all you have to do is divide this equation by this then you get R2 and if you know R2 you can get R1. The final values are R2 equal to 680 ohms and R1 equal to 47 ohms this illustrate what an electrical engineer does when he is required to design a power amplifier?

The point is how do you choose the transistor? One supposes, somebody says well, I want a 5 watt power amplifier, okay. Then a power amplifier which can drive 5 watts into a 750, how much power in this case we get to the load? Do you get 5 watts? Load power, yes what is the load power? How do you calculate the load power?

(Refer Slide Time: 22:37)



Let us look at this again, the swing the voltage swing in 750 ohms would be approximately 25 volts, alright. So 25 volts, what is the root mean square value? This is the peak value divided by root 2, this is V let us say small c that is the RMS value of the voltage across the load and what is the power been? Power is Vc square divided by RL, what is RL? 750 ohms.

So how much is this 625 divided by 750, multiplied by 2. You see how true our this circuit is? It is approximately it is even less then less than 0.4 watt. 5 watts is being dissipated in the transistor and by driving the transistor phase limit we can get on the (()) (23:41). So it is very efficient, is not it right? It is not even 10 percent from 5 watt we are 5 watt we are wasting and we are getting 0.4, alright.

The maximum that can be obtained under this condition the maximum efficiency this will be a tutorial problem which we will work it out in the tutorial class but maximum efficiency you take it from me is 25 percent, for such operations the maximum efficiency of a power amplifier is only 25 percent, so if you want 5 watt into the load the transistor that you will select be able to dissipate a minimum of 20 watts and you see we could get only 10 percent or so efficiency here.

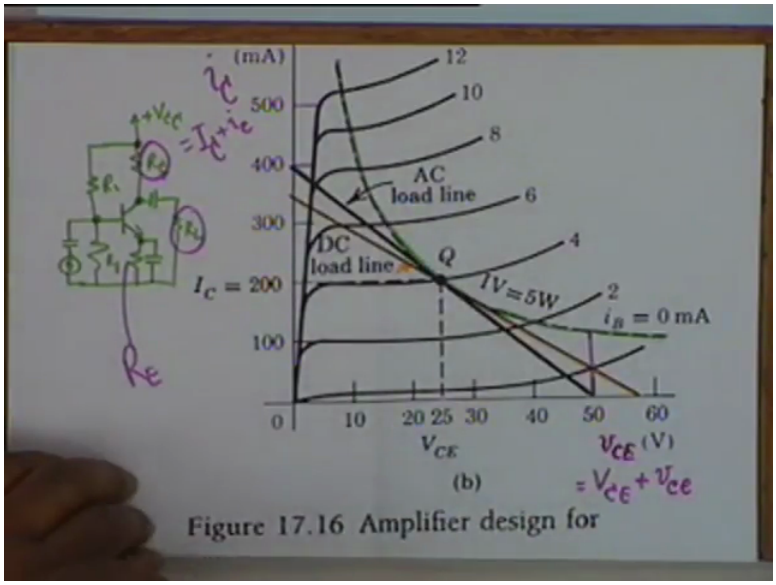
And therefore to be on the safe side in order not to burn the transistor out, you choose a transistor which is not 20 but let say 30 watts or 40 watts transistor then you are safe, alright. The stereo amplifier will not burn out in the middle of your music or in the middle of your speech, alright. So that is where you start from, after you choose the transistor the main consideration for the transistor is how much power it can dissipate?

Depending on what power you want in the load? After you do that then you take the characteristics as specified by the manufacturer and go ahead and design the circuit with various resistances and so on. Now you got a resistance like 15 ohms, fortunately 15 ohms is manufactured by the manufacturers but suppose you have 45, 45 is not manufacturer the closes resistance is 47.

There are some preferred values of resistors, preferred value of capacitors that are manufactured, so you will have to go to the stores take let say if you want 1k resistance, 1K is manufacturer but who knows 1K, the 1k that you take may have 01 percent tolerance or 20 percent tolerance. So you take a bill from the storekeeper and go on measuring and you match the requirement.

You take a dozen maybe one of them will fit your description. So there are compromises all throughout the design process is such, what you do analytically is not exactly reflected in the laboratory because there are limitations, there are tolerances and if you achieve let us say if the specification is 5 watts and if you achieve 4.9 watt then you see I have done a good job you might also get 5.1 then you are happy, alright. Because the errors might accumulate in the maybe favourable direction and may give you a power more than what you want, alright.

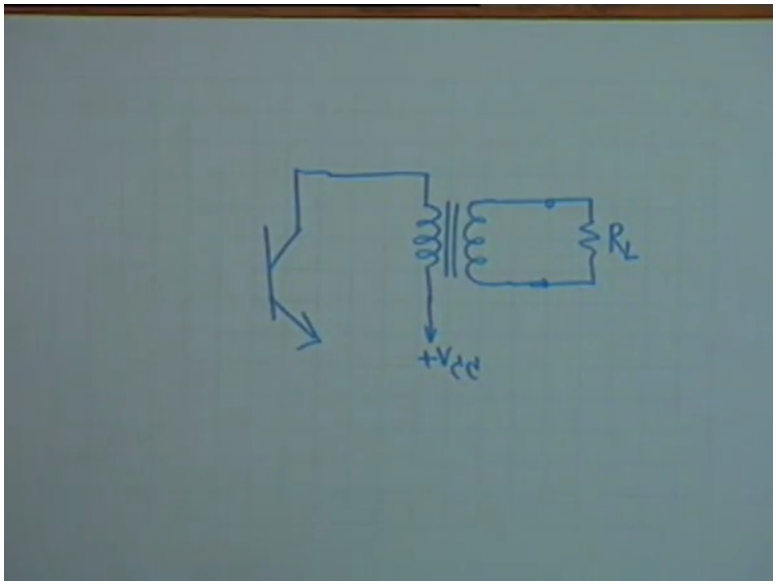
(Refer Slide Time: 26:44)



Now in the circuit that we have discussed so far one of the reasons that you do get so poor efficiency is because some power is wasted in RC. You said you do not want power to be wasted in RC, you want all power to go to RL and therefore if you had a means of transferring power to the resistive load without any intermediate resistance than it would have been very nice you would be able to save some power.

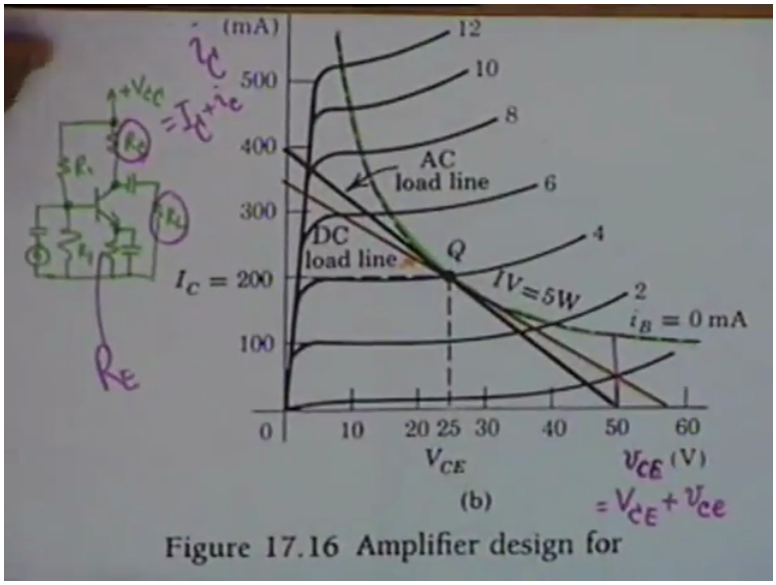
You would be able to increase the efficiency and this is how the (()) (27:07) by transformer coupled power amplifier. If you couple the load to the transistor through a transformer that derive 3 benefits but before looking at the benefits let us look at this circuit.

(Refer Slide Time: 27:30)



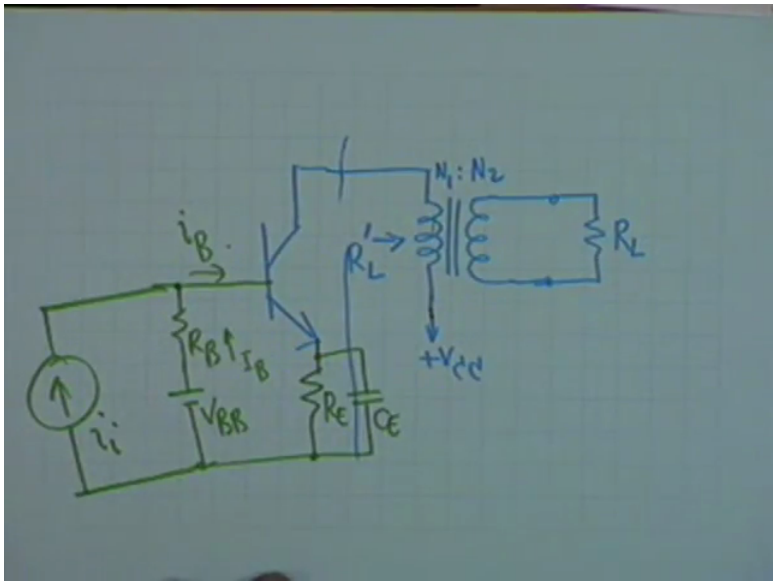
The circuit is like this, instead of an RC what you have is a transformer primary in the collector circuit, this goes to plus VCC there is no RC, the collector goes straight to the primary coil of the transformer, the transformer has a secondary and it is today secondary that the load is connected, the load RL is connected to the secondary. So there is no intermediate resistance through which the load is connected.

(Refer Slide Time: 28:11)



In the previous circuit there was a resistance R sub C, why was R sub C needed? Could we make R sub C equal to 0? Just a minute, could we make this R sub C equal to 0? Could we? If we had made R sub C equal to 0 what would be the effective AC load? 0, RL parallel short-circuit is a short-circuit. So there was no way I could get rid of R sub C.

(Refer Slide Time: 28:36)



But in this circuit when the circuit that you see now there is no R sub C, there is a small amount of resistance here in the primary of the transformer but that will be several ohms and you can ignore. We shall assume that this transform of is a perfect transformer that means it has no resistance using the primary or secondary a few ohms should be tolerated, alright. Very small dissipation but otherwise you can assume it to be ideal.

So the load power is transferred to the load without getting wasted in the while media, the wire media is a transformer, alright. Not only that it has another benefit that for what? That capacitor that we have to use in the previous circuit is no longer required for the price that you pay is a heavier block. Transformer is a larger block and a heavier block but it avoids the use of a capacitor it isolates the load from the DC, alright.

It isolates the load from the DC, why? Because it is only varying currents that are transformed, a steady current is not transformed, alright. So first was no dissipation in RC, second is isolation of DC and the third and the most important is that a transformer allows a matching maximum power transfer tables says that the load should be complex conjugate of the source resistance, alright.

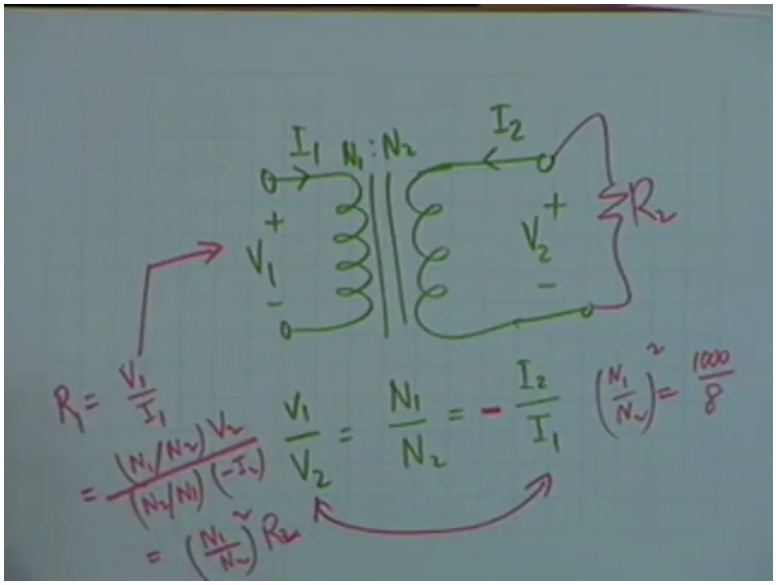
So with this transformer while varying the trance ratio N1 to N2, you can so design that the effective load that you see in the primary RL prime may be the maximum maybe the condition for maximum power transfer that is it may be equal to if you take the Tribune an equivalent it may be equal to the Tribune an equivalent resistance looking to back at the transistor then you are sure that maximum power is being transferred to the load, alright.

So these are the 3 basic benefits, now if I complete the circuit I must get an RE here I must have an RE and I must have CE in parallel which is a bypass and in addition I must have the usual R1 R2 combination, usual R1 R2 combination. Now where from shall you take the R1 and R2? From here or from here? From VCC direction, why? Pardon me. No. Yes, if we take it from here then we include some resistance here dividing resistance, we do not want to do that.

So we connect directly from here and I shall simply show the equivalent circuit, the equivalent circuit is that you have an RB and VBB which is equal to VCC R1 divided by R1plus R2 and RB is a parallel combination of R1 and R2 and this signal, let me show this as a signal as a current source, the input signal is here i sub i. This current is I sub B the DC current and this is the total current small i sub capital B, this is the total circuit, well, not quite because I have shown here the equivalent (()) (32:12) circuit. I should have drawn R1 from here to the base and R2 to ground instead of that I have shown a (()) (32:20) equivalent circuit.

Now how do I analyze this circuit and how do I design this circuit? The transformer coupling that is one thing which I said R3 and as you shall see the maximum theoretical efficiency of this is 50 percent that means if you take a 5 watt transistor you can deliver in theory 2.5 watts to the load, alright.

(Refer Slide Time: 33:00)



We will see this by analysis, now if you recall second theory the transformer the perfect transformer has the properties that if V1 now I am showing (()) (33:09), V1 maybe voltage here the current is I1 and omitting the bars and this is I2 and this is V2 the trans ratio is N1 to N2 then you know that V1 by V2 is equal to the ratio of the turns that is N1to N2 and it is also equal to the ratio of the currents I2 to I1, is that correct?

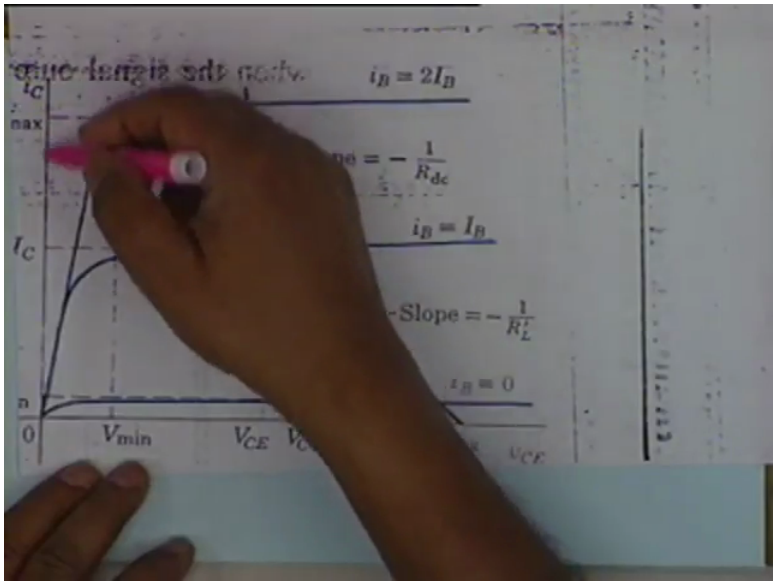
No, there is a big mistake in this there is a minus sign here, why is a minus sign required? Because the total power absorbed by the transformer is 0, so V1 I1 plus V2 I2 should be equal to and this is what this is how this relation is obtained V1 I1 shall be equal to minus V2 I2 and there is a negative sign here. Not only that if you recall if there is a resistance R2 here connected then what is effective resistance R1?

It is simply, it is V1by I1, correct? And V1 from this relation is N1 by N2 times V2 derived by I1, I1 is minus I2 N2 by N1 which is equal to N1 by N2 whole square multiplied by V2 by minus I2 is simply R2 and then this is how the transformation is affected that is if you take this resistance if you terminate the secondary in R2 then what you see in the primary is called reflected resistance, this resistance reflects itself to be primary with a factor of N1 by N2 whole square this is the trans ratio whole square.

For example if you require for maximum power transfer at 1K resistance and your speaker is 8 ohms then obviously N1 by N2 square should be equal to 1 K that is 1000 divided by 8, so you can choose your trans ratio property, alright. And this can be (()) (35:49) very easily with course available in the in the laboratory. So this is the basic relationship of a transformer

which you should utilize and to illustrate the design of a typical circuit we will take a very simple case, is this clear? Yes it is.

(Refer Slide Time: 36:21)



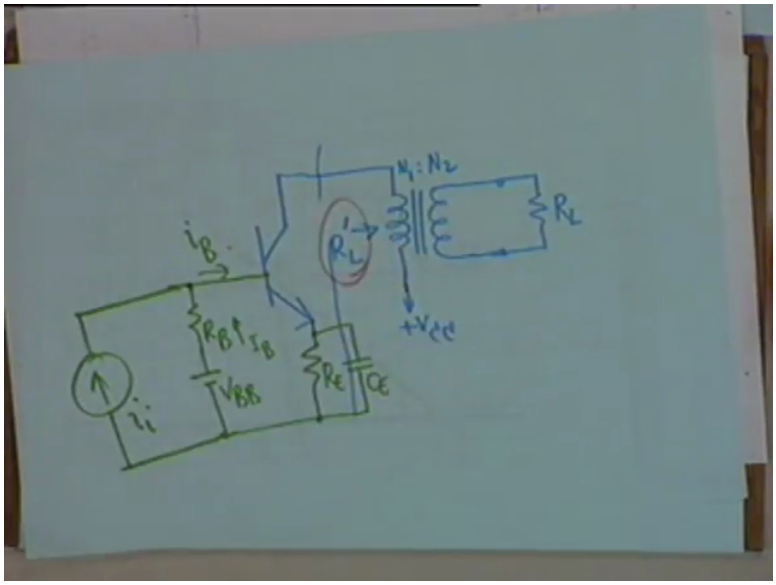
So we will take a typical characteristic while you see this is also a plotter I sub C versus VCE, alright. And there are several things now which one has to be very careful about you see in the transformer couple amplifier there is no RC the DC load therefore is simply RE plus this small winding resistance of the transformer small means (()) (36:48) power transistor you have seen in the previous case that RE is of the order of 15 ohms you do not want a large RE.

Because an RE will itself waste power, is not it right? When a transformer couple amplifier RE should also be a small quantity. In other words you will not you will not choose VE equal to if the power supply is let say 12 volts you will not choose VE equal to 3 volts, you will choose VE equal to 1 volt or maybe 0.5 volt because what matters is RB, RB should be beta min RE divided by 10, alright. So that gets easier flexibility.

In other words DC load line is almost vertical line, is a point clear? DC load line is this green line, there is a slight slope here because of its small resistance but actually in practice there is very little difference between VCC and VCE it is almost a vertical line, is the point clear? If the transformer was ideal and there was no RE then the line should have been a perfect straight line.

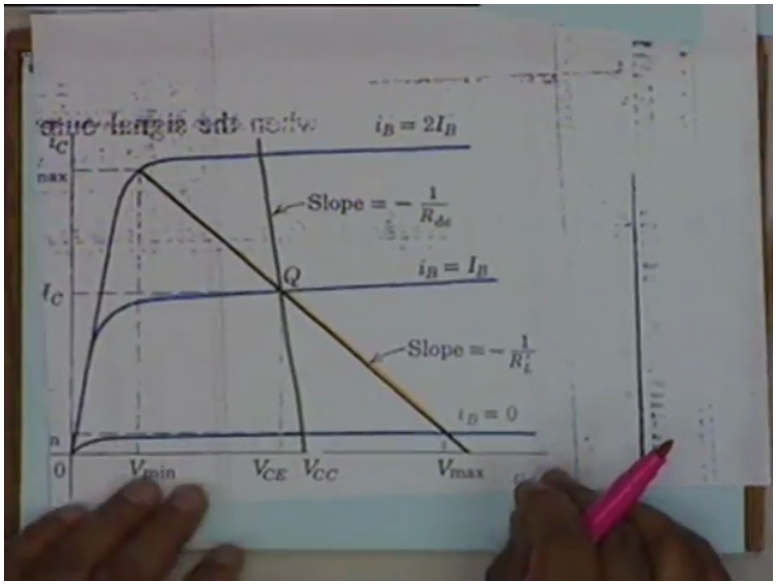
It is slightly inclined because of RE, so the slope is minus 1 by RBC, alright. And the Q point therefore it is very easy to find the Q point, what you do is you find the maximum dissipation hyperbola and drop a vertical line at VCC wherever it cuts is approximately the Q point, if you want to be (()) (38:23) then you shift the Q point you actually draw the DC load line and find out where the Q point lies but it is clear that VCE and VCC are very close to each other, is this point clear? Then what should be maximum swing?

(Refer Slide Time: 39:01)



Approximately twice VCC, alright. And the slope the AC load line, AC load line shall now be whatever resistance is sent by the primary, is load line shall be determined by RL prime, alright. AC load line slope shall be minus 1 by RL prime because RE is approximately 0 winding resistance is approximately 0.

(Refer Slide Time: 39:20)



And then on these characteristics you draw the AC load line. Well, is load line obviously the Q point is fixed, if the Q point is determined when you know its vertical intercept is approximately VCE therefore you go another VCE distance, alright and then you find out the slope as I did in the previous case.

In the previous case we found this out to be another 25 ohms, you remember how we did that, alright? So you know this slope minus 1 by RL prime. Now you have to be careful, once we have done this what I have shown here is Q point is at small iB into the capital I sub capital B and we said the swing would be limited between 0 and twice IB, obviously we cannot exceed that.

This is your Q point you go IB on this side then you must come down IB on the other side also for no distortion, alright. You must apply allow equal swings the point however is that you cannot exceed this point you cannot go down below this, why? Because this is the curve iB equal to 0 and you cannot go beyond this point, why? Because this is a saturation region.

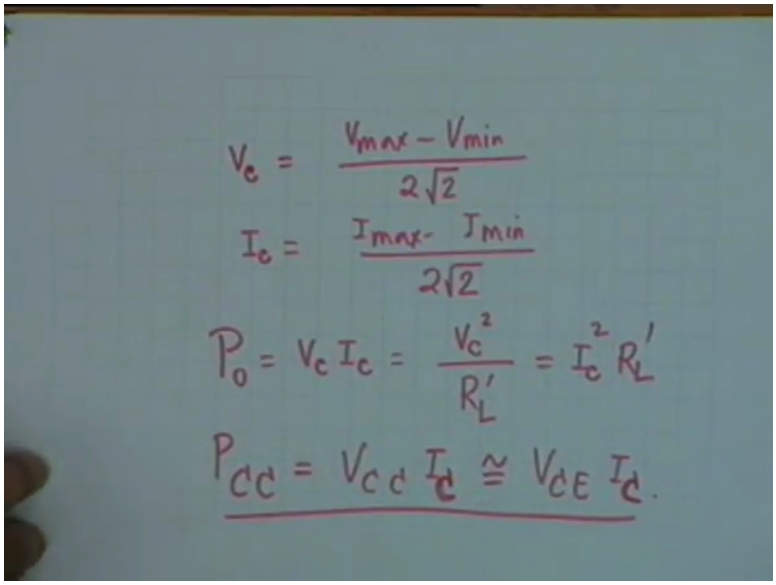
This is a highly nonlinear region and we shall not permit the transistor to go beyond this. So there is a Vmin there is a minimum value of Vmin we cannot go exactly to 0 and there is a V-max, V-max is not equal to twice VCE it's like less than twice VCE and Vmin is slightly greater than 0, okay. Whatever the current swings, at the Q point the current the current is I sub C.

Now the maximum that you can go is this me this point when you call this i max the minimum that can go is this much which is I min, alright. Capital I min, I min is not equal to 0, these are facts of life and 1 has to live with them, alright. Now what guarantees that the swing is equal to the swing? No, there is no guarantee, is not that right?

This distance may not be equal to this distance, okay. So you will have to choose the smaller of the 2, is that clear? Similarly VCE, VCC I am sorry VCE minus Vmin may not be equal to V-max minus VCE you will have to choose the smaller of the 2. Got that but one thing is clear that the swing the peak to peak voltage swing between collector and emitter would be approximately V-max minus Vmin divided by 2, agree?

Similarly the peak to peak current swing shall be i MAX minus I min divided by 2 and if you would know not peak to peak, the peak value. Peak to peak is V-max minus Vmin divided by 2 is the peak value of the swing and if you know the peak value divided by square root of 2 to get the RMS current, alright.

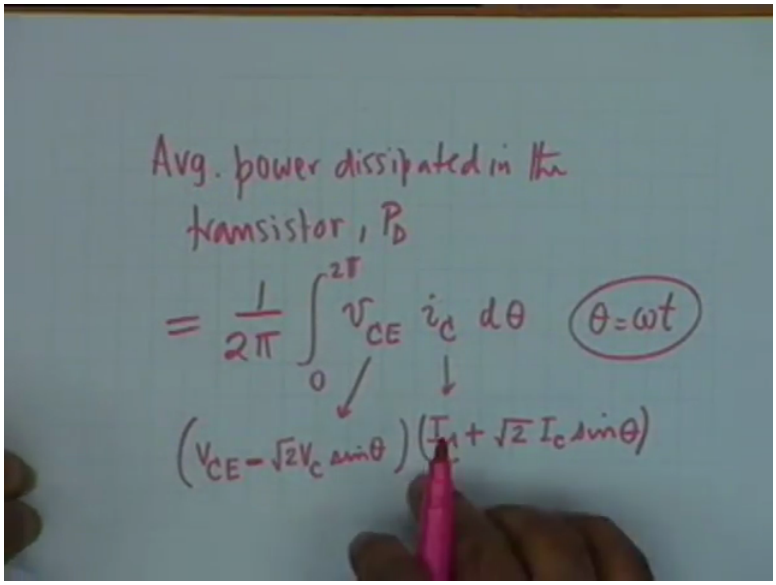
(Refer Slide Time: 43:04)



And therefore we can vary simply write the RMS value of the load voltage, the RMS value of the low AC voltage V sub c, this is small c not capital C, if it is capital C than it is the DC. Capital V sub small c is simply V-max minus Vmin divided by 2 root 2 similarly the RMS value of the load and I sub c shall be I max minus Imin divided by 2 root 2 and the power in the load shall be simply the product of the 2 that is Vc times Ic or you can also write this as Vc squared divided by what? Defective load RL prime or this will also be equal to Ic square times RL prime.

Either way any of these 3 relations will give you the power that goes into the load, alright. This is the load power, this is the AC power signal power delivered to the load, what is the power that is supplied by the source, the battery? Let us call that power is Pcc this obviously Vcc multiplied by I sub c and Vcc is approximately equal to VCE, is that correct? This C is capital, this C is capital. VCC is approximately to the VCE, why? There is no resistance in the collector, except for the small winding resistance and the editor resistance is also very small quantity. So this approximation is usually valid.

(Refer Slide Time: 45:26)



And under this condition therefore, let us find another quantity that is the average power dissipated in the transistor (()) (45:22). How much power is dissipated in the transistor? Obviously instantaneous power dissipated in the transistor is VCE a total collector to emitter voltage multiplied by i sub C, alright. This is the instantaneous value, so what we will do is, we will integrate this over 1period of this sinusoid let us say d theta where theta goes from 0 to 2pi.

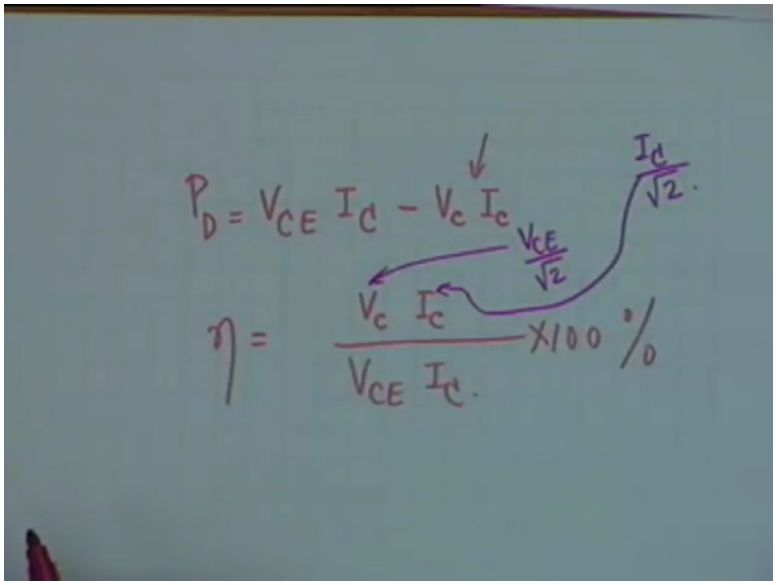
Theta is equal to Omega t and then you divide by 2pi, is that okay? Where we have assumed sinusoidal variations. Now if I assume that i sub c the total collector current is equal to the DC collector current class the AC collector current. AC collector current would be good to, not input current, the collector current the current in the collector, okay. It will be root 2 I small c the RMS value times sine of omega t which you have put equal to theta sine theta.

If I sub c is taken as this, is the point clear? The total collector current has a DC component (()) (46:57) component and an AC component. The DC component I represent that I sub capital C and the AC component is IM the maximum value which is root 2 times the RMS value we have already calculated the RMS sine theta then what should be VCE under this condition?

It would be the DC value V subscript capital CE and then, yes? Plus the AC value which is root 2 VC sine of theta, what would be the signal between 2 quantities? Why? Out of phase, yes, that is right. When the collector current increases the collector to emitter voltage

decreases and therefore this should be a minus sign. Now if you carry out this algebra and integration then the result becomes very revealing one.

(Refer Slide Time: 48:12)



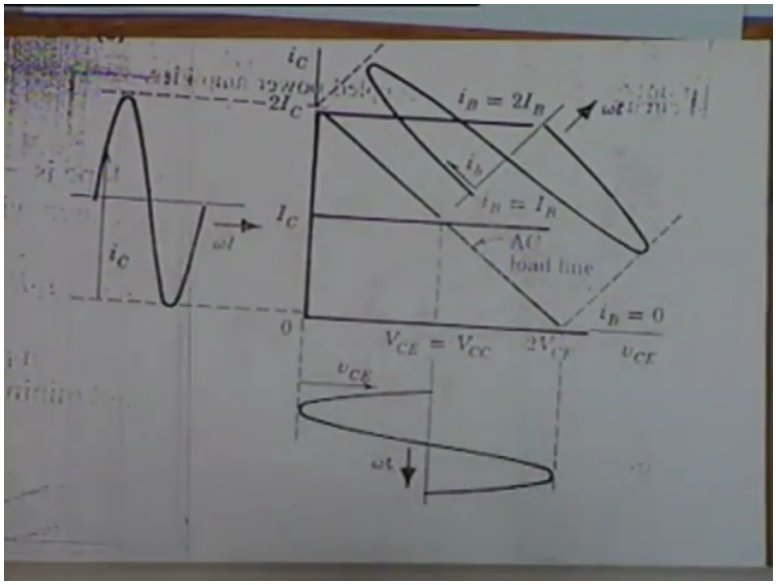
What we get is by calculation P sub D because VCE times I sub C minus Vc times Ic as simple as that and this is very revealing relationship. It should have been clear from commonsense, alright. VCE IC is the power delivered by the battery and this is the power which is transformed into signal power and it is delivered to the load. So the total power supplied with the battery minus the power supply to the load, signal power must be the power dissipated in the transistor, alright.

So and this also show something else that if you do not apply a signal, that is V sub C equal to 0 or I sub C equal 0 then obviously the power dissipation in the transistor shall be maximum, alright. So before the political leader comes you should not put your probably get the system on because it gets more and more heated, is a point clear? When there is no signal the power dissipation is maximum.

Not only that when you are delivering maximum power to the load dissipation in the transistor is minimum, alright. So it is not good to put a power amplifier on without a signal, it is only after the signal has arrived is better to put the power amplifier on. Otherwise unnecessarily you waste heat. Now comes the question of efficiency, well efficiency Eta is simply equal to power to the load, signal power to reload V sub C I sub C divided by VCE I sub C, alright. And this usually is multiplied by 100 and express the percentage.

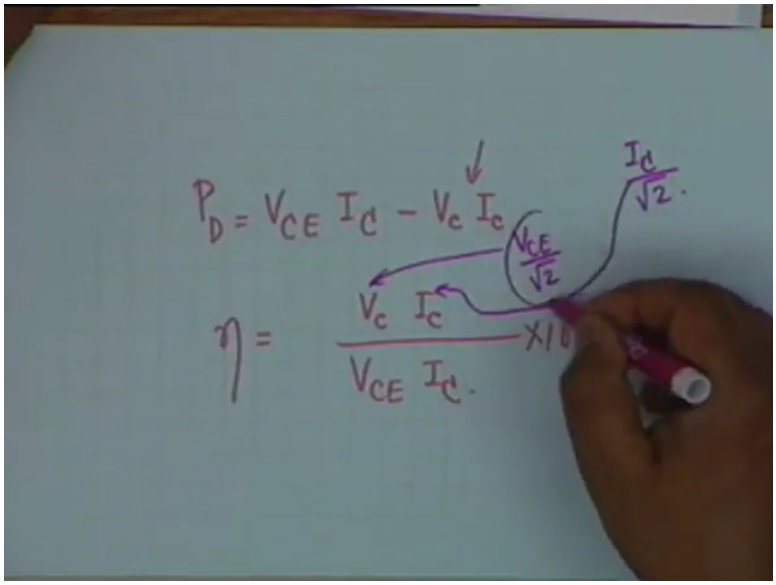
What would now be the maximum possible efficiency? What is the maximum possible VC? Where would be in squared value? What is the maximum possible VC? If that takes time, pardon me, Load 2 times, how would is it related to VCE? Tell me, that is correct. The peak value is VCE, so it is VCE by root 2 then what is I sub C, maximum possible value?

(Refer Slide Time: 51:03)



Capital I sub C divided by Root 2 if conditions are ideal that means if conditions are like this that is if we can approximate the transistor characteristic by straight lines, okay. The saturation is a vertical line iB equal to 0 line is the horizontal line and then in between there was no nonlinearities there perfectly straight this is the most ideal condition. So then VCE would be equal to VCC and the swing would be after to VCE. The current would go from 0 to twice ic and this is the most ideal condition.

(Refer Slide Time: 51:33)



And under this ideal condition this is what should be valid that is we say would be VCE by root 2 and Ic would be Ic by root 2 and you can see that this is equal to, this is the ideal efficiency of the transformer coupled amplifier. The usual values that we get in practice surely should be less than 50 but it is a very encouraging thing that 40-45 percent of efficiency can be obtained even by the most negligent designer which means that even if you have lot of tolerances and the transistor, in the design, alright.

If you are not very careful even then 40 to 45 percent (()) (52:21) power of the, transformer coupling is very easily obtained but the price that you be literally is the price of the transformer. Transformer is much more costly as compared to a capacitor and a resistor. A resistor may be a rupee, capacitor may be 5 rupees, a good capacitor 5 to 10 rupees but transformer may be about 80 to 90 rupees, a good transformer, value, you have to pay a price to get a good performance.

Next time we shall be taking an example and go to other types of operations of a transistor.