**Fundamentals of Power Electronics**
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**Lecture - 14**
**Simulation setup for NgSpice and gEDA schematic capture**

In this video capsule we shall take a walk through the simulation process. We shall draw a schematic and we will take the full bridge rectifier capacitor filter circuit as an example, generate the netlist and use n g spice to simulate it see the waveform, plot the waveforms and try to get some insight of the circuit. One thing that you have got to understand is that simulation is for mature people. The values of the simulation or the results of the simulation is as good as the models that we put in.

So, remember that many a times, we will put kind of idealized model for the diodes or transistors or various components, and expect the simulation to do waveforms which you would get on the oscilloscope of a real system. However, there will be considerable difference because there are many non-idealities and many of the uncertainties which we will not be taking care in the simulation.

Keep in mind that simulation used to give you good insight of the concept of operation of the system. It can be used for design the rating of the various components, but the real test is when you put them into the hardware physical hardware and realize the actual waveforms and results on the real hardware. So, use the [see/simulation] simulation and simulation results with a pinch of salt and use it for understanding and design purposes. So, with this kind of a limitation, you try to go ahead with the simulation.

So, let us now begin the simulation work using gEDA for generating the schematics and n g spice for simulating. Let us begin the simulation process by opening the gEDA schematic. Last time we had used the terminal to open, but we could also go into the show applications menu there is the gEDA schematic startup, click icon, click on that one you will have gEDA open up. We have a light background gEDA as we have set it up last time. Use the mouse wheel to zoom in and out dynamically. So, first let us save it as a file that we can name it as a rectifier dot schematic. So, what we can do is go into file, we will do a save as I have this DCDC here. I have cleaned up DCDC, there is nothing else we can name it as rectifier dot s c h.

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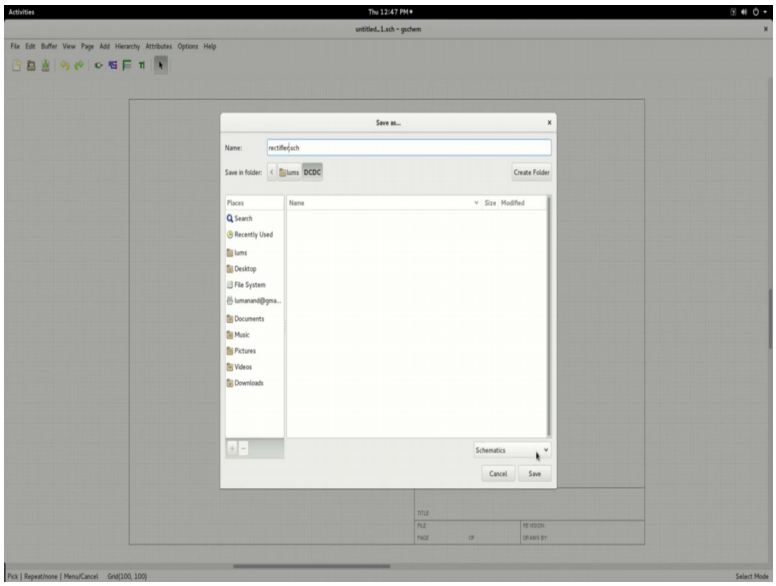

So, it will be located in that place.

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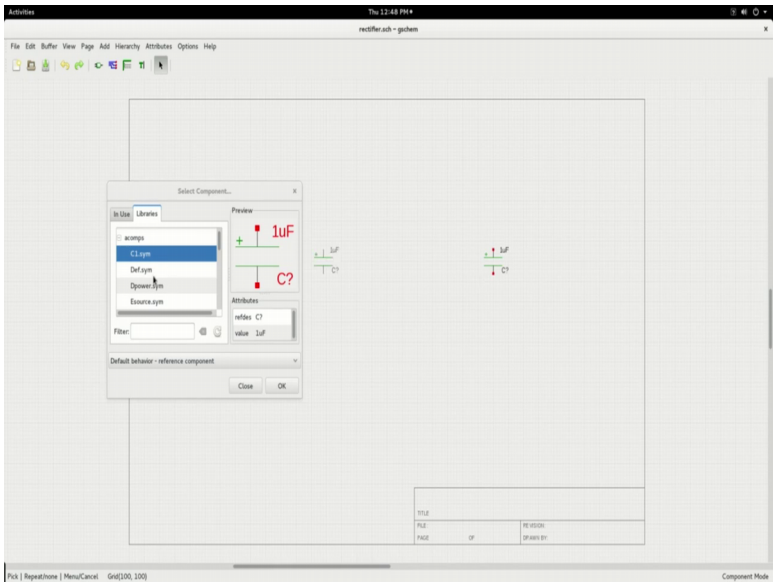

Next we go to the components. And try to draw the components from the libraries. So, first let us go and draw the circuit components which is the diodes, the sources and the capacitors load. The acomps folder library which we had installed, yes in the last session contains the generic components; you can use it for most of the simulation because there are generic models. Let us pick the capacitance we need that. We need a diode, a power diode, we need four of them.

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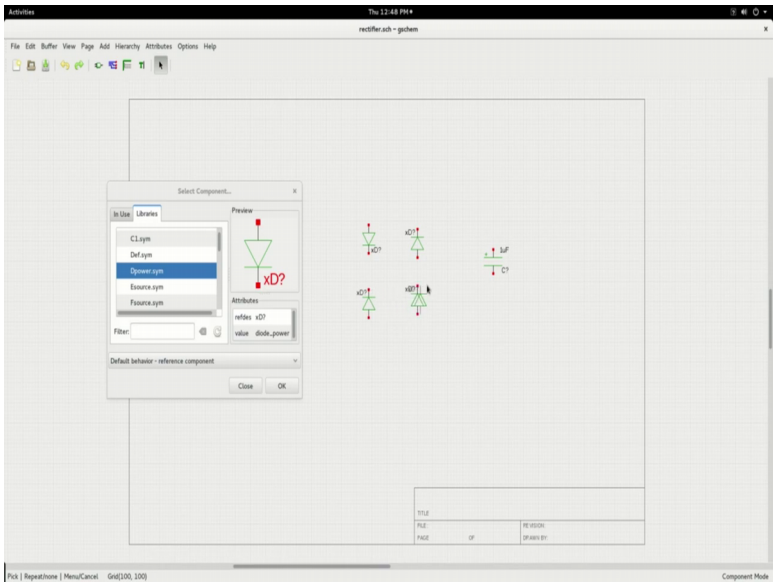

So, let us install 4, I am using e r to rotate the devices.

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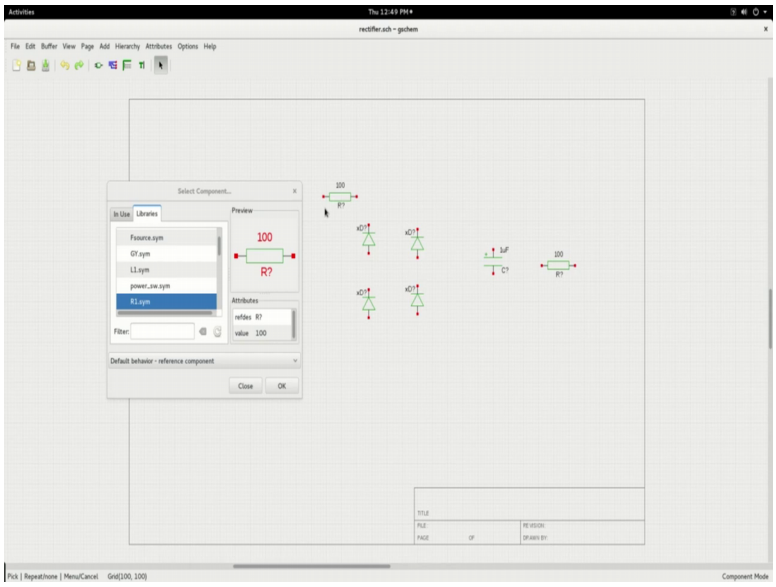

I will rotate this device too. Then we will need load resistance. We will put one resistance here; I would also need another resistance to put act as track resistance, otherwise you will land up in convergence problems. So, I will place that here we will see how we will connect it into the circuit. Then we need to take draw the source. So, the source you can take from the spice simulation elements library.

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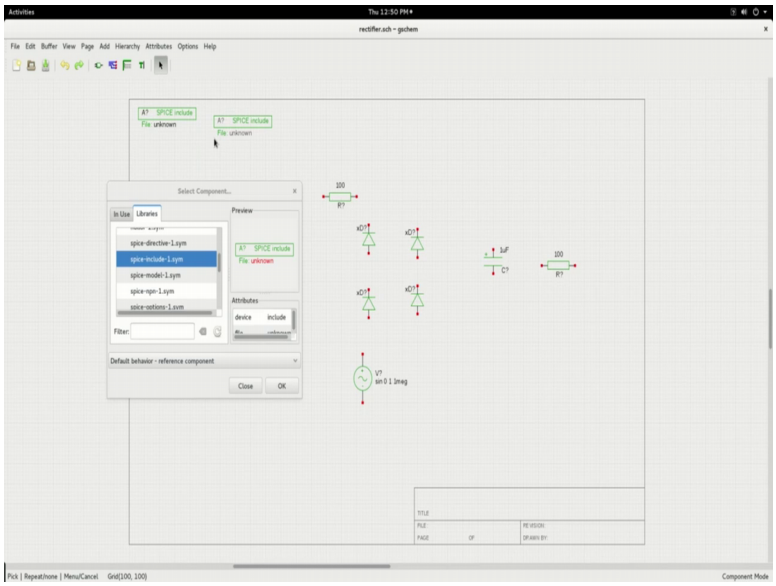

The source is a sign source; we will pick a sign source. We also need to pick one more item here, there is spice include directory. We need to include a file which contains the library of models custom model that we would be creating. So, we will give a pointer to the file that that would be our library, our custom library.

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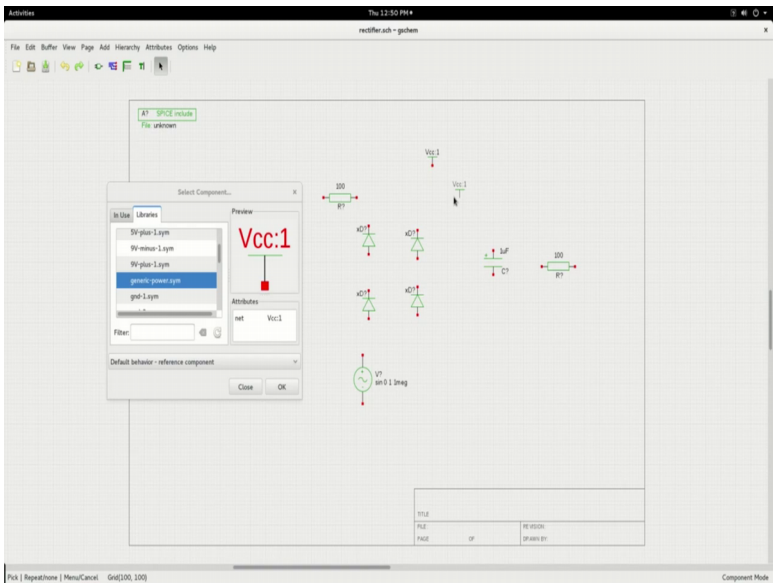


Next we need to take in from the power rails library. The generic this is a generic marking symbol which can pick of the potentials of any points or circuits.

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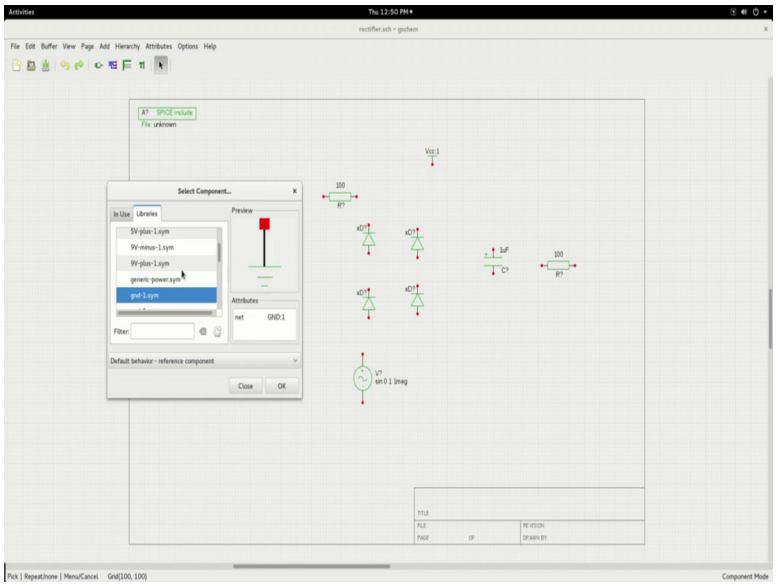


We will keep on there, we need a ground symbol. This is important without the ground single spice will not work. So, I think we have most of them in place. So, let us position these elements. So, let me put the source here. Let me have a series impedance. This would be a very small impedance. Let us position the diodes something in the form of (Refer Time: 07:04) bridge nature just position them, and then you can adjust it later on like this, there were more diode.

Then we can have the capacitance position like this. I will rotate this load resistor and position it like this here ok. This we will leave it for now. Now, let us draw the wires the wires can be drawn using this ad nets. So, click on that now you are in the ad net more, you will see that it searches and links to this net.

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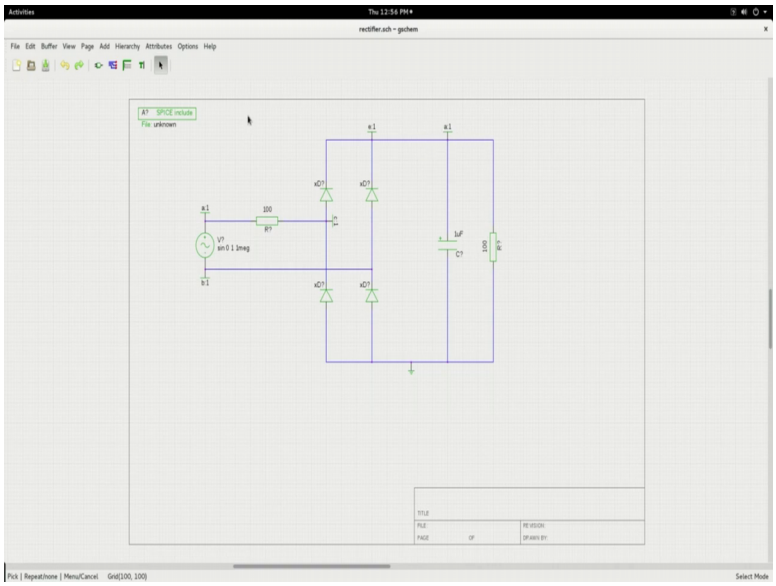

I will start putting the wires click right click. Now, now will go here, click, click, right click, click, right click, click , click, click, click, right click and completing the wiring by right clicking click, click, right click, click, right click and so on you make the connection. You make the connection for the diodes too. The diode is a sub circuit model that is why we have an x mark, x at the beginning all sub circuits will have x at the beginning.

Then the source is connected to the center portion of the bridge. And we have the circuit in place change over the cursor. Now, the ground we could probably see ground is a virtual concept. It is just a reference or the zero node with respect to which the voltages are measured. If we keep the ground here, then when you measure this node, you will get directly to output voltage. We give the ground here, then you will have to get the output voltage will have to take voltage of this minus the voltage of this node ok, that is something which you already know circuit analysis.

Now, let us place these labels here, placing these labels are important because when you run the simulation in spice the netlist is generated according to the labels that you would provide. If you do not provide the labels, then it will assign some numbers. And then it will be difficult for you to keep track of the circuit node points. If you consciously assign labels, then you will be able to get more insight, analyze and know the understand the netlist is much better.

So, let me call this as node a and I will copy this paste it, I will rotate it, and I will call this node b. By this what I have done, I have given a conscious label to this node. Now, when I want to refer to the input source I will say V a minus V b which will give me the value of the result of that waveform. Then we could give a node number here and let us say we call this as, and we could give a node for this point. They call this as e; we will call this as c. We, we can give one more node. Here I would like to place a tracking buttons here to introduce a non ideality later on. So for now I will just not give this label, I will give this I will remove this label and denote this label as o, so that we know it is an output label.

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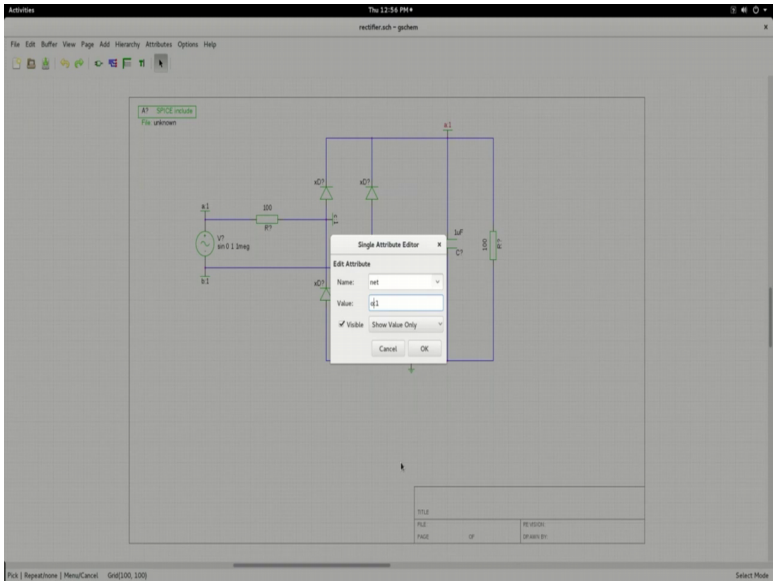


So, we have the labels; we have the ground; we have the components on place; we have wired it; we have to give the component names. So, you double click on those.

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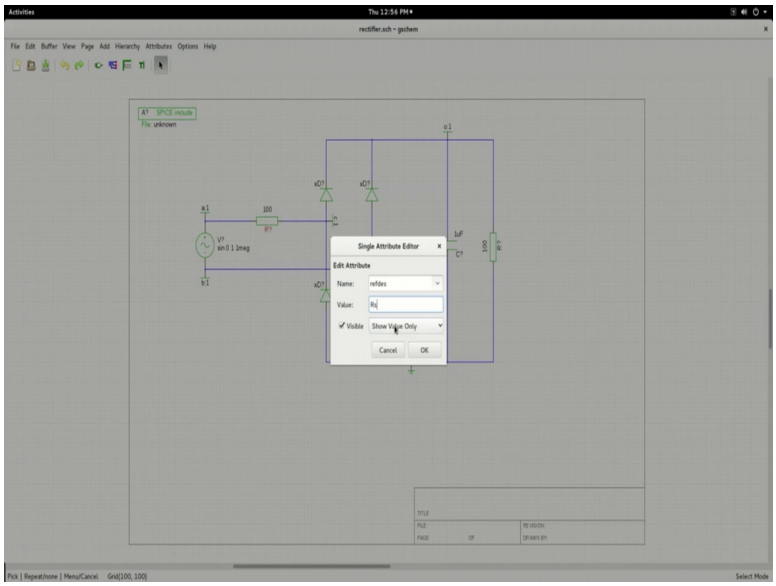


You will call this as R s series resistance. And it should have a value. And let us not give 100 Ohms; it is too much of a series resistance a 0.1 ohm, the reasonable value to take care of the tracking impedance.

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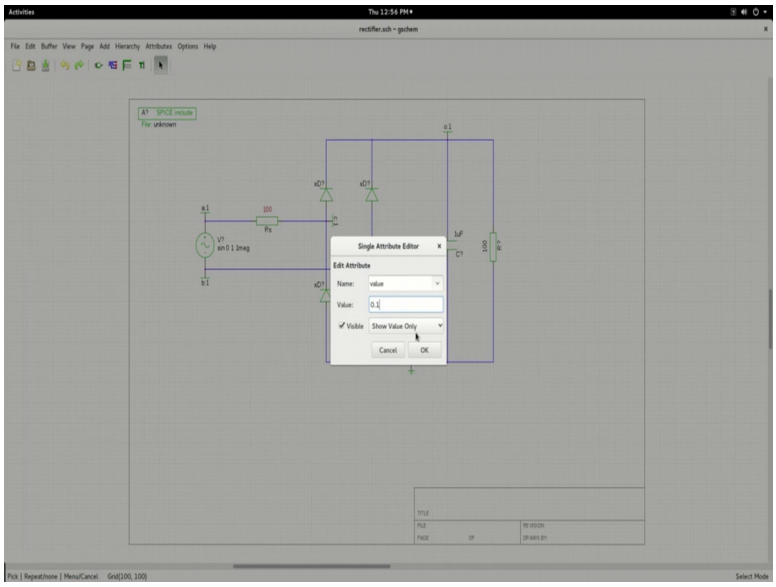


We will we will come to the source later we will give names for this diodes x D 1.

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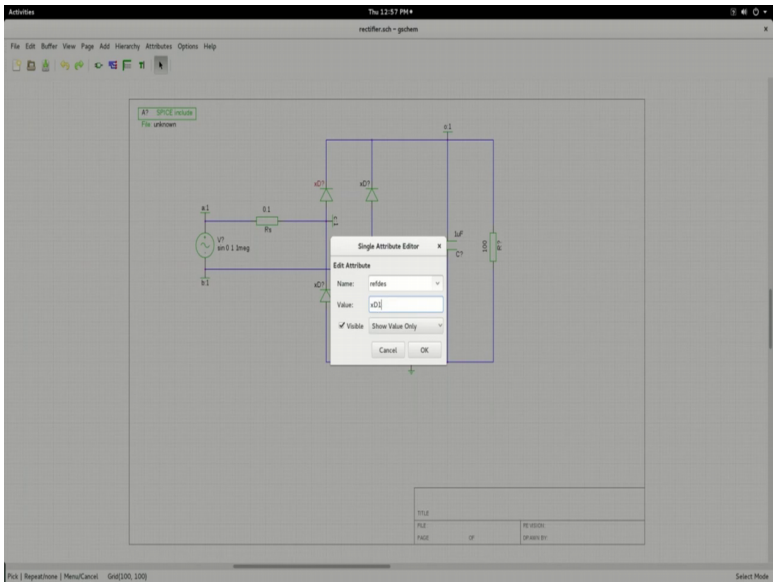


We will call that D 1; will call this D 2.

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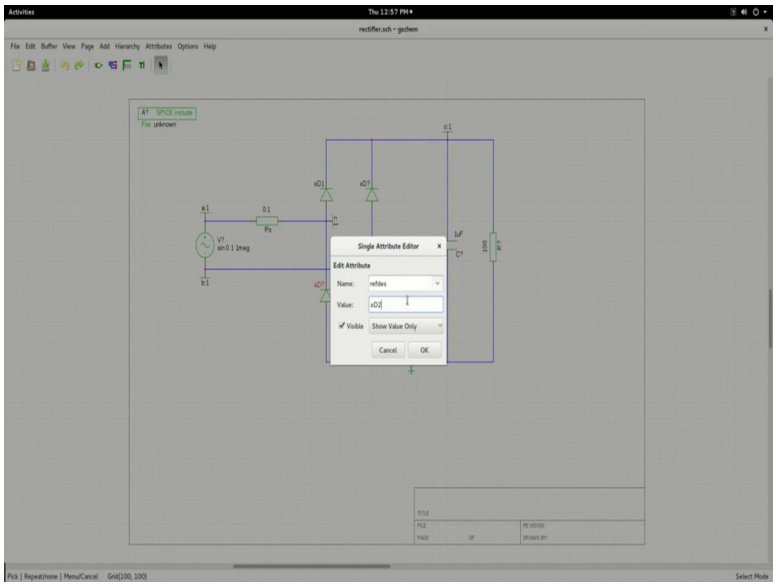


D 4.

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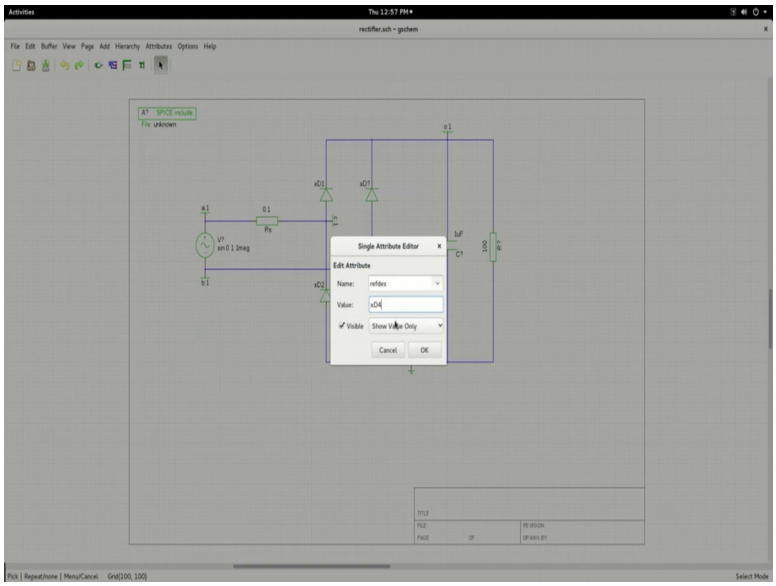


D 3.

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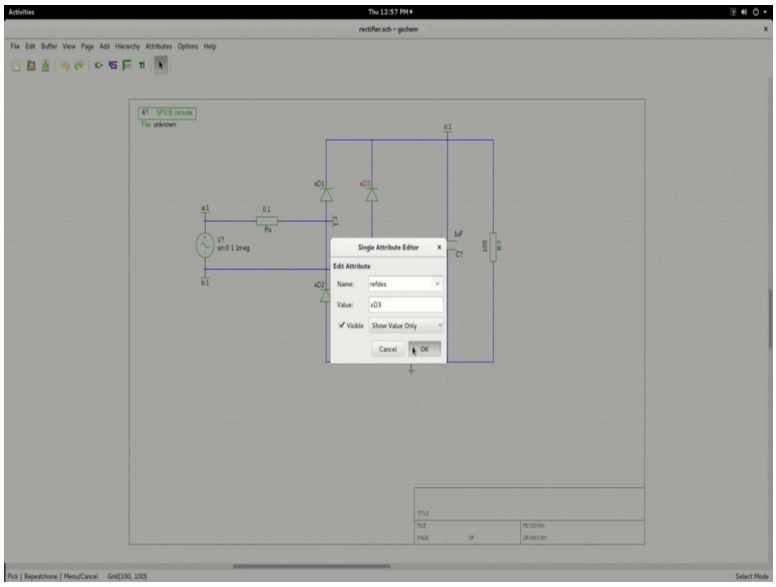


And the diodes are labeled. Then after that let us label this capacitance, we would call it a filter capacitance C f.

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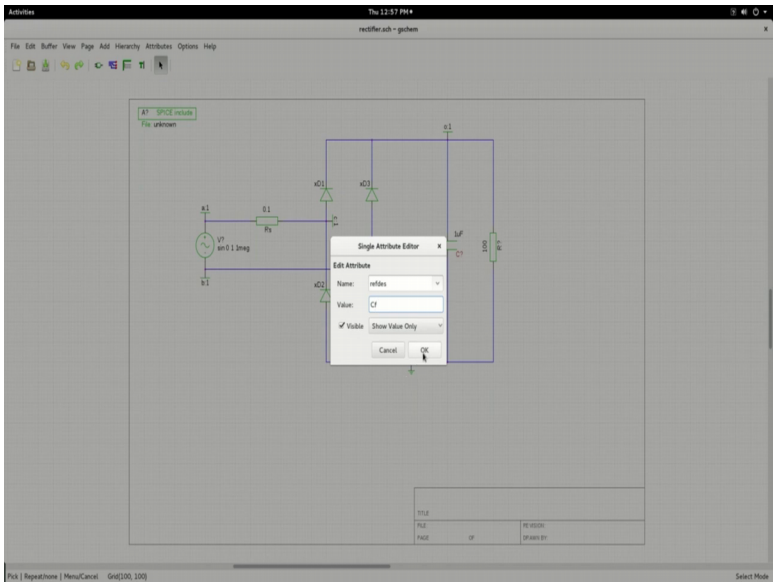


We will call this as load resistance I will call it as r r naught. So, we will give some value, we would keep this kept around 25 Ohms.

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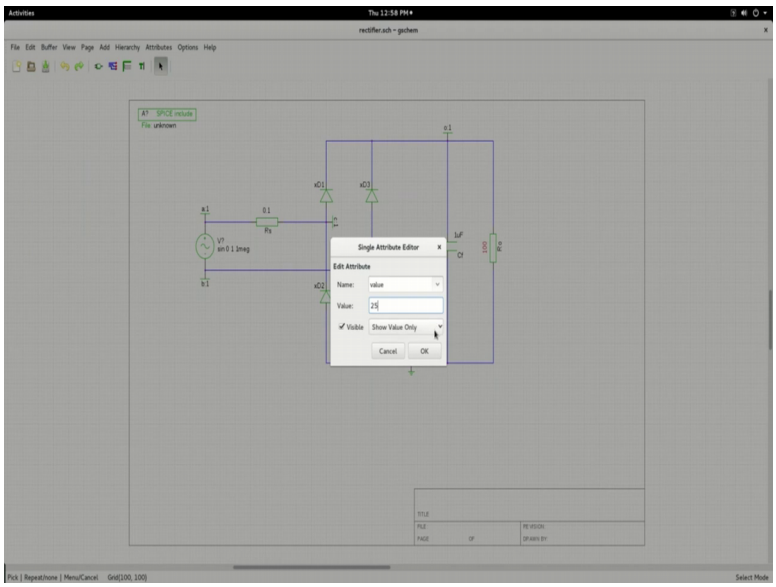


So, I that would see some amount of current they will put 1000 micro farad capacitance.

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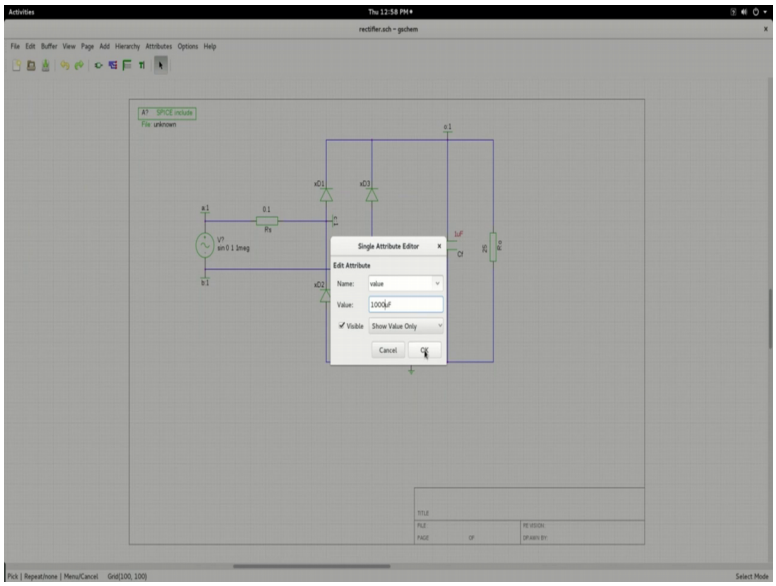


Like what we saw yesterday the capacitance value. And now the source we need to give, some value let us first give it the name V in.

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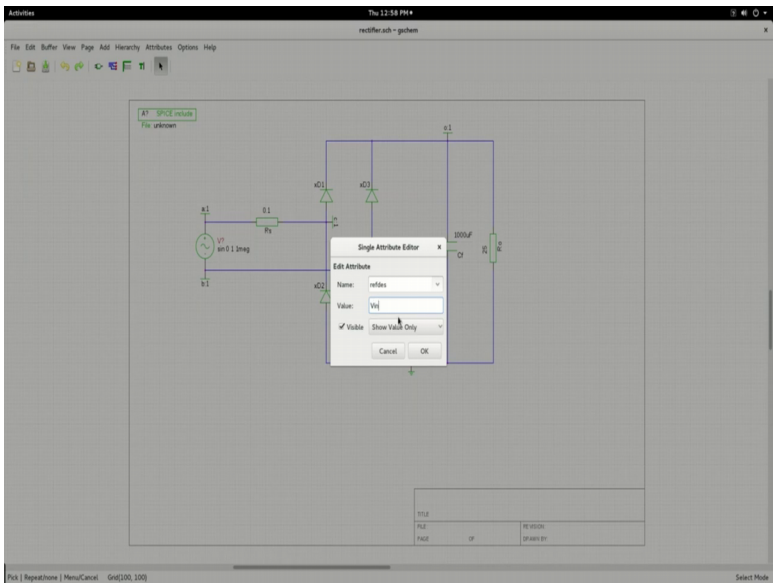


So, we have the name V in. And we need to provide the parameter for the sign attribute.

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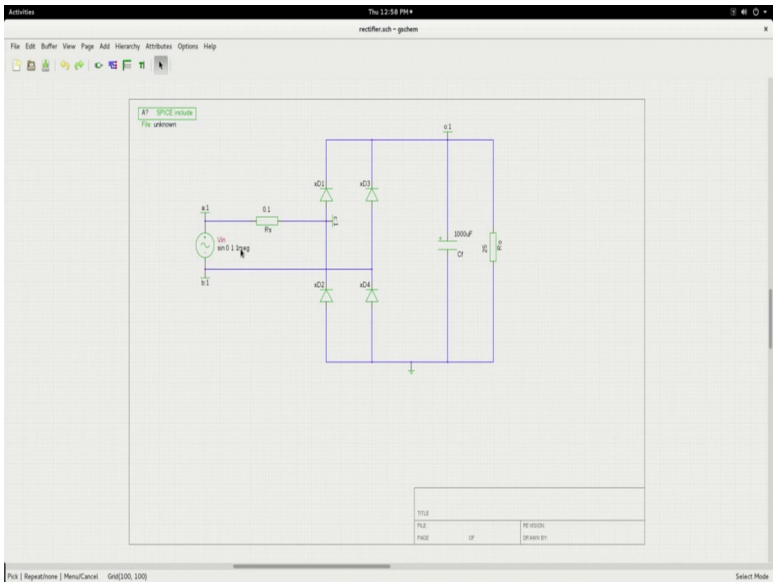

So, here we will have to give the sign wave parameters. When in doubt you can always refer to the manual, I had recommended in the last session that it is good practice to download the n g spice manual and keep it by your side. Just to look at the parameters of the sign, now let me go to the manual.

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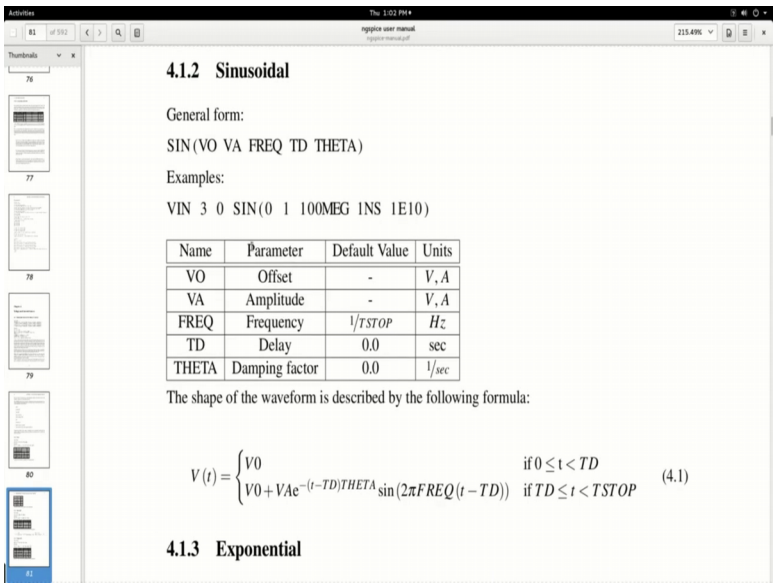

#### 4.1.2 Sinusoidal

General form:

SIN(VO VA FREQ TD THETA)

Examples:

VIN 3 0 SIN(0 1 100MEG 1NS 1E10)

| Name | Parameter | Default Value | Units |
|---|---|---|---|
| VO | Offset | - | $V, A$ |
| VA | Amplitude | - | $V, A$ |
| FREQ | Frequency | $1/TSTOP$ | $Hz$ |
| TD | Delay | 0.0 | sec |
| THETA | Damping factor | 0.0 | $1/sec$ |

The shape of the waveform is described by the following formula:

$$V(t) = \begin{cases} V0 & \text{if } 0 \le t < TD \\ V0 + VAe^{-(t-TD)THETA}\sin(2\pi FREQ(t-TD)) & \text{if } TD \le t < TSTOP \end{cases} \quad (4.1)$$

#### 4.1.3 Exponential

This is the n g spice manual you see the general syntax sign, we offset, we amplitude, frequency, delay and the damping factor. So, you can give a dammed sine wave also. This is an example of the sign you have the V in between the positive node. And the

other node sign 0, offset 1 amplitude 100 MEG frequency. What we need to give is 0 offset 3 V m root 2 or 325, 230 root 2 or 325 volts amplitude 50 hertz 00, so that is what we will do.

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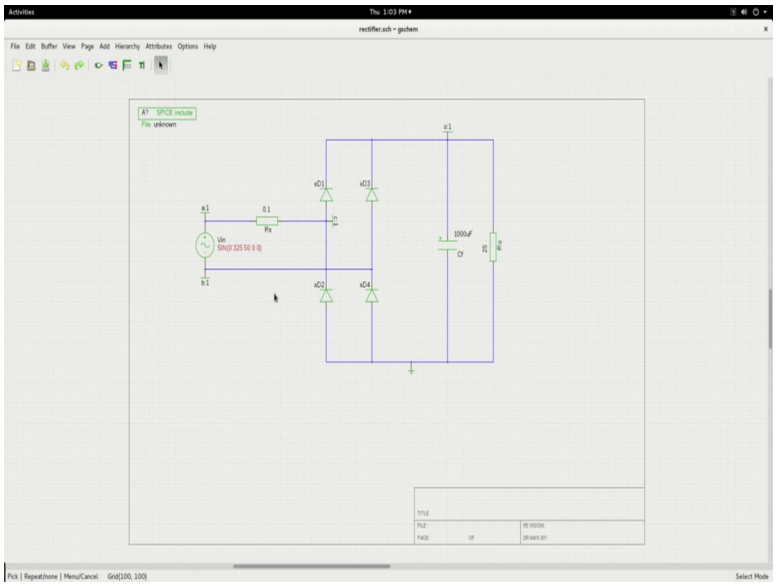

So, we shall put it as sign spices case insensitive 0, 325 volts is what we have V 1 50 hertz. What we wore no delay and no damming, so that is it that is source is set.

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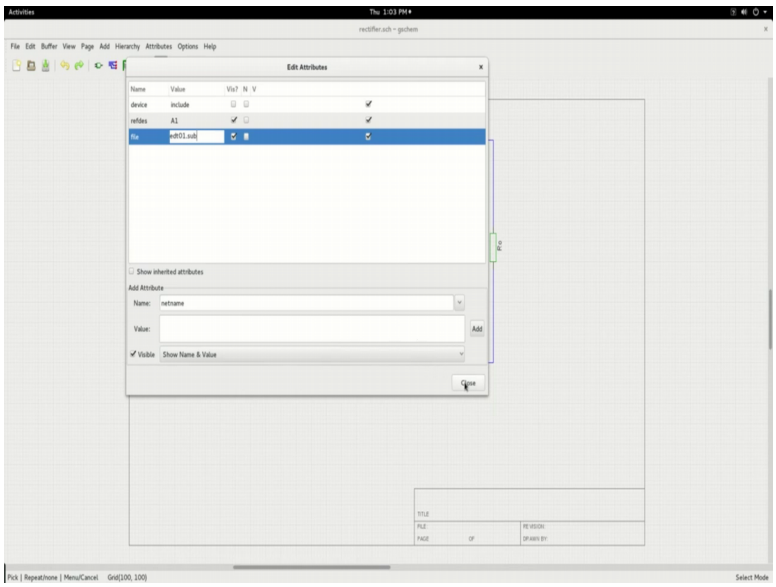

Now, to the intro directory at a directive you make correct s. value 1 and the file. So, right now I will type in a file e d t 01 dot s u v, e d t is electronic design technology 01

dot s u v, you can have your own name which is convenient and close. So, it will reflect here, and this is the file that will get included when you generate the netlist, so good time to save, save the file. Let us close the circuit.

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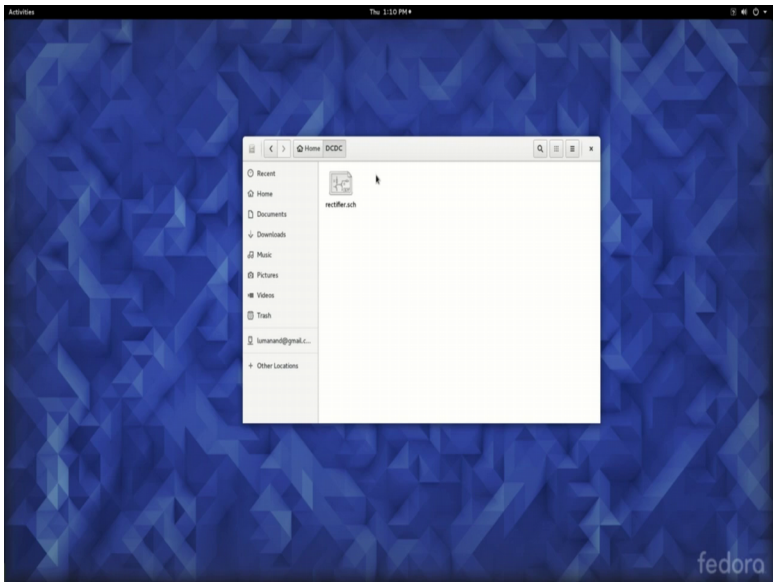


The schematic, and now you see that in the DCDC folder. We have rectifier dot s e h. So, we have now the schematics ready, but we have to add two more files, one file we will save as into the DCDC.

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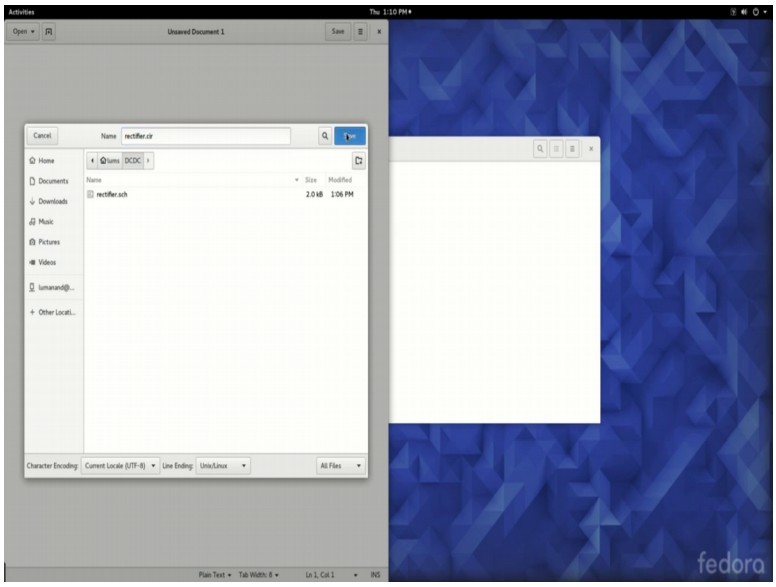

I will name it as rectifier dot c ir. Always keep the same, the same name as the two schematic file name, and only the extension you change it to cir, save that.

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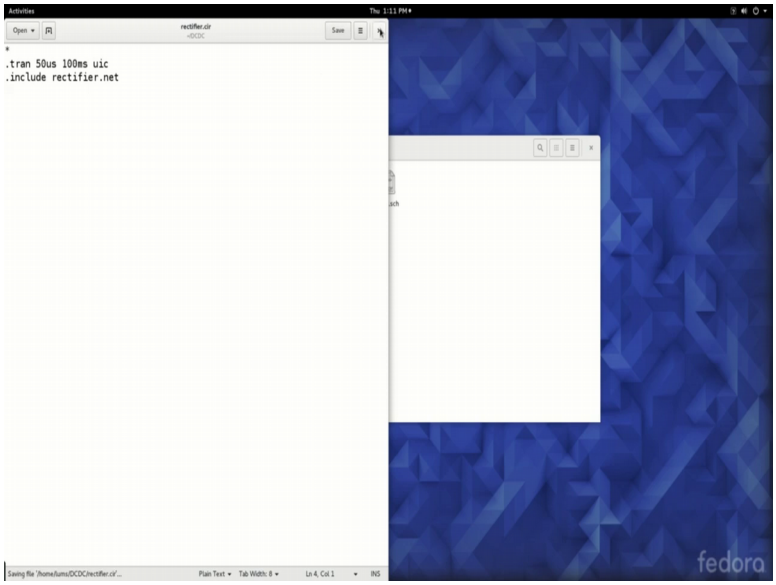


And here first line is always a comment. So, start from the second line, we walk we would like to do, sorry, we would like to have a branch and analysis perform step time of 50 micro second up to 100 millisecond using the initial conditions. Also include the rectifier dot net rectifier for dot net is not yet generated, but we will shortly generate that I will let you know how to do that.

So, these two control statements for simulation include it in a separate file never include it into the net file. It is better if you do it in this kind of an organized way, so that later on for modification complex simulations it would be very, very easy, save that and close this file. So, now you have rectifier dot cir also here. One more file we will include you remember that we had a e t d 01 dot sub file which is supposed to contain the models. So, let me save this in the same directory.

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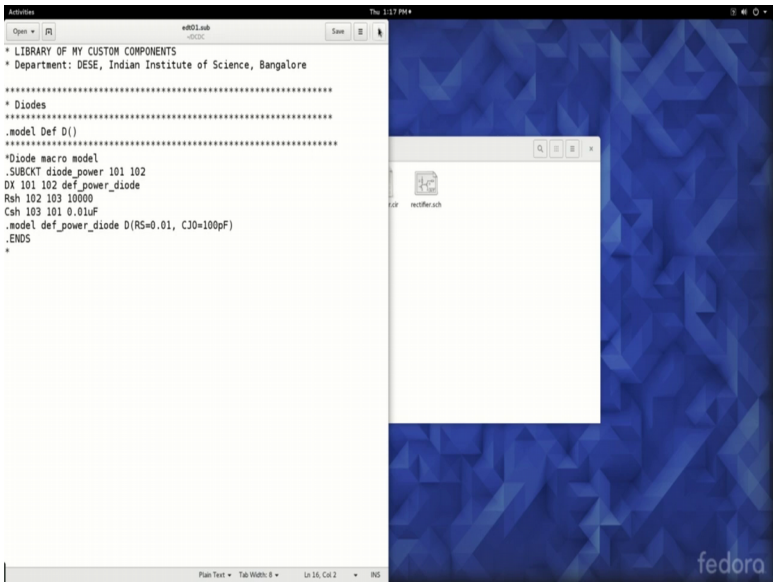


And this time e d p 0 1 dot s u v and save that. So, this we have linked in as an include directive. And what should this contain. This is a library of my custom components. So, you could have DESE science Bangalore can have your own thing ok. What is it that we need to provide a model, we used a diode there and it was a power diode let us have a model for that. So, the power diode is consisting of two parts, a model for the diode T 40, diode and the model sub circuit model for the power diode.

So, I will just write this. I think you know how to use spice how to make sub circuits. So, I will not right now teach about, how to go about making sub circuits, because it is outside the scope of this course. I assume that you know spice modeling model I will give a name def now d this is a default diode model of a default diode. Now, let me model the power diode. Now, it is a macro model. It is it is useful to how this macro model sub circuit model, because there are a lot of non idealities which will not take care in the default ideal diode which you can take care in the subcircuit model, and it will the convergence numerical conversions will be much better.

So, dot sub circuit I just put 13 caps just recognize that however, spice is case insensitive. So, let me write down the model first and diode. Let me take a normal ideal diode say a default power diode can give some descriptive names I put a option between one naught two and three and some high value 10,000 ohms. And C shut one not three one naught one 0.01 microfarad dot model, default power diode D, which has RS series

0.01 junction capacitance of 100 p f dot end s end the sub circuit. So, this is the sub circuit save that.

So, I think you recognize this you have the diode between one naught one and one naught two and you a resistant shunt resistance, then again in series with a shunt capacitance. So, R shunt and R c shunt are in series and across the diode dx. So, this can be closed. And we have required files. This is referred already in the schematic. This rectifier dot c a r gives you what is the type of analysis that you want to perform.

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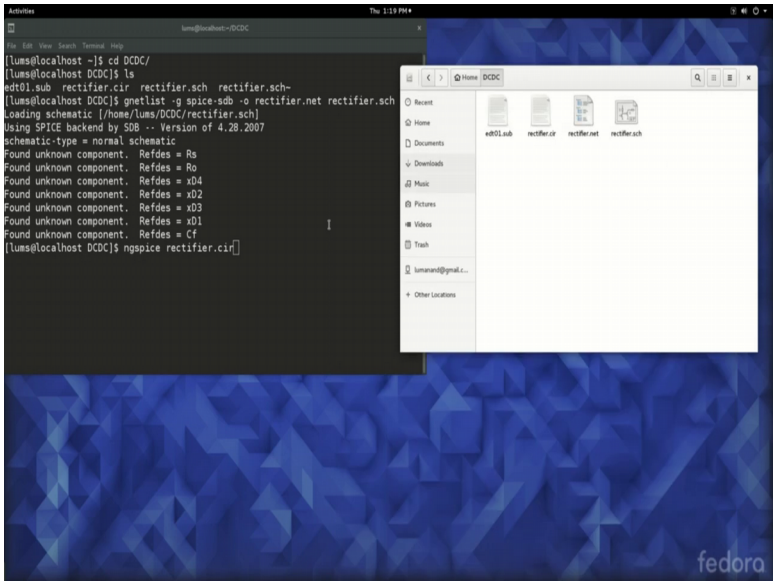


And we need now to generate the netlist. So, generating the netlist pretty simple, open a terminal and we will go into that folder through the terminal. You see that all these files of there. So, let us generate netlist from the schematic. The command is like this g netlist, slash g spice s d b dash o rectifier dot net. We want the output to rectifier dot net from rectifier dot s c h schematic. So, when you run this, it will generate the netlist. So, if you look there is a rectifier dot net generated. Now, these three files are the ones that will go into n g spice or simulation.

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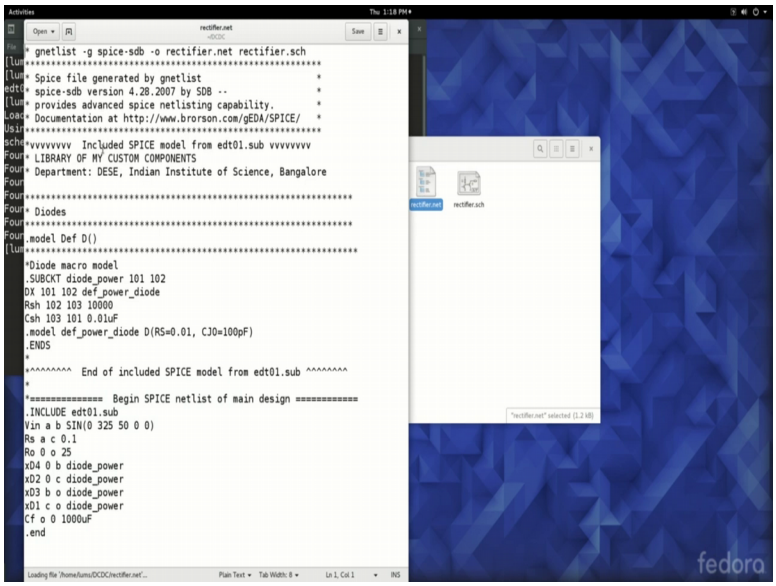


So, if you look at the not let you see the generated netlist, the models taken from the e d t sub because of the intro d dt dot s u b, you see the v in between a and b we have applied the labels and it can the label names for the nodes r s, r naught the powers power diodes and the capacitance. Now, we just have to simulate. So, let us go through the simulation process. You are already in the DCDC folder; you have to call n g spice. So, you say n g spice rectifier dot c a r you call a rectifier dot c i r because within c i r, you already have said include rectifier dot net. So, it will appropriately take the netlist from here.

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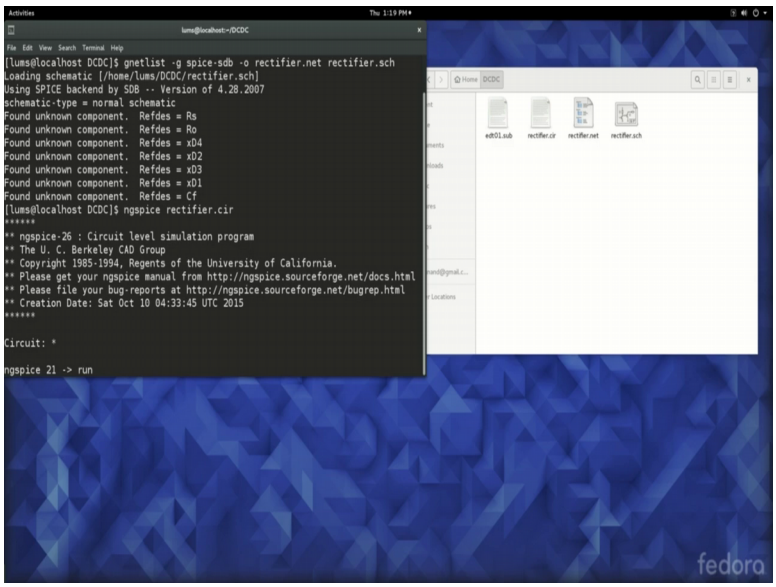

So, now you go into the n g spice environment. So, the n g spice environment has the circuit taken into its memory space, workspace, run type the command run.

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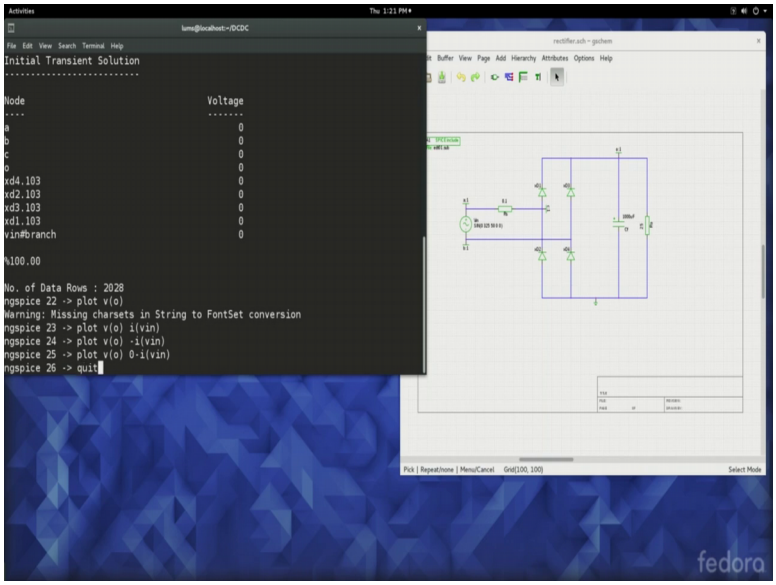


It will run the circuit, and these are the nodes plot vectors that you will have. What we have to do next is let us plot v naught or the output. You can always open the schematic for reference keep it by your side here, and let us say we want to plot this plot p naught plot v v naught. You will see the plot come up you can double click on that.

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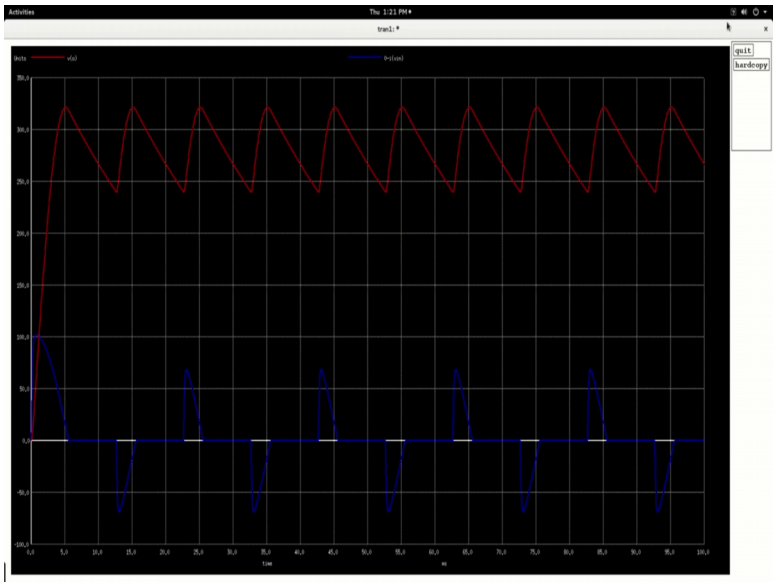

And then you see the capacitor charging from the starter and then the rebels as we had discussed in theory close that you want to probably see the source current here. So, let us say plot v naught a and also I would like to plot the current of which branch v in branch v in branch here and then you will see that you see the current.

Now, the current through the source is always considered in the opposite direction. So, therefore, you see that it is shown minus, but actually the current is in flowing in this direction. So, whenever you take a source branch, you can give minus of that. By for example, you can say plot v naught minus I v in sorry plot v naught 0 minus v in. So, this was the proper direction of that kind. You see that initial starter current is higher than the normal steady state current as we had discussed in the last session. So, after this quit and you are out. So this completes the one assimilation process. There are a few points and tips that I would like to mention at this point which I will do so.

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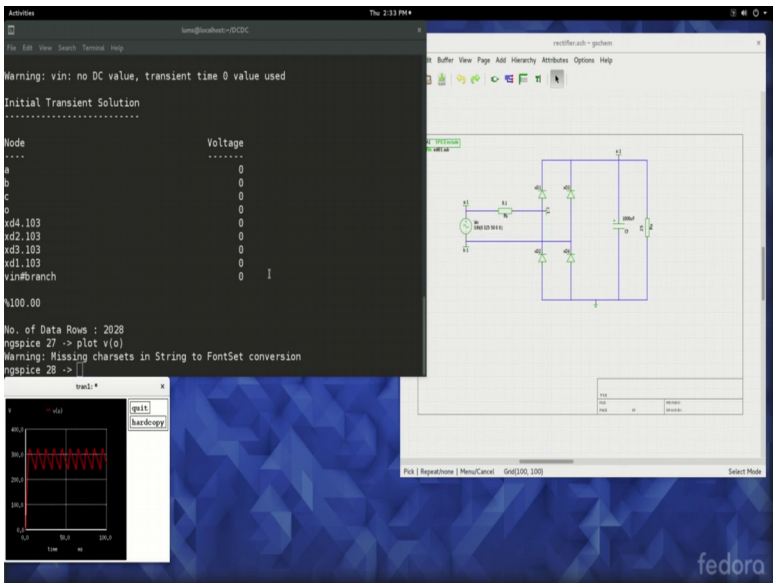


Now, now in the case of the simulation after generating the netlist use the n g spice. One issue with the n g spice plot, n g spice rectifier dot cir, and the (Refer Time: 28:47) see that plot, take some example v naught though the plot is of a good quality and you can expand it compressive.

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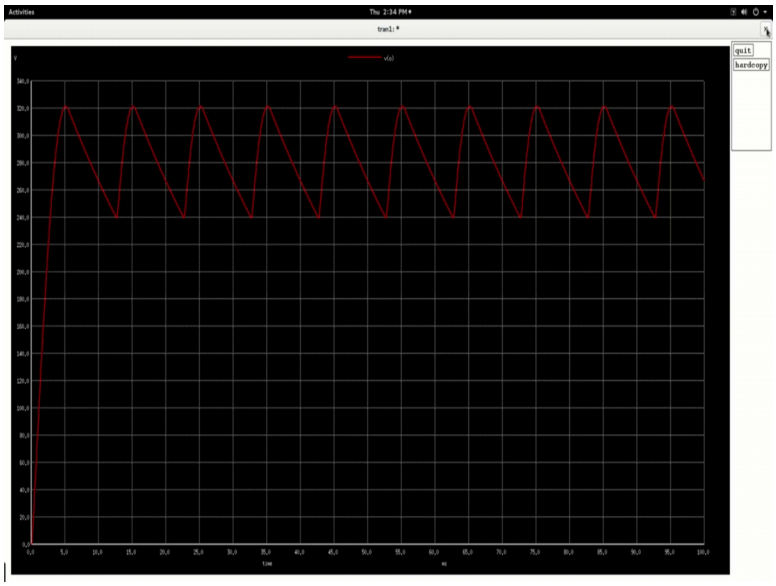


And you see that you can also zoom into a particular part, you will get an expanded you also of that, all these are possible. The only way you can take this for documentation is by making a screen capture short of that so which can be pretty high memory when you are making a document. And when you make the document, you will get this black background. And hard copy is only for directly taking it as a printout. Therefore, for the purposes of documentation, this n g spice plot is not very comfortable I would say. So, you can do some documentation with that that is one issue.

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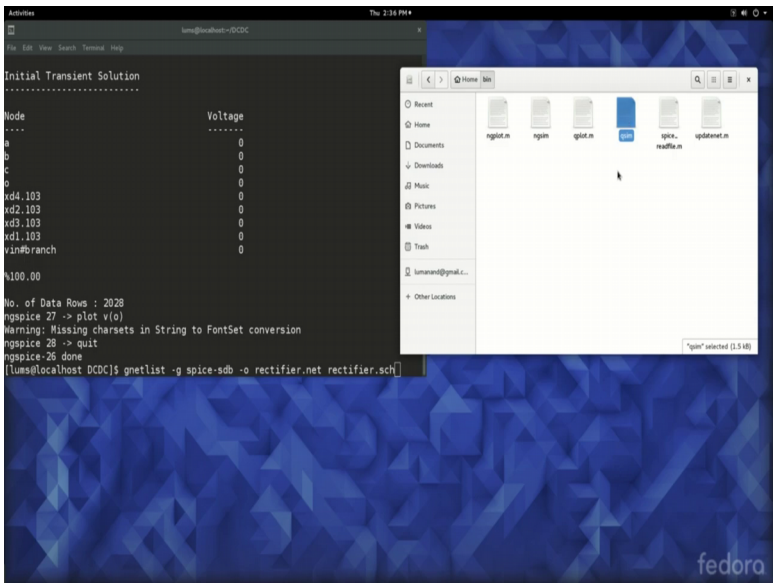

And the other issue that we saw is at the time when we were generating this netlist. So, when we generated the netlist from the schematic, we used a command like this g netlist dash g e spice dash s e b so on so on. But every time typing is every time you make a change in the schematic, you have to type this out and then generate the netlist dotnet file. What you can do is put this into a script file, and then keep calling it in a generic way for any such simulation.

So, combining these two problems and making a script such that these two problems are solved using octave, we have generated we have made a script file and that is what you had initially copied and put into the bin directory here. So, in the bin directory, in the last session, we had copied sits files and put it into this folder from resources. You see that there is squeeze qsin and then there is a n g n g sem. Now, this qsin is an octave script which takes care of the issue of this netlist command generating netlist command.

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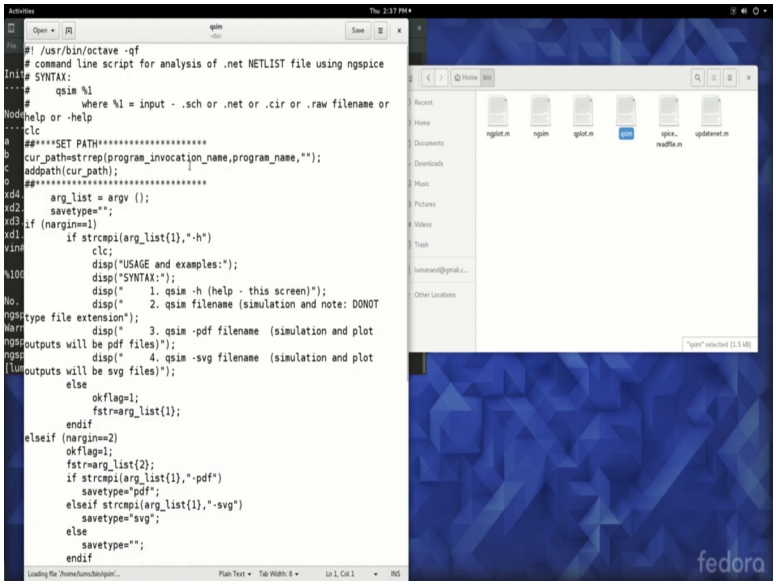


And also to show you the waveforms using octave or MATLAB type of commands, and also to put an output in the form of a PDF file.

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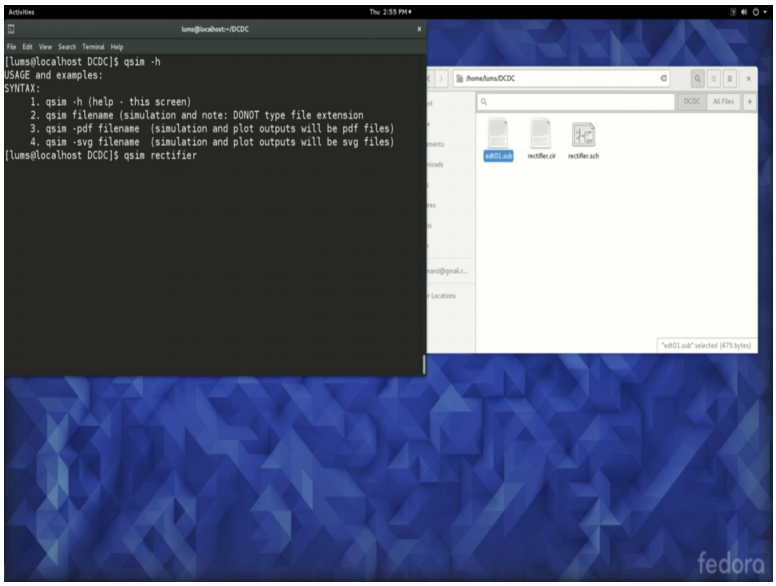


Qsin what it will do is it will take the netlist do the spice simulation, and then put the results of the simulation in to the raw file. And the raw file is passed as a parameter to the spice as spice read file (Refer Time: 32:16) file. This, this is a open source tool function available from n g spice whish which can be downloaded, but I have included it in the resource you can use it.

So, it will read this raw file, and then the octaves g n u plot is used for plotting g nu plot is very powerful and you can have different types of outputs PDF outputs or s v g output from that. So, that is what we do. And this is a small script file written by us here. It is there are there is lot of scope for improvement in this it is just a sample type of script file which goes to show what you can do and there is lot that you can. N g sin is actually as also similar to qsin only that it also generates the rectifier dot c i r file thus many times we forget, forget to forget the syntax what you want to write or plan you know is the step size ending time n u i c, but if it is an a c analysis or if it is bias for analysis so many other analysis which are there you may forget the syntax, so that way n g sin helps you do that one.

So, I will leave you to go through that and use it if you feel that it is comfortable. I will just show one small example with qsin we are in the DCDC folder. I will run qsin slash h for health, so that you know what to do. So, you have to give it in this form slash h will give you this particular screen, qsin file name without the extension. So, qsin rectifier

without the dot s c h just say qsin rectifier. It will appropriately take the appropriate files generate the net file, and then the n g spice or raw output file which will be used by octaves g n u plot, it will be read by the spice, read find m dot m, and then a cube plot dot m will be used to plot the outputs.

So, these are some of the syntax which you do not need to now use these two syntax because the g n u plot itself will give you an output whatever format you want. So, let me just run qsin rectifier. Now, you do not need to have generated the net file. So, what we will do I will just delete this netfile to show that that was not needed immediately after you do those schematics, you have, this you should have this. And of course, edit zero one dot sum qsin rectifier will generate the netlist, will generate raw file output which contains all the results of the simulation.

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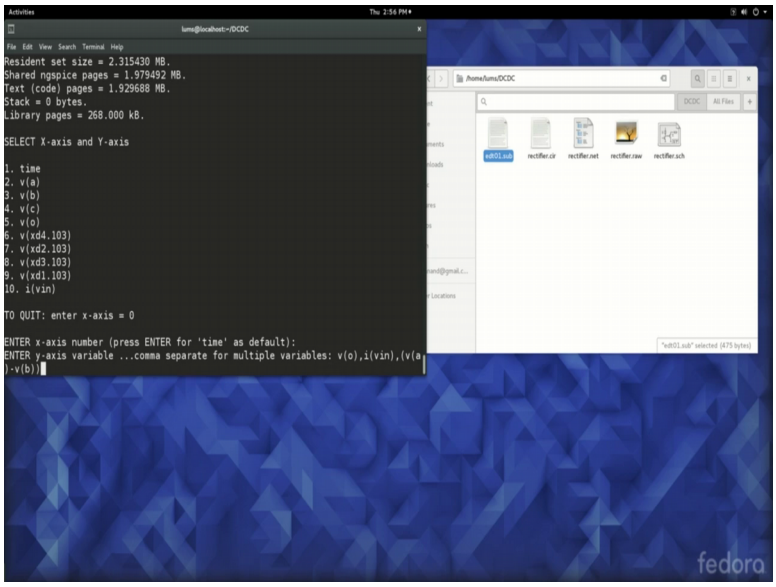


Now I the default time, so I can give it as v naught, now here are to become a separation I can say current through v in things like that I can also give the v v a minus v b. So, all this let save like to see.

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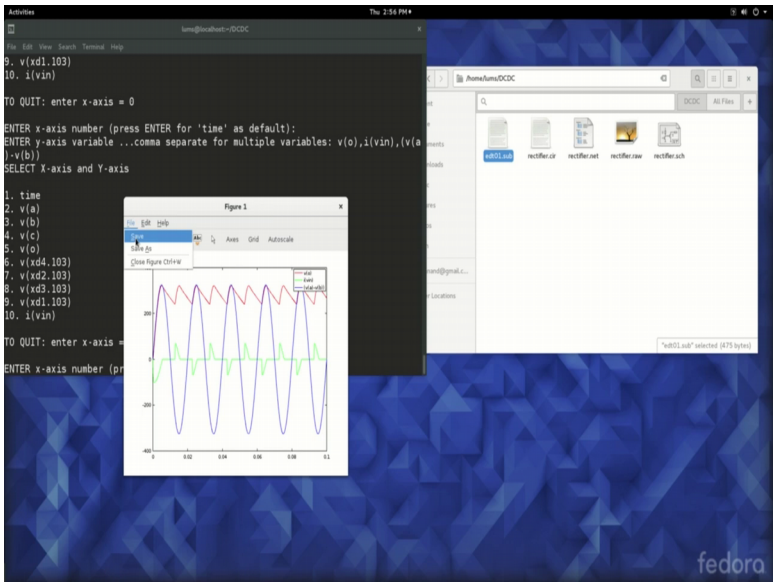


So, you will see it something like this g n u brought output, and you see here you have you can save it into the file.

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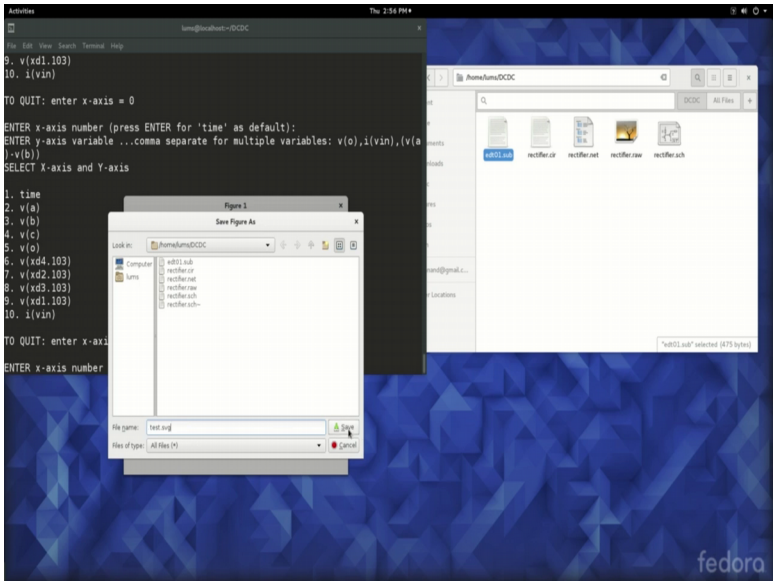


So, now let us say save as test dot s v g save, and then I will come out of qsin. So, here you will see the test dot s v g which can which can be taken into any of the graphics package like vector graphics package like in scape.

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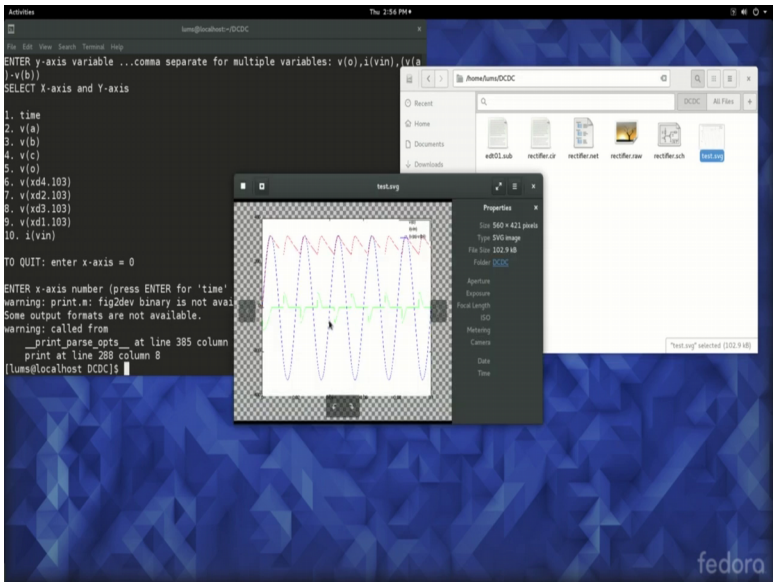


Or anything similar packages and you can do further editing and then put in to the documentation. So, this is how we go about doing a complete simulation starting from schematics and n g spice and the plot holes.